

# PIR MCU

(Pyroelectric Infrared Motion Sensor)

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## . General Description:

The MCU provides high cost-performance for Pyroelectric Infrared Sensor application. It designs by LSI high technology with low power CMOS process.

## . Features:

- ◇ Use 4 bits microprocessor core
- ◇ Operating Voltage:
  - OTP : 2.4v-5.5v (TTR561)
  - Mask : 2.4-5.5v (TTU561)
- ◇ System oscillator
  - 32Khz RC oscillator external Resistor and Capacitor ( OSCL )
  - Built-in 256Khz RC oscillator (OSCH)
- ◇ User ROM 1K\*16, RAM 64\*4
- ◇ Built-in 2 stacks
- ◇ Built-in one 8-bit Timer/Counter with internal overflow interrupt
- ◇ Built-in time base timer function with overflow interrupt function
- ◇ Built-in watch dog timer function
- ◇ Built-in analog signal wake up & interrupt function
- ◇ Built-in low power consumption CMOS OP\*2(operation amplifier)
- ◇ Provide 8 I/O ports (share with 6 channel comparator input)
- ◇ Provide 6 channel comparator input with internal voltage reference
- ◇ Provide three voltage reference
- ◇ Provide internal reset function and external reset pin

## . Application:

- PIR security application (Motion sensor)
- Sensor detected application (IR sensor/ Shock sensor etc.)
- 運放 + 單片機整合運用



## . AC / DC Characteristics

### 1 Absolutely max. Ratings

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-20- +70	°C
Storage Temperature	Tsto	-50- +125	°C
Supply Voltage	VDD	6.0	V
Voltage to input terminal	Vin	Vss-0.3 to Vdd+0.3	V
ESD*	Esd	3	KV
Package soldering	S <sub>TEMP</sub>	255-260	°C
	S <sub>TIME</sub>	20-40	Sec

\* ESD standard is MIL-STD-883 Method 3015 of Human Body Model

### 2 D.C. Characteristics

(Condition : Ta= 25 ± 3 °C , RH ≤ 65 % , VDD =+ 5V , VSS=0V)

Item	Symb ol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	VDD	OTP	2.4	5	5.5	V
Operating voltage	VDD	MASK	2.4	5	5.5	V
Power consumption current	I <sub>OPR1</sub>	System clock off, A/D on, No load, @5V, when option is [ DC type ]		30	60	uA
Power consumption current	I <sub>OPR2</sub>	System clock off, A/D on, No load, @5V, when option is [ AC type ]		90	180	uA
Power consumption current	I <sub>OPR3</sub>	System clock at 32Khz RC oscillator, A/D on, No load, @5V When option is [ DC type ]		50	100	uA
Power consumption current	I <sub>OPR4</sub>	System clock at 256Khz RC oscillator, A/D on, No load, @5V When option is [ DC type ]		250	500	uA
Power consumption current	I <sub>OPR5</sub>	System clock off, A/D on, No load, @3V, the mask is [ DC type ] only		25	50	uA
Power consumption current	I <sub>OPR6</sub>	System clock at 32Khz RC oscillator on, A/D on, No load, @3V		50	100	uA
Power consumption current	I <sub>OPR7</sub>	System clock at 256 Khz RC oscillator on, A/D on, No load, @3V		200	300	uA
stand by current	I <sub>st</sub>	System halt, No load, RC oscillator off, A/D off, @5V		1	2	uA
Input low voltage for input and I/O port	V <sub>IL1</sub>		0		0.3VDD	V
Input high voltage for input and I/O port	V <sub>IH1</sub>		0.7VDD		VDD	V
Input low voltage for RESB pin	V <sub>IL2</sub>		0		0.35VDD	V
Input high voltage for RESB pin	V <sub>IH2</sub>		0.7VDD		VDD	V
Output port source current	I <sub>OH1</sub>	V <sub>OH</sub> =0.9VDD, @5V	4			mA
Output port sink current	I <sub>OL1</sub>	V <sub>OL</sub> =0.1VDD, @5V	10			mA

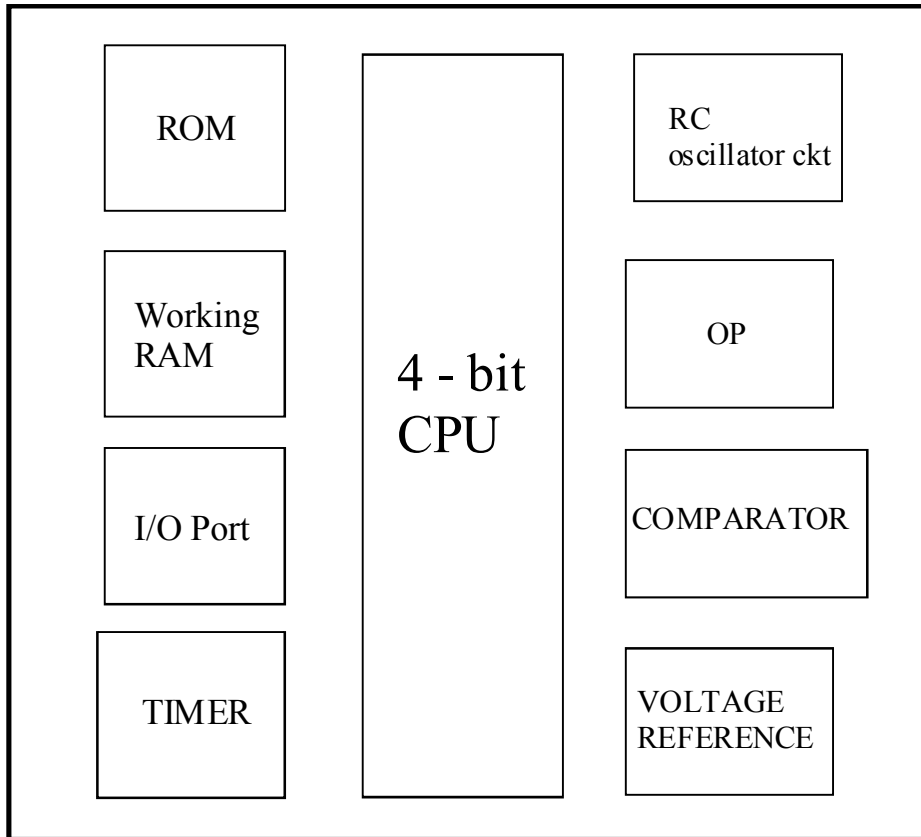
### 3 A.C. Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
System clock	f <sub>SYST</sub>	RC oscillator @5v (32Khz) 外接固定電阻/電容	28	32	36	KHz
External reset low pulse width	t <sub>RES</sub>		1			us

### 4 Operational amplifiers features (VDD=5V, 25°C)

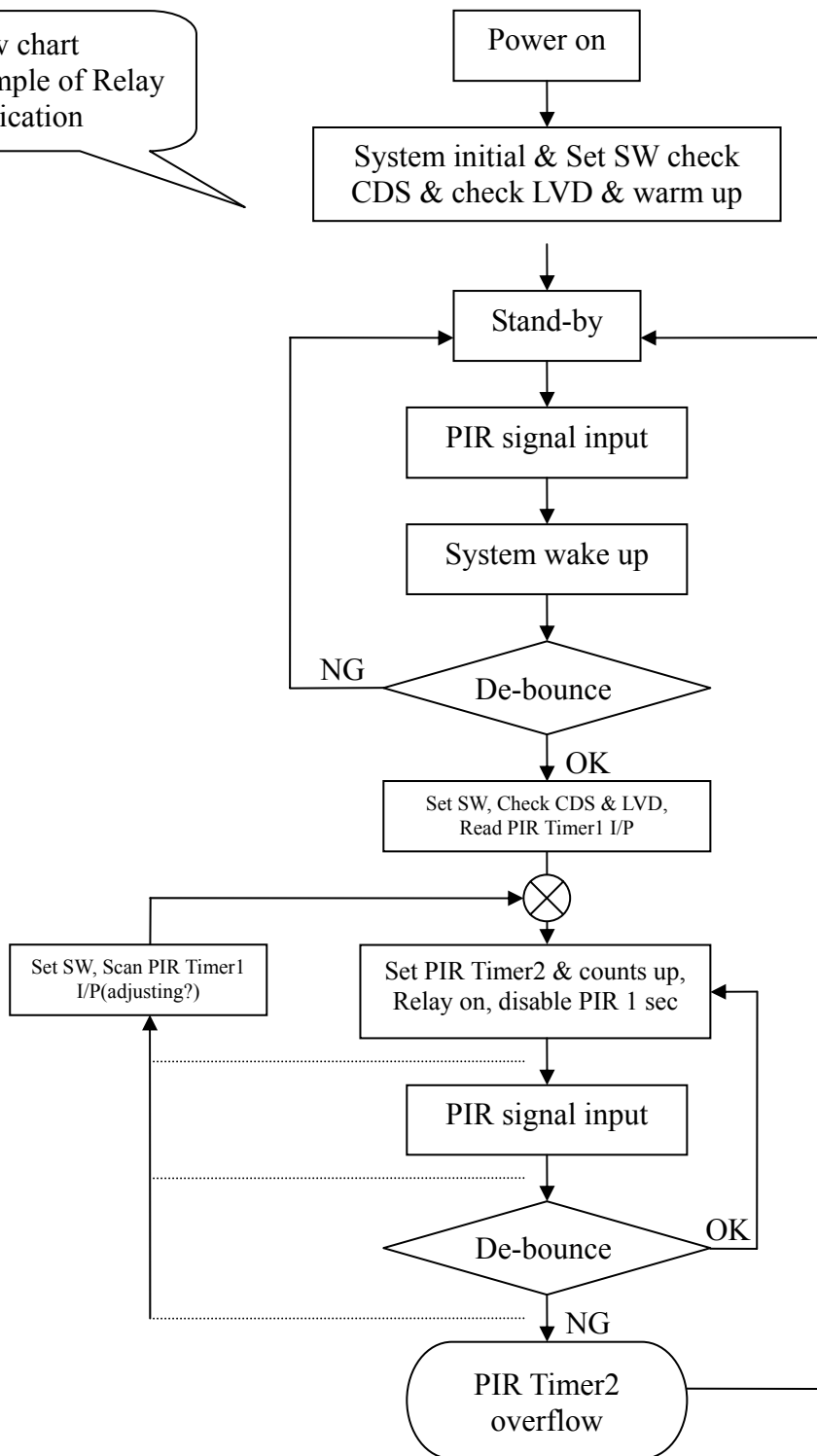
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input offset voltage	Vios			5	10	mV
Input offset current	Iios			1	100	pA
Input bias current	Iib			10	200	pA
Positive output swing	Vsh		4.1	4.4		V
Negative output swing	Vsl			0.1	0.2	V
Unity Gain Bandwidth	fb	Loading,C=50p		5		KHz
Common mode reject ratio	CMRR	Vo=1V	60	65		dB
Supply voltage reject ratio	SVRR	Vo=1V	60	65		dB
Slew rate at a unit gain	SR	No load	0.01			V/us
PIR window midpoint	Vref		2.3	2.50	2.7	V
Output short source current	Ioph	(Vin+)-(Vin-)>10mV	5			mA
Output short sink current	Iopl	(Vin+)-(Vin-)<10mV	5			mA

. Block Diagram



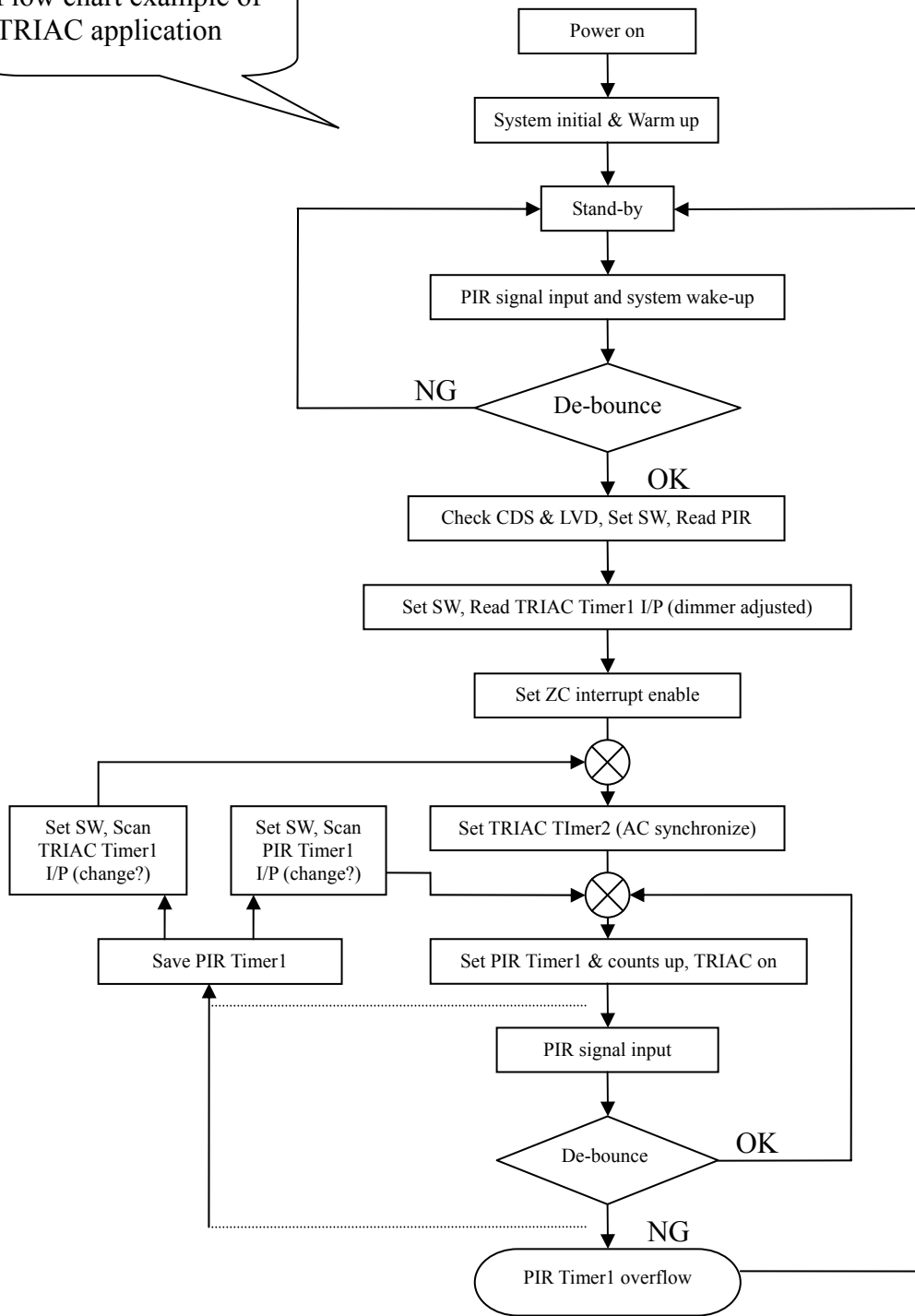
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Flow chart  
example of Relay  
application





Flow chart example of TRIAC application



. Function Description

1 Map of memory and I/Os

000H	(DP1)
001H	A
002H	TB1
003H	TB2
004H	TB3
005H	DPL
006H	DPM
007H	DPH
008H	PS
009H	INTF
00AH	INTC
00BH	SV&ADoff
00CH	PA
00DH	PAC
00EH	PAINT
00FH	PB
010H	PBC
011H	AD&VR
012H	TB
013H	CHS
014H	TMR1L
015H	TMR1H
016H	TMC1
017H	Reserved
018H	
019H	
01AH	
01BH	
01CH	
01DH	
01EH	RAM
01FH	
020H	
05FH	Reserved
060H	
FFFH	

Data memory map

000	Reset vector
001	INT vsector
002	On-chip program memory
3FF	
400	
FFF	Reserved

Program memory map

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**2 CONTROL REGISTER TABLE**

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
008H	PS	x	H/L	SLEEP	STOP	0100
		x	R/W	R/W	R/W	
009H	INTF	CPF	TM1F	ADF	TBF	0000
		R/W	R/W	R/W	R/W	
00AH	INTC	CPIE	TM1IE	ADIE	TBIE	0010
		R/W	R/W	R/W	R/W	
00BH	SV&ADoff	ADOFF	SV2	SV1	SV0	0000
		R/W	R/W	R/W	R/W	
00CH	PA	PA3	PA2	PA1	PA0	1111
		R/W	R/W	R/W	R/W	
00DH	PAC	PAC3	PAC2	PAC1	PAC0	1111
		R/W	R/W	R/W	R/W	
00EH	PAINT	RF1	RF0	PA0IE	PA0F	0000
		R/W	R/W	R/W	R/W	
00FH	PB	PB3	PB2	PB1	PB0	1111
		R/W	R/W	R/W	R/W	
010H	PBC	PBC3	PBC2	PBC1	PBC0	1111
		R/W	R/W	R/W	R/W	
011H	AD&VR	ADN	ADP	VR1	VR0	0000
		R	R	R/W	R/W	
012H	TB	x	TB2	TB1	TB0	u000
		x	R/W	R/W	R/W	
013H	CHS	CPO	CH2	CH1	CH0	u000
		R	R/W	R/W	R/W	
014H	TMR1L	TMR1_3	TMR1_2	TMR1_1	TMR1_0	0000
		R/W	R/W	R/W	R/W	
015H	TMR1H	TMR1_7	TMR1_6	TMR1_5	TMR1_4	0000
		R/W	R/W	R/W	R/W	
016H	TMC1	RL1	CK1S1	CK1S0	TMR1S	0000
		R/W	R/W	R/W	R/W	

**3 SYSTEM CONTROL REGISTER**

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
008H	PS	-	H/L	SLEEP	STOP	1100
		-	R/W	R/W	R/W	

STOP : high active ◦

SLEEP : high active ◦

Power on reset 或是從 STOP mode wake up 都是執行 high speed mode operation ◦  
 進入或是解除 STOP or SLEEP mode 時，H/L state 不變，都保持原來 state ◦

Function status \ Operating mode	SLEEP(high active)	STOP(high active)
Oscillator	Operating	Stopped
CPU internal status	Retain the status	
Memory, Flag, Register, I/O	Retain the status	
Program counter	Hold the executed address	
Timer/Counter	Operated	Stopped & Retain
Watch-dog timer	Disable	
Release Condition( and clear STOP or SLEEP flag)	AD-INT/ TMR1-INT/ TB-INT/ PA3-Wake-up/ PA2-Wake-up/ PA1-Wake-up/ PA0-INT CP_INT	AD-INT/ PA3-Wake-up/ PA2-Wake-up/ PA1-Wake-up/ PA0-INT CP_INT

\* 有 INT 就做 wake up 的動作 ◦

Oscillator stable time :

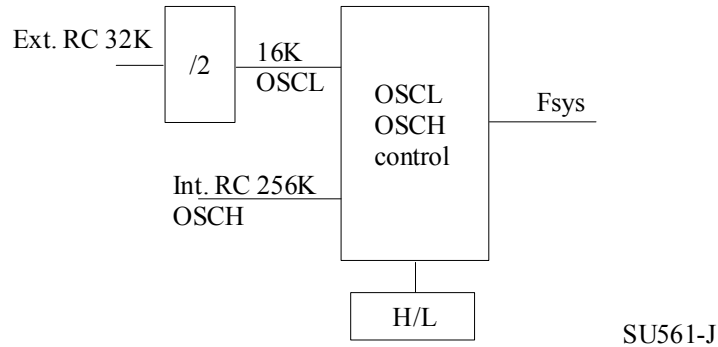
1. When power on reset or WDT overflow or external reset: OST is 1024 system clock
2. When STOP mode wake up: OST is 128 system clock
3. When SLEEP mode wake up: OST is 128 system clock
4. When low speed change to high speed: OST is 128 system clock(OSCH)

**4 RC OSCILLATOR CONTROL REGISTER**

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
008H	PS	-	H/L	SLEEP	STOP	1100
		-	R/W	R/W	R/W	

H/L : Oscillator speed control register ◦

FLAG	FUNCTION
H/L	Low : oscillator low speed mode (OSCL) High : oscillator high speed mode (OSCH)



CPU 的 instruction cycle 是 OSCL 除以 2 或是 OSCH 除以 2 ◦

**5 PIR signal window selection & analog circuit control**

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
009H	INTF	CPF	TM1F	ADF	TBF	0000
		R/W	R/W	R/W	R/W	
00AH	INTC	CPIE	TM1IE	ADIE	TBIE	0010
		R/W	R/W	R/W	R/W	
00BH	SV&ADoff	ADOFF	SV2	SV1	SV0	0000
		R/W	R/W	R/W	R/W	
011H	AD&VR	ADN	ADP	VR1	VR0	0000
		R	R	R/W	R/W	

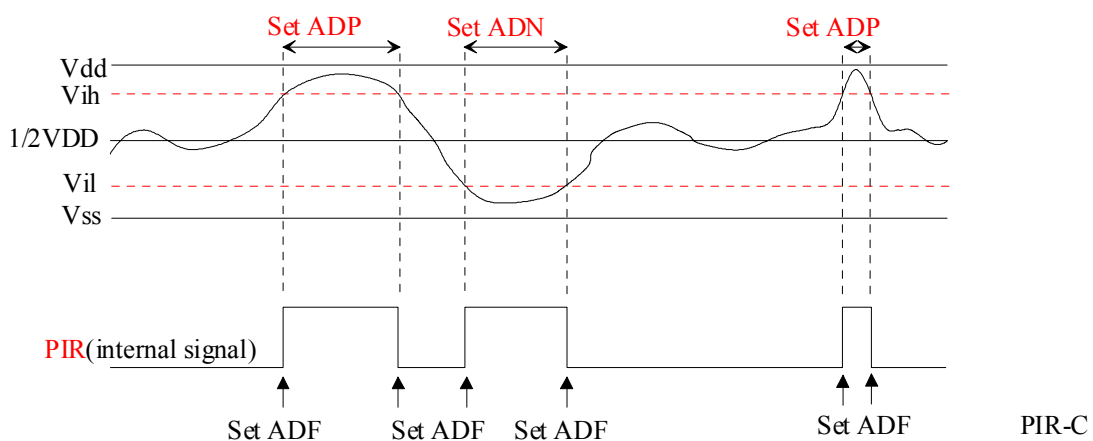
ADF：輸入訊號只要超過 PIR window，就要 set 此 flag，此 flag 在 read 後，要用 software write 來 clear。

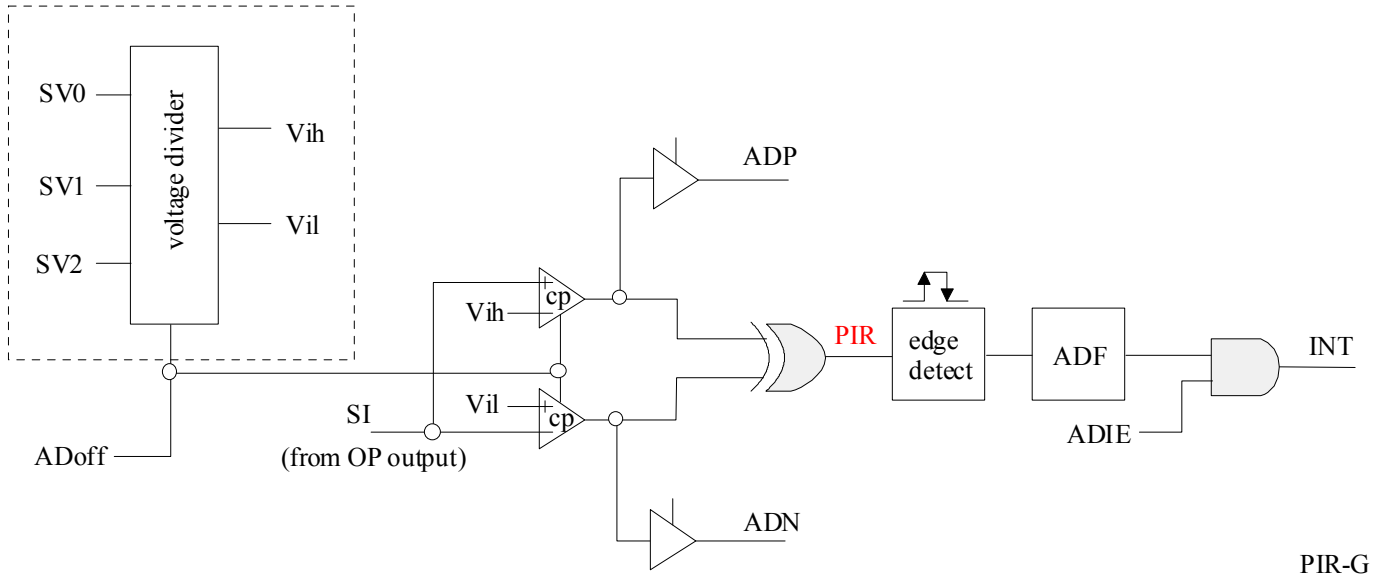
ADIE：ADF interrupt 的 enable 控制腳（default 是 high，是 enable wake up & interrupt function）。

ADOFF：為 high 時，會 disable 所有的 OP 線路。

SV0, SV1, SV2：adjust PIR signal window range。PIR 中心點為 0.5VDD，其 WINDOW 是以此中心點為參考點，而訂出的一個 PIR WINDOW，其值如下表：

SV2	SV1	SV0	Vih	Vil
0	0	0	$0.5VDD + 0.07VDD$	$0.5VDD - 0.07VDD$
0	0	1	$0.5VDD + 0.10VDD$	$0.5VDD - 0.10VDD$
0	1	0	$0.5VDD + 0.13VDD$	$0.5VDD - 0.13VDD$
0	1	1	$0.5VDD + 0.16VDD$	$0.5VDD - 0.16VDD$
1	0	0	$0.5VDD + 0.19VDD$	$0.5VDD - 0.19VDD$
1	0	1	$0.5VDD + 0.22VDD$	$0.5VDD - 0.22VDD$
1	1	0	$0.5VDD + 0.25VDD$	$0.5VDD - 0.25VDD$
1	1	1	$0.5VDD + 0.28VDD$	$0.5VDD - 0.28VDD$





**NOTE :**

1. OP and Comparator 在 on 後，要等 200us 以上才能穩定
2. 切換 switch (SV0/SV1/SV2) 後，要等 20us 以上，訊號才會穩定
3. ADF flag 是在 PIR (internal signal) 有 edge 變化時，會被 set 為 high。ADP/ADN 是 level 輸出，所以要做 PIR de-bounce 時，需要用 ADP/AND 來做判斷，不能用 ADF 來做。

**6 Comparator and Pulse width measurement control**

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
009H	INTF	CPF	TM1F	ADF	TBF	0000
		R/W	R/W	R/W	R/W	
00AH	INTC	CPIE	TM1IE	ADIE	TBIE	0010
		R/W	R/W	R/W	R/W	
00CH	PA	PA3	PA2	PA1	PA0	1111
		R/W	R/W	R/W	R/W	
011H	AD&VR	ADN	ADP	VR1	VR0	0000
		R	R	R/W	R/W	
013H	CHS	CPO	CH2	CH1	CH0	u000
		R	R/W	R/W	R/W	

CPF : Comparator data register

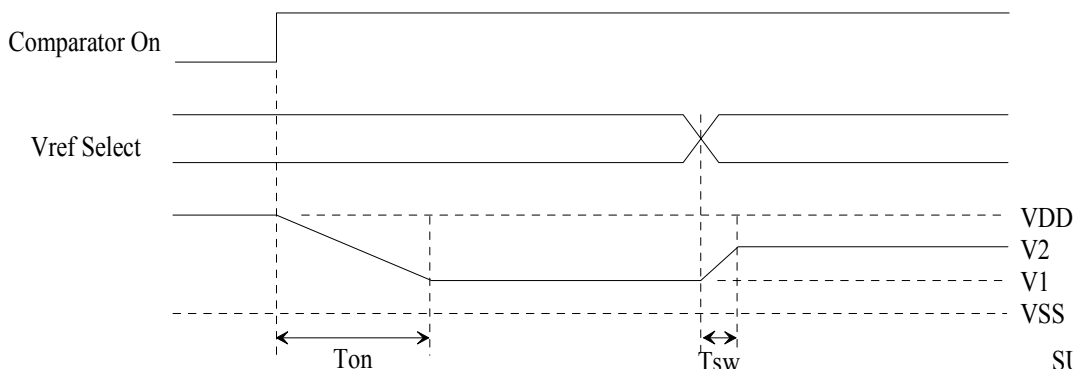
CPO : Comparator data out signal

FLAG	FUNCTION
VR1/ VR0	(VR1/ VR0) 00: Disable comparator and Vref function (VR1/ VR0) 01: select Vref voltage=2/3VDD (VR1/ VR0) 10: select Vref voltage=1/2VDD (VR1/ VR0) 11: select Vref voltage=1/3VDD
CH2/ CH1/ CH0	(CH2/ CH1/ CH0) 000&001&111: no analog input mode 。 (CH2/ CH1/ CH0) 010: select AD1(PA2) 。 (CH2/ CH1/ CH0) 011: select AD2(PA3) 。(CH2/ CH1/ CH0) 100: select AD3(PB0) 。 (CH2/ CH1/ CH0) 101: select AD4(PB1) 。(CH2/ CH1/ CH0) 110: select AD5(PB2) 。

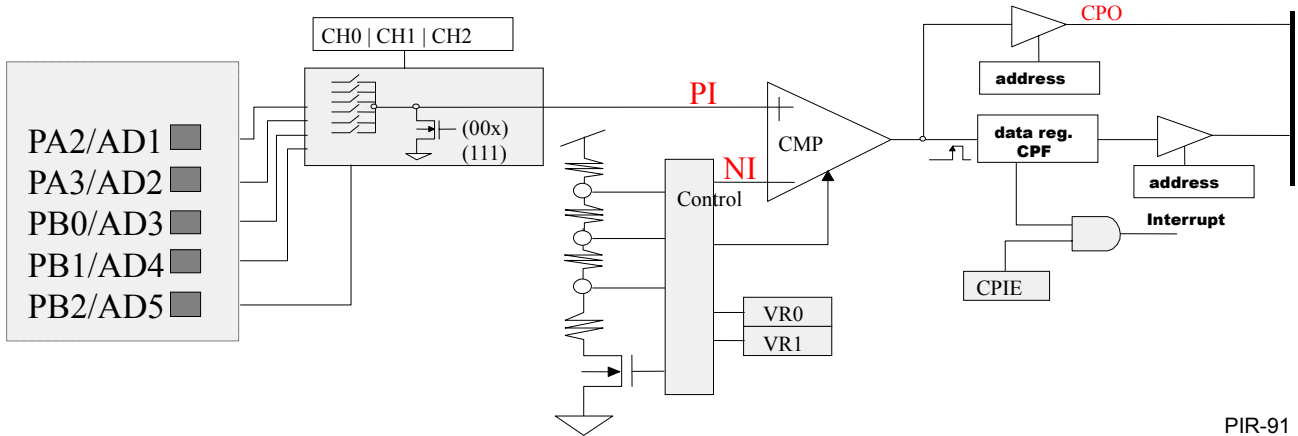
PA2-3 , PB0-2 : 在 input mode 時，沒有選擇 pull high function，則為 analog input function，而 channel select 是以 CH0/CH1/CH2 來選擇。

當 analog input function 使用注意事項：

1. 建議要切換 analog switch 時，都先把 CMP 的 interrupt disable (CPIE clear to low) 後，再切到所要的 channel，以防止不正常的 CMP interrupt 發生。
2. 切到要偵測的 analog channel 後，建議 delay 100us( $T_{on} @ VDD > 3V$ ) 以上，再來 read CPF flag 或是打開 interrupt enable，以讓 CMP 的 output stable。其後切換 Vref，建議 delay 20us( $T_{sw} @ VDD > 3V$ ) 以上
3. PI (請見下圖 PIR-91) 若是要 pull low，做 RC 充放電偵測 pulse width，可以利用 I/O port 的 output port 來拉 low。
4. 此時做 read 動作，會一直 read 到“1”。



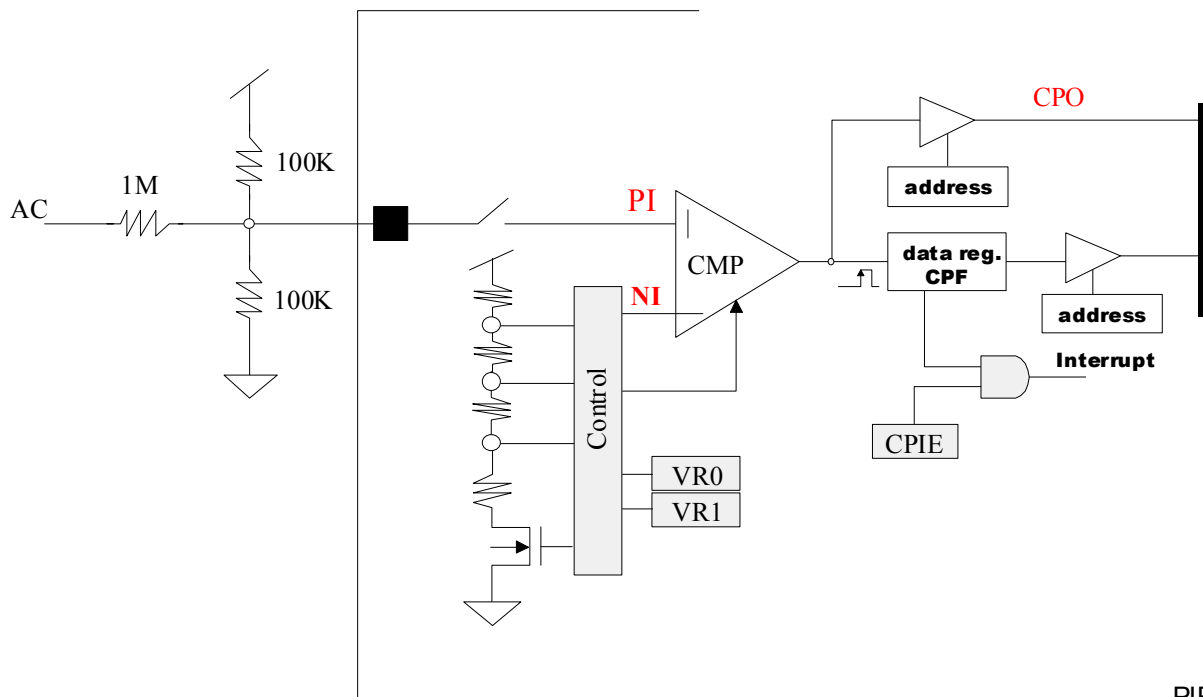




PIR-91

應用例子：

- 在 TRIAC 應用
- 必須取得和 AC signal 同步
- 可以用如下接法，先衰減 AC (110V/220V) 訊號
- 切換 VR0/VR1 使得 NI 點為  $1/3V_{DD}$  或是  $2/3V_{DD}$  模擬 Schmitt Trigger，切換時機可以經由 read CPO 來判斷
- 如此就可以取得準確的 ACsignal 同步訊號了



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## 7 I/O REGISTER

### A. Port A & B

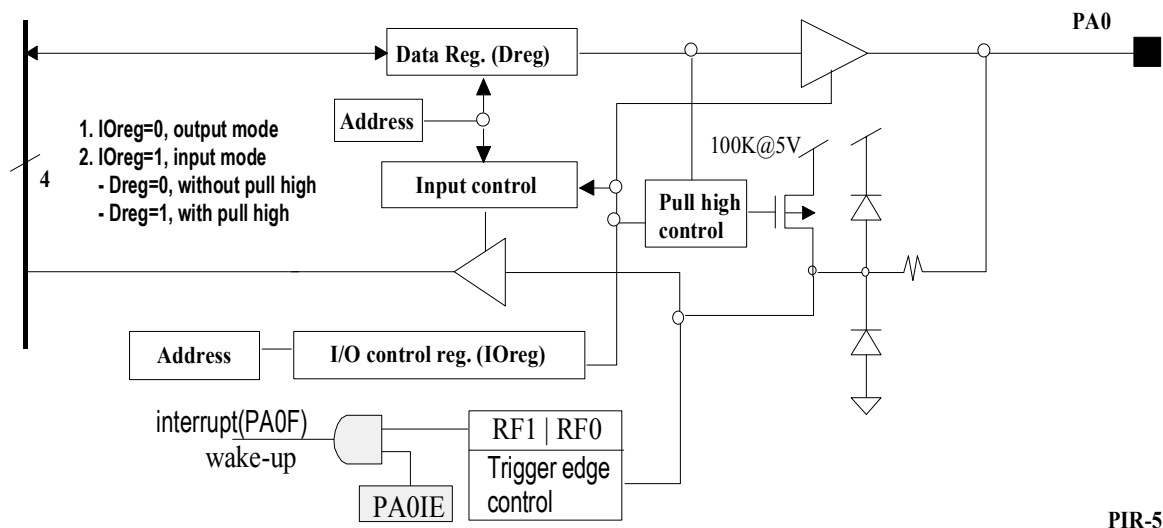
Address	Register	Bit3	Bit2	Bit1	Bit0	Initial state
00CH	PA	PA3	PA2	PA1	PA0	1111
		R/W	R/W	R/W	R/W	
00DH	PAC	PAC3	PAC2	PAC1	PAC0	1111
		R/W	R/W	R/W	R/W	
00EH	PAINT	RF1	RF0	PA0IE	PA0F	0000
		R/W	R/W	R/W	R/W	
00FH	PB	PB3	PB2	PB1	PB0	1111
		R/W	R/W	R/W	R/W	
010H	PBC	PBC3	PBC2	PBC1	PBC0	1111
		R/W	R/W	R/W	R/W	

PAC/PBC：是控制 I/O mode，為 high 時，是 input mode。

PA0：為 I/O port data，在 input mode 時，(Dreg) 可以控制是否有 pull high function，如下圖。在 input mode 時，有 interrupt 功能(rising edge and falling edge trigger)，當系統進入 STOP or SLEEP mode 時，可以用此 PIN 來 wake up，此時會 set PA0F flag。(Power on Dreg 為 high，是有 pull high function)

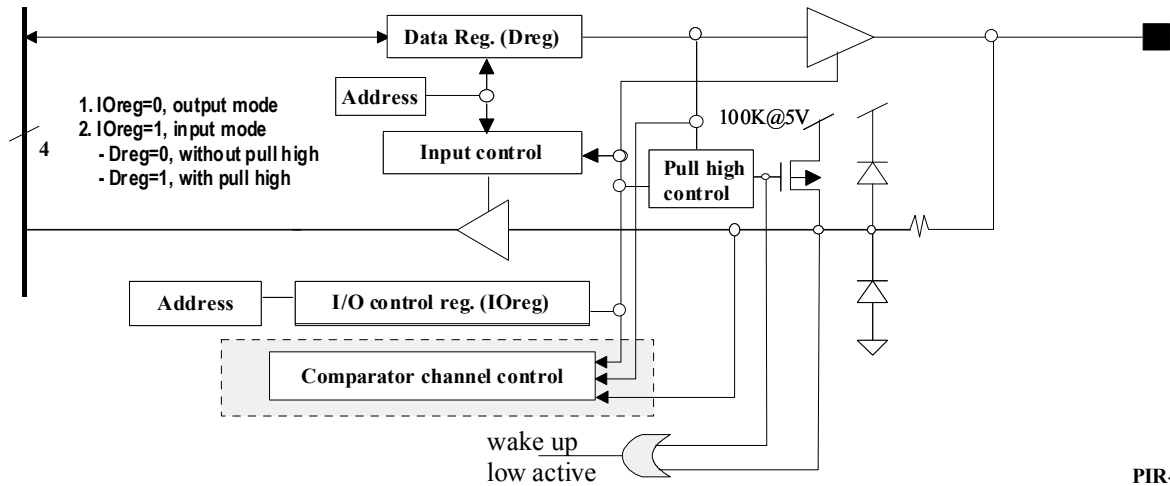
RF0/RF1：控制 interrupt 的 trigger 方式。

RF1	RF0	Trigger
0	0	falling edge
0	1	rising edge
1	0	falling & rising edge
1	1	falling & rising edge



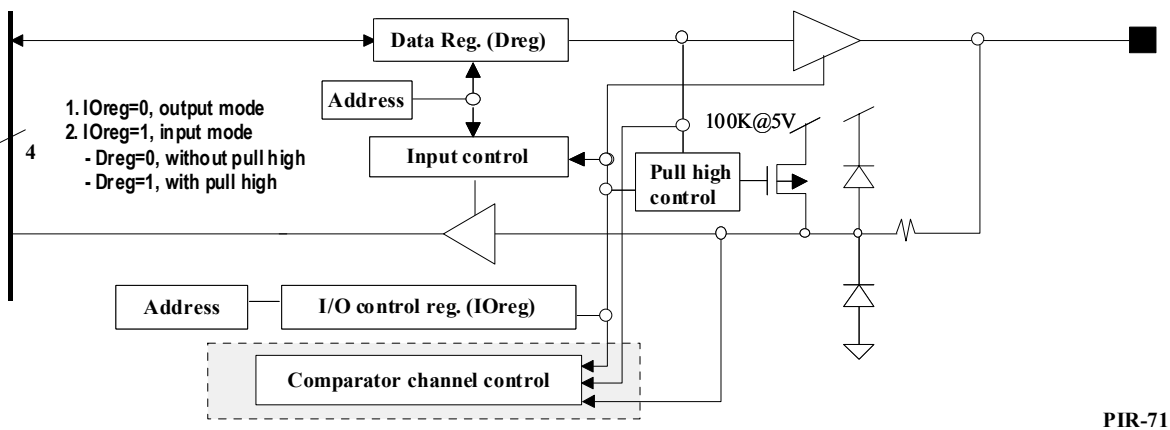
PA1/PA2/PA3：為 I/O port data (Dreg)，Power on 為 high，功能詳述如下。

1. 為 input mode 時，(Dreg) 可以控制是否有 pull high function。
  - (Dreg) 為 high 時，有 pull high function 和 wake up function，read (PA) 是 PAD 值。
  - (Dreg) 為 low 時，沒有 pull high function 且為 Comparator 的 input，read (PA) 是一直為 high。
2. 為 output mode 時，(Dreg) 即 PAD 輸出值，read (PA) 是 (Dreg) 值。



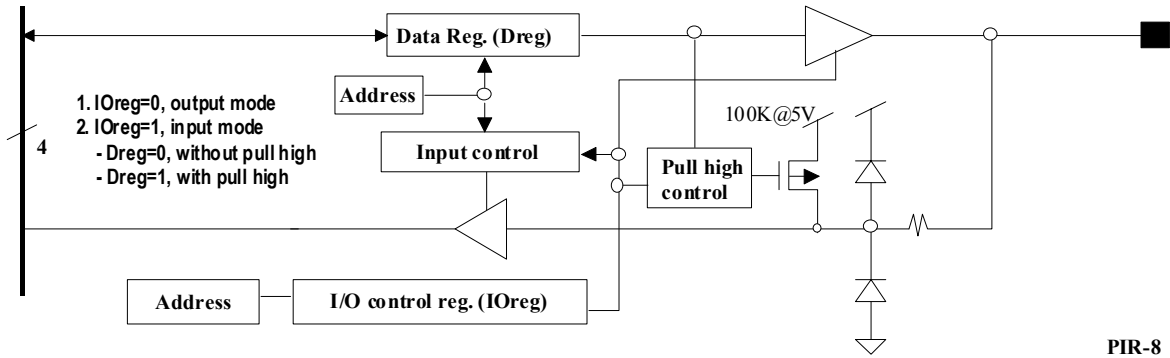
PB0/PB1/PB2：為 I/O port data (Dreg)，Power on 為 high，功能詳述如下。

1. 為 input mode 時，(Dreg) 可以控制是否有 pull high function。
  - (Dreg) 為 high 時，有 pull high function，read (PB) 是 PAD 值。
  - (Dreg) 為 low 時，沒有 pull high function 且為 Comparator 的 input，read (PB) 是一直為 high。
2. 為 output mode 時，(Dreg) 即 PAD 輸出值，read (PB) 是 (Dreg) 值。



PB3：為 I/O port data (Dreg)，Power on 為 high，功能詳述如下。

1. 為 input mode 時，(Dreg) 可以控制是否有 pull high function。
  - (Dreg) 為 high 時，有 pull high function，read (PB) 是 PAD 值。
  - (Dreg) 為 low 時，沒有 pull high function，read (PB) 是 PAD 值。
2. 為 output mode 時，(Dreg) 即 PAD 輸出值，read (PB) 是 (Dreg) 值。



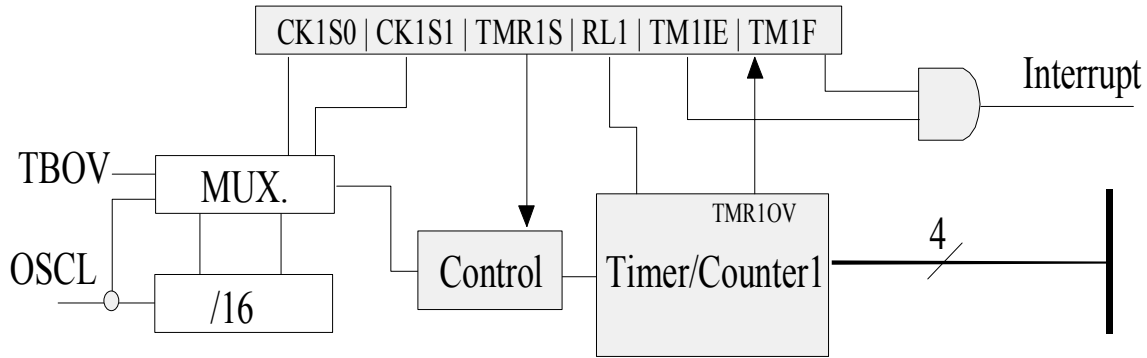
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## 8 Timer/Counter circuit & Pulse width measurement

Address	Register	Bit3	Bit2	Bit1	Bit0	Initial state
009H	INTF	CPF	TM1F	ADF	TBF	0000
		R/W	R/W	R/W	R/W	
00AH	INTC	CPIE	TM1IE	ADIE	TBIE	0010
		R/W	R/W	R/W	R/W	
014H	TMR1L	TMR1_3	TMR1_2	TMR1_1	TMR1_0	0000
		R/W	R/W	R/W	R/W	
015H	TMR1H	TMR1_7	TMR1_6	TMR1_5	TMR1_4	0000
		R/W	R/W	R/W	R/W	
016H	TMC1	RL1	CK1S1	CK1S0	TMR1S	0000
		R/W	R/W	R/W	R/W	

TMR1L/ TMR1H：Timer/Counter data，Timer/Counter 的 data 可以 R/W。Overflow 時會 set interrupt flag (TM1F)

FLAG	FUNCTION
TMR1S/ TMR2S	Low : stop Timer/Counter High : start Timer/Counter
CK1S1/ CK1S0	CK1S1/ CK1S0) 00: select OSCL (CK1S1/ CK1S0) 01: select OSCL/4 (CK1S1/ CK1S0) 10: select OSCL/16 (CK1S1/ CK1S0) 11: select TBOV
TM1F	Low: normal state High: after overflow
TM1IE	low : disable interrupt function high : enable interrupt function
RL1	low : disable TIMER1 reload function high : enable TIMER1 reload function



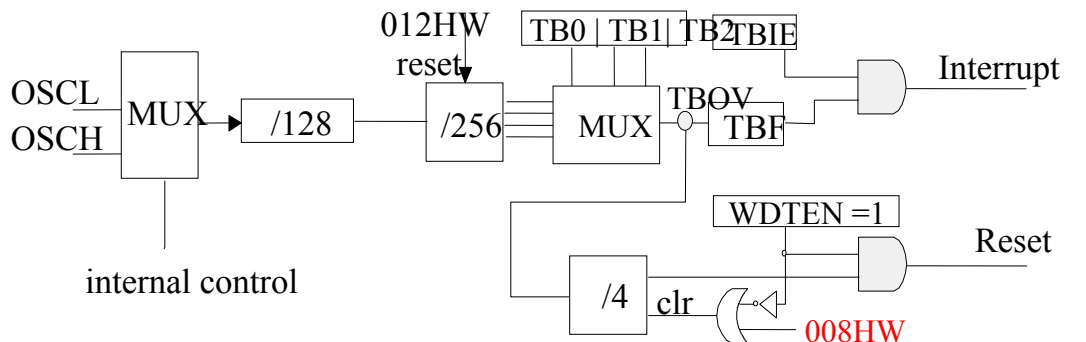
PIR-42

## 9 Time Base Timer / Watch Dog Timer cleared

Address	Resister	Bit3	Bit2	Bit1	Bit0	Initial state
009H	INTF	CPF	TM1F	ADF	TBF	0000
		R/W	R/W	R/W	R/W	
00AH	INTC	CPIE	TM1IE	ADIE	TBIE	0010
		R/W	R/W	R/W	R/W	
012H	TB	x	TB2	TB1	TB0	u000
		x	R/W	R/W	R/W	

After write 012H then clear time base counter .

TB2	TB1	TB0	O/P@16K
0	0	0	64HZ
0	0	1	32HZ
0	1	0	16HZ
0	1	1	8HZ
1	0	0	4HZ
1	0	1	2HZ
1	1	0	1HZ
1	1	1	0.5HZ



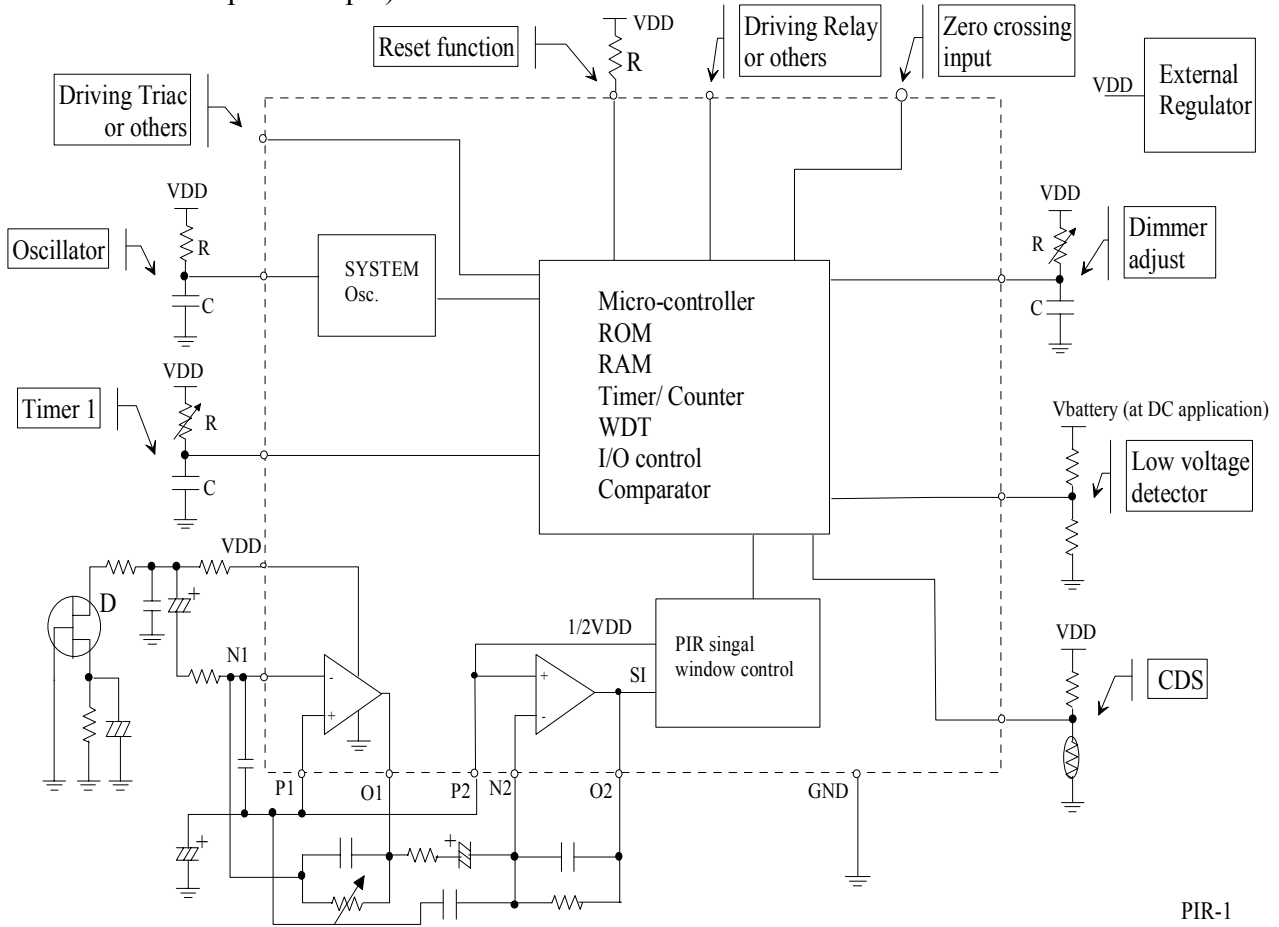
PIR-F1

注意：若有使用 Time base timer 功能，在 power on 後和每次在 Stop mode wake-up 起來之後，一定要先下“read 008H”的動作，否則其頻率會不準確。

Write 008H 可以 clear WDT counter .

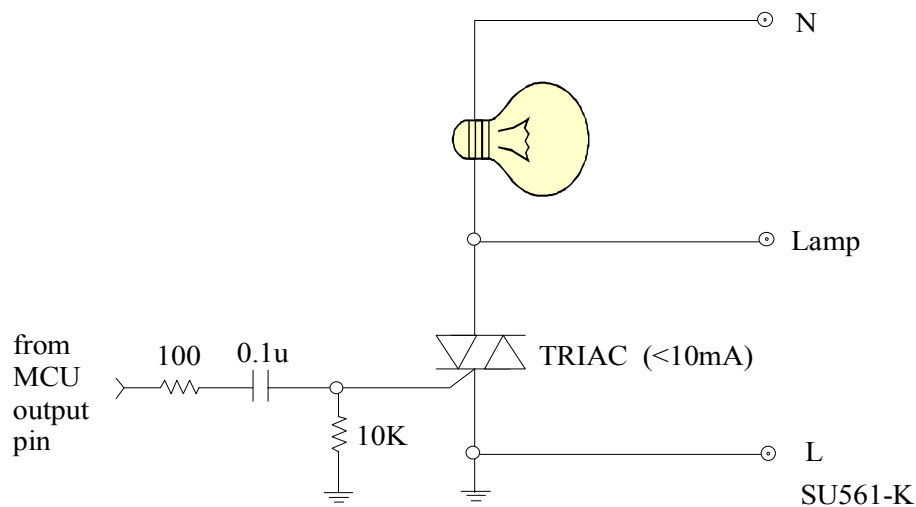
## . Application Circuit

(For PIR sensor D-input example)



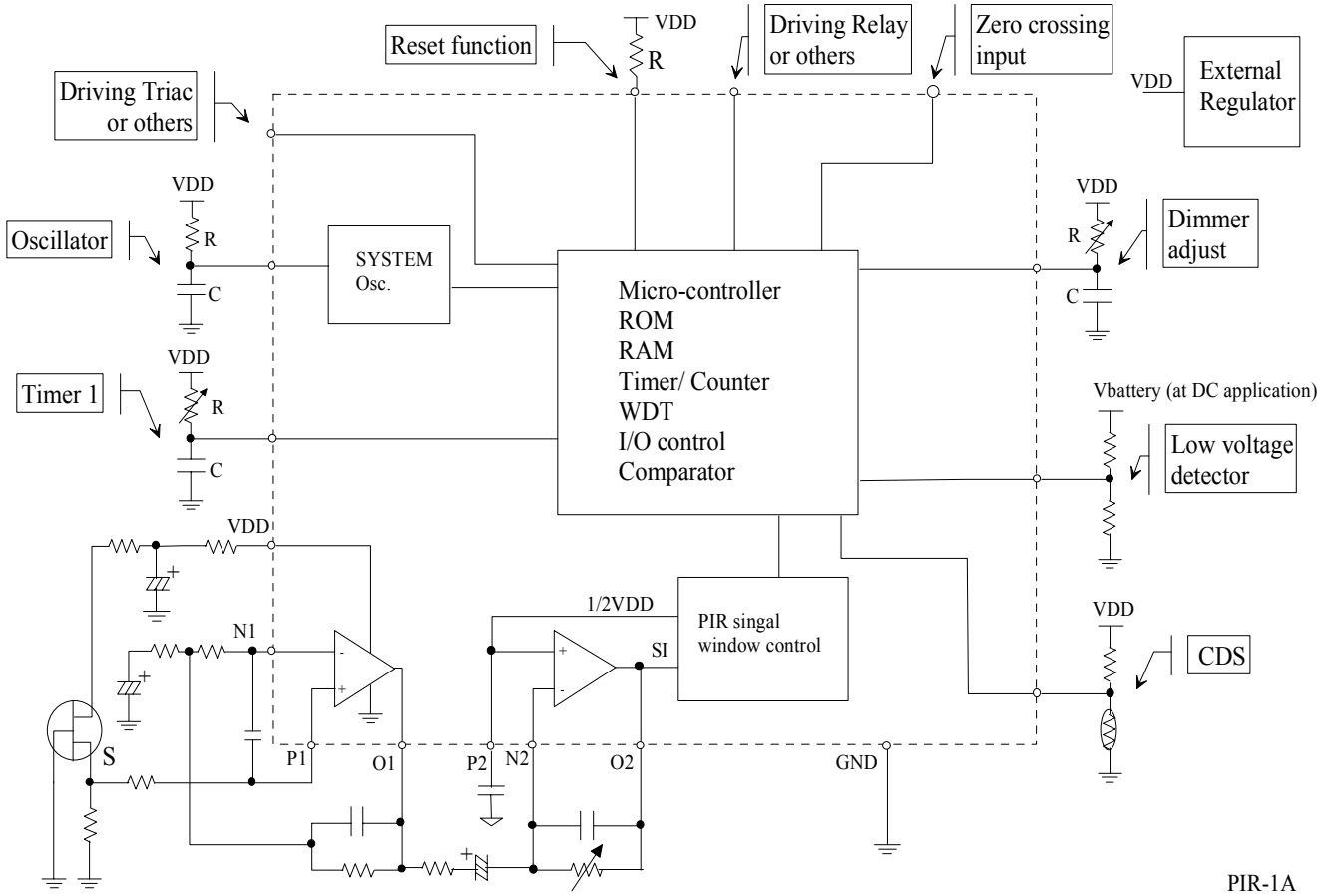
PIR-1

(Example circuit of driving TRIAC)



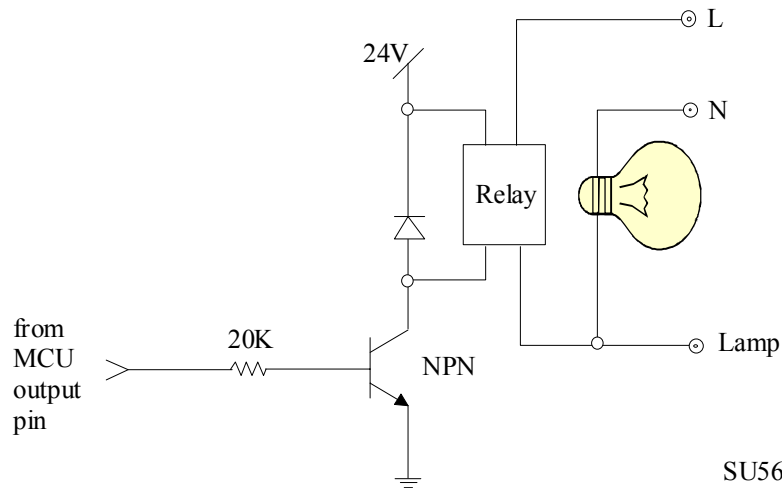
(Note : You can change 0.1u capacitor for difference TRIAC)

(For PIR sensor S-input example)



PIR-1A

(Example circuit of driving RELAY)



SU561-K1

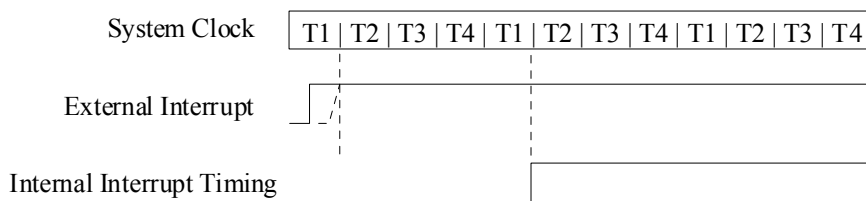
## . Mask Option Table

Function	Option	TTU561	TTR561
Operating voltage	<input type="checkbox"/> 3V(using low power consumption operation amplifier) 。 <input type="checkbox"/> 5V 。	mask	mask
Operation amplifier bias select (when VDD=5V)	<input type="checkbox"/> Don't care (if using AC power) 。 <input type="checkbox"/> Low power consumption 。	mask	mask

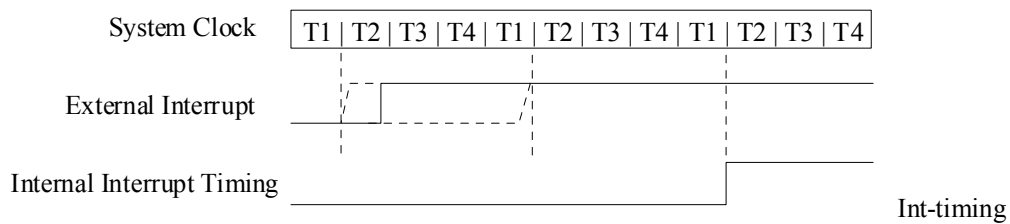
## . Application Note

1. Interrupt flag 只能被 software clear(write “0”), 而不能被 software set(write “1”)。
2. 進入 interrupt 的時機，會決定是否要執行完下一個 PC counter(PC+1) 的指令後，才進入副程式，或是執行完目前指令後，就進入副程式，其狀況有二，如下：

CASE A :



CASE B :



## . Order Information

	Project Number Name	
Package form	TTR561	TTU561
Chip form	不支援	TCU561
Wafer base	TDR561	TDU561



. Package Information

(18-DIP)

SYMBOLS	MIN.	NOR.	MAX.
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.880	0.900	0.920
E	0.300 BSC.		
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e <sub>B</sub>	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:  
 1. JEDEC OUTLINE : MS-001 AC  
 2. "D", "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.  
 3. e<sub>B</sub> IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.  
 4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.  
 5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.  
 6. DATUM PLANE  $\square$  COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

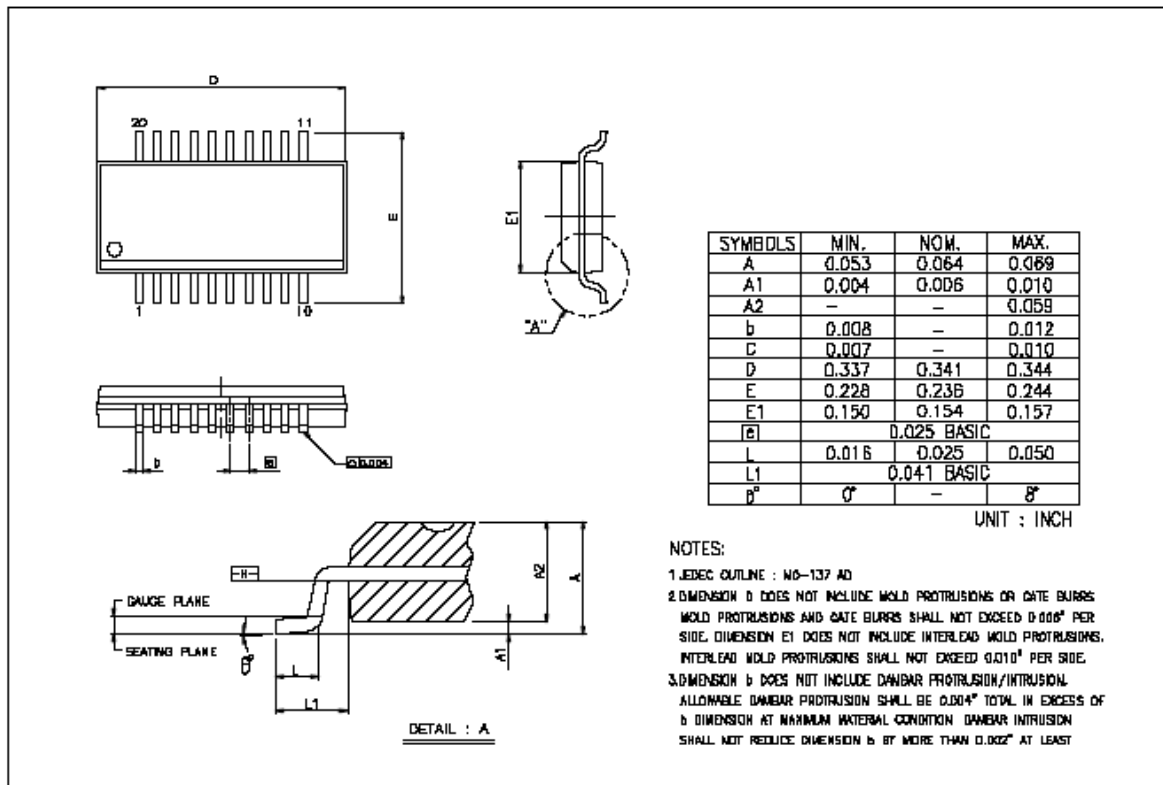
(20-SOP)

SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.496	0.508
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:  
 1. JEDEC OUTLINE : MS-013 AC  
 2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.  
 3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

(20-SSOP)



## Revise History

1. 2004/11/04
  - 新建立
2. 2005/03/15
  - 修正 014H/ 015H/ 016H 位址定義
  - 修正 PORT B 的 register
3. 2005/08/10
  - 拿掉 Preliminary 字眼
4. 2005/08/11
  - 增加 ESD 規格 (page 5)
  - 增加 Package soldering 規格 (page 5)
  - 增加 AVSS/AVDD 說明 (PIN DESCRIPTION)
  - 修改 Page 5 中 supply voltage
5. 2006/8/25
  - 修改 Page12, 13,21 WDTEN
  - 增加 20-SSOP 包裝資料 (page 26)
6. 2006/10/30
  - 增加 Page4 Pin Assignment 20SSOP 字樣
7. 2006/12/4
  - PA1 不能當 analog pin. 修改 page4, 16, 17.