Preliminary

TTR01D (IR remote 2K MCU)

§ General Description:

TTR01D MCU is an easy-used 4-bit CPU base microcontroller. It contains 2K-word ROM、64-nibble RAM、timer/Counter、interrupt service 、IO control hardware、 carrier generation timer which is especially designed for infrared remote appliance.

§ Features:

1. Tontek RISC 4-bit CPU core
2. MTP structure
   .2Kx16 ROM x1
   .1Kx16 ROM x2
3. Total 26 crucial instructions and two addressing mode
4. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
5. advance CMOS process
6. Working memory with 2K*16 program ROM and 64*4 SRAM
7. 2-level stacks
8. Operating voltage: 1.8V~3.6V for built-in oscillator
9. System operating frequency: (at VDD=3V) select by option
   . High speed system oscillator (OSCH):
   - ✧ Built-in RC oscillator: 3.64MHz ± 2%(PVT)
   - ✧ Resonator mode: 4MHz~455KHz
10. Offers 17 general open drain I/O or input pins
    - ✧ 8 input port with wakeup function and one of them shared with oscillator pin
    - ✧ 6 open drain IO port
    - ✧ 2 open drain IO port with CMOS(weak PMOS)/NMOS output option
    - ✧ 1 CMOS IO port shared with oscillator pin
    - ✧ Offering typical 450mA output driver directly drive IR LED
11. Two auto-reload timer/counter
    - ✧ Special 8- bit timer for carrier generation(duty & frequency)
    - ✧ Standard 12-bit timer offers interrupt request
12. MCU system protection:
    - ✧ Built-in watch dog timer (WDT) circuit

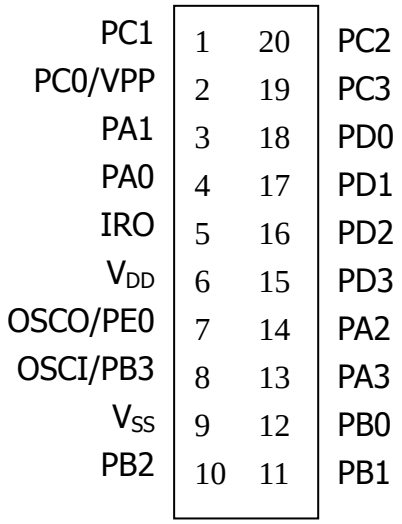
- ✧ Low voltage Reset(LVR)

13. Provides 2 interrupt sources
    - ✧ Internal: Timer/counter A & B
14. Provide package types
    - ✧ SOP 20 pins
    - ✧ Dice available

§ Applications:

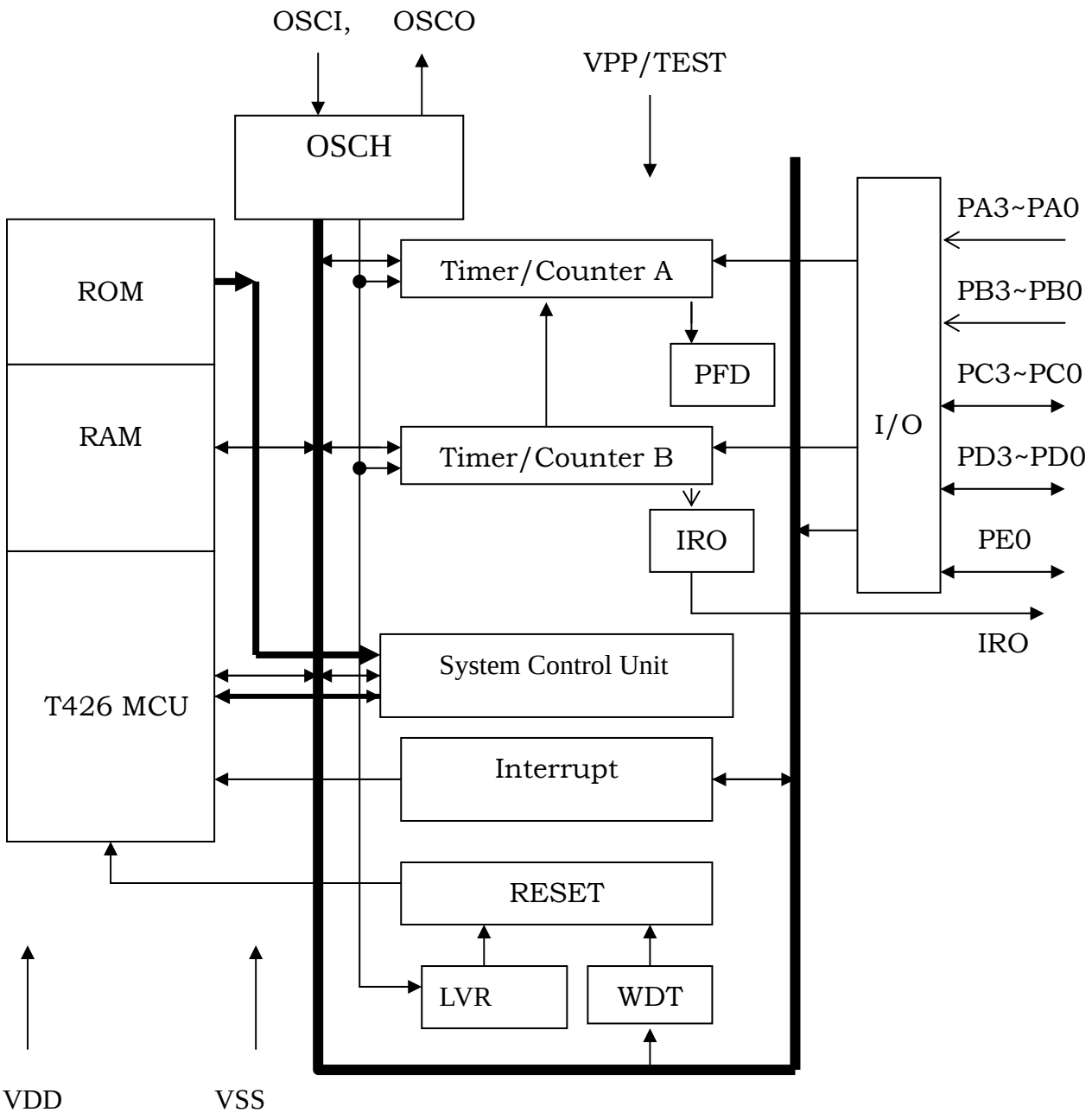
1. Infrared remote control transmitter
2. AV & household electrical appliance
3. Serial programming retail remote control

§ Package type:



20-SOP-A

§ Block Diagram:



§ Pin Description:

Pin Name	Share Pin	I/O	Pin no.	Mask Option	Pin Description
PA0~PA3		I	+4		Input port PA
V_{SS}		Power	+1		Negative power supply, ground
IRO		O	+1		IRO output
V_{DD}		Power	+1		Positive power supply
V_{SS}		Power	+1		Negative power supply, ground
PE0/OSCO		IO	+1		CMOS IO port shared with OSCO
PD0~PD1		IO	+2		Open drain type IO port
PD2~PD3		IO	+2		Open drain type IO port with mask option weak PMOS
PC0		IO	+1		PC0 shares pad with VPP pin Open drain type IO port
PC1~PC3		IO	+3		Open drain type IO port
PB0~PB2		I	+4		Input port
PB3/OSCI		I	+1		Input port shared with OSCI

§ IO Cell type Description:

Pin Name	I/O Type	Description
PA0~PA3,PB0~PB2	Figure IO-E	Input Port
PB3	Figure IO-H	Input Port shared with OSCI
PC0~PC3,PD0~PD1	Figure IO-F	STD open drain IO Port
PD2~PD3	Figure IO-F	STD open drain IO Port with weak PMOS
PE0	Figure IO-I	STD IO Port share with OSCO
IRO	Figure IO-G	STD Output Port

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-20℃ ~ +70℃	℃
Storage Temperature	Tst	-50℃ ~ +125℃	℃
Supply Voltage	VDD	VSS-0.3 ~VSS+3.6	V
OTP Supply Voltage	VPP	VSS-0.3 ~ VSS+7.5	V
Input Voltage	Vin	VSS -0.3 to VDD+0.3	V
Human Body Mode	ESD	>3	KV
Note: VSS symbolizes for system ground			

Preliminary

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	F_{OSCH}=3.64MHz	1.8	-	3.6	V
Operating Current (Normal Mode, CPU working, I/O no load)	I_{nd}	VDD=3.0V, no load, F_{OSCH}=3.64MHz,	-	1.0	3.0	mA
Standby Current	Istb	I/O no load, F_{OSCH} stop	-	-	1.0	uA
PA,PB,PC,PD,PE	V_{IL}	Input Low Voltage	0	-	0.2	VDD
PA,PB,PC,PD,PE	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
PC0 Sink Current	I_{OL0}	VDD=3.0V, Vol=0.3V	1	2	-	mA
PC1~3,PD,PE Sink Current	I_{OL1}	VDD=3.0V, Vol=0.3V	4	6	-	mA
IRO Sink Current(NMOS)	I_{OL2}	V_{DD}=3V, V_{OL}=0.6V	-	450	-	mA
IRO Sink Current(CMOS)	I_{OL3}	V_{DD}=3V, V_{OL}=0.6V	4	6	-	mA
IRO Source Current(CMOS)	I_{OH0}	VDD=3.0V, Voh=2.7V	1	1.5	-	mA
PD2,PD3 output source current	I_{OH1}	VDD=3.0V, Voh=-0.0V	10	-	30	uA
PE0 output source current	I_{OH2}	VDD=3.0V, Voh=2.7V	4	5	-	mA
PA,PB pull-high Resistor	R_{PH}	VDD=3.0V	50	100	150	KΩ
Oscillator Start up voltage	V_{ST}	F_{OSC}=3.64M	1.6	-	1.8	V
Oscillator Sustain voltage	V_{SU}	F_{OSC}=3.64M	1.3	-	1.5	V
Low Voltage reset voltage	V_{LVR}			1.6		V

§ AC Characteristics:

Parameter	Test Condition	Min	Typ.	Max	Unit
System Oscillator Frequency	VDD=1.8V~3.6V, TA=0°C~60°C Built in RC oscillator mode	3.5672	3.64	3.7128	MHz
System Stable Time after Power up	Built in RC oscillator mode (RC_{cycle}=1/built in RC frequency=1/3.64MHz)	32*RC_{cycle}	32*RC_{cycle}	32*RC_{cycle}	s
	Resonator mode (OSC_{cycle}=1/Resonator frequency)	32*RC_{cycle}+ 256*OSC_{cycle}	32*RC_{cycle}+ 256*OSC_{cycle}	32*RC_{cycle}+ 256*OSC_{cycle}	s

§ Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~$7FF_H$		Program ROM [2K*16]
	000_H ~ 007_H	File Registers
	008_H~$01F_H$	Peripheral registers (I)
	020_H~$05F_H$	Working RAM [64*4]

§ Interrupt Vectors:

Interrupt Vectors	Function Description
$000	hardware RESETB
$001	Hardware IRQB /Soft IRQB

§ File registers:

Address	Symbol	R/W	Default	Description
000_H	(DP1)	R/W	-	Indirect addressing register
001_H	ACC	R/W	-	Accumulator & Read Table 1st data
002_H	TB1	R/W	-	Read Table 2nd data
003_H	TB2	R/W	-	Read Table 3rd data
004_H	TB3	R/W	-	Read Table 4th data
005_H	DPL	R/W	-	Data Pointer low nibble
006_H	DPM	R/W	-	Data Pointer middle nibble
007_H	DPH	R/W	-	Data Pointer high nibble

§ Peripheral registers: Interrupt request flag register

Address	Symbol	R/W	Default	Description
008_H	PS	R/W	1110	CPU power saving control register
009_H	INTC	R/W	0000	Interrupt enable control register
$00A_H$	INTF	R/W	0000	Interrupt request flag register
$00B_H$	TCPAC	W	----	TCPA Timer/counter A control register
$00C_H$	TCPAL	W	0000	TCPA Timer/counter A data low register
$00D_H$	TCPAM	W	0000	TCPA Timer/counter A data middle register
$00E_H$	TCPAH	W	0000	TCPA Timer/counter A data high register
$00F_H$	PA	R	----	I/O port A data register
010_H	PB	R	----	I/O port B data register
011_H	PC	R/W	0000	I/O port C data register
012_H	PD	R/W	0000	I/O port D data register
013_H	TCPBC	W	----	TCPB Timer/counter B control register
014_H	TCPBLL	W	0000	TCPB Timer/counter B low data low nibble register
015_H	TCPBLH	W	0000	TCPB Timer/counter B low data high nibble register
016_H	TCPBHL	W	0000	TCPB Timer/counter B high data low nibble register
017_H	TCPBHH	W	0000	TCPB Timer/counter B high data high nibble register
018_H	PSP	R/W	---0	Peripheral power saving control register
019_H	PE	R/W	---0	I/O port E data register
$01A_H$	PEC	R/W	---0	I/O port E control register

Note: a. Default means initial value after power on or reset.
b. R is “read” only, W is “write” only, R/W is both of “read” & “write”.

§ System function description:

1. System Oscillators

The high speed oscillator can only be operated in built-in mode.

2. CPU clock

The CPU clock comes from system oscillator. In the normal operation, the system clock comes from high speed system oscillator (OSCH).

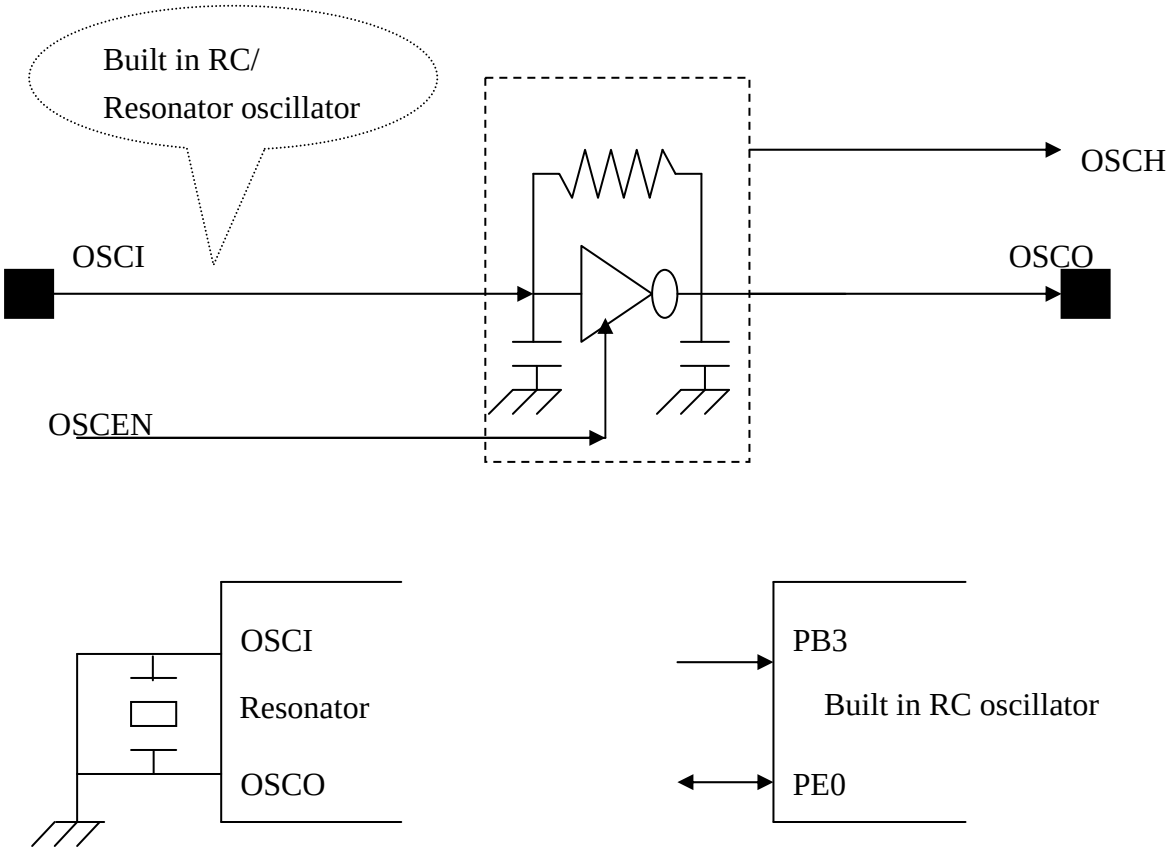


Figure: High Speed System Oscillator(OSCH)

3. Power saving mode (Stop mode)

The CPU enters stop mode is operated by writing CPU power saving register (PS). During the power saving mode, CPU holds the internal status of the system. In stop mode, the oscillator clocks will be stopped and system need a warm-up time for the stability of system clock running after wake up. As system wake up from stop mode will cause a CPU reset. Software program will restart from reset vector.

4. MCU System Operation Modes

The MCU has 2 operating modes, including high speed operation, stop modes. After power on reset, the MCU will go into high speed operation mode automatically. After wake up from stop mode, the MCU will resume the last operation mode.

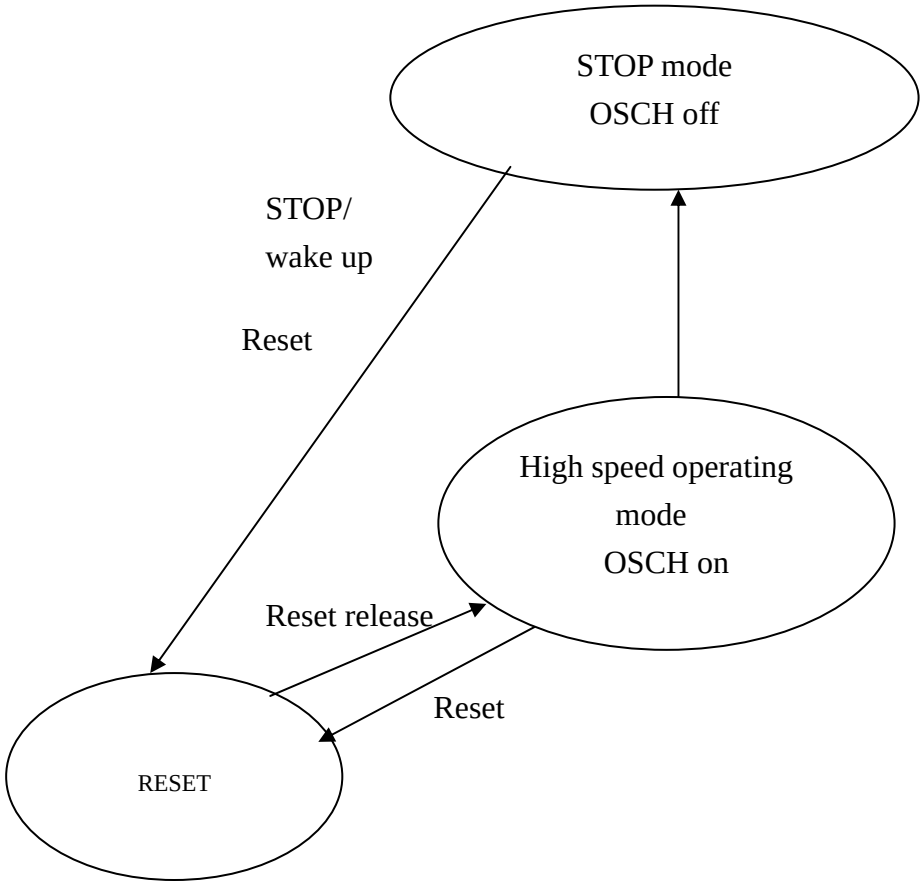


Figure: System Operation State Diagram

✧ Power saving mode condition & Release

Modes	Stop mode
Oscillator	**Stopped**
CPU internal status	Program counter, stack, flag register reset
Program counter	Reset as $0000
Peripherals: Timers, Interrupts, Register, I/O PC & PD **I/O PE**	Stopped & Retain Output data cleared(PD2 & PD3 depend on PD2_R & PD3_R) Stopped & Retain
Watch Dog Timer	Disable & cleared
Release Condition	Reset, Input wake-up

✧ PS: Power saving register [R/W] , default value [1110]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PD3_R	PD2_R	SELIR	STOP
Read/write	R/W	R/W	R/W	R/W

STOP: Into stop mode. (0: inactive; 1: active)

SELIR: IRO output active level (0: CMOS external transistor; 1: NMOS built-in transistor)

PD2_R: PD3 clear mode (0: not clear when CPU stop; 1: clear when CPU stop)

PD3_R: PD3 clear mode (0: not clear when CPU stop; 1: clear when CPU stop)

✧ PSP: Peripheral power saving register [R/W] , default value [---0]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	IROEN
Read/write	-	-	-	R/W

IROEN: IRO output enable (0: disable; 1: enable)

The system oscillator generates the system control timing for CPU core or peripheral devices with fixed control phase, so the waveform of oscillator becomes sensitive to noise, abnormal duty especially fatal for CPU. Any switching of clock source needs oscillation stable time (OST) to make sure the oscillation is stable and synchronized with CPU timing phase. The OST is 32's RC clocks at built-in RC oscillator and 32's RC clocks plus 256's OSCH clocks at resonator mode.

5 .Interrupts

The CPU provides only 1 interrupt vector ($001H) and no priority, but can expand to multi-sources. Interrupt source includes two timer/counter interrupts (TCPAINT &TCPBINT). The interrupt control registers (INTC) contain the interrupt control bits to enable and disable corresponding interrupt request and the corresponding interrupt request flags in the (INTF) registers. Before finishing the INT service routine, another INT request will keep waiting until program return from interrupt routine.

✧ INTC: Interrupt control register [R/W], default value [--00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	TCPBIE	TCPAIE
Read/Write	-	-	R/W	R/W

TCPAIE: Enable interrupt of timer/counter A. (0: disable; 1: enable)

TCPBIE: Enable interrupt of timer/counter B. (0: disable; 1: enable)

✧ INTF: Interrupt request flag register [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	TCPBF	TCPAF
Read/Write	-	-	R/W	R/W

TCPAF: Timer/counter A' interrupt request flag. (0: inactive; 1: active)

TCPBF: Timer/counter B' interrupt request flag. (0: inactive; 1: active)

If the interrupt request needs service, the programmer may set the corresponding INT enable bit to allow interrupt active. The internal timer/counter interrupt is setting the TCPxF to 1, resulting from the timer/counter overflow.

When the corresponding interrupt enable and flag bits is set to 1, the CPU will active the interrupt service routine. Then CPU reads the service flag and check the request priority then proceeds with the relative interrupt service. After CPU writes the corresponding bits to 0 in the INTF register, the service flag will be cleared to 0(using STX #n, $m instruction). The INTF registers' bit can only write "0" to clear the flag. User writes "1" to Flag bit with no effect.

6. Watch Dog Timer (WDT)

The clock of watch dog timer comes from timer A' PFD. User can use the time up signal to prevent a software malfunction or abnormal sequence from jumping to an unknown memory location causing a system fatal failure. Normally, if the watchdog timer time up signal active that will reset the chip. At the same time, program and hardware can be initialized and resume system under normal operation. The chip also provides 2 steps clear watchdog command as the programmer writes INTF with $F data first that will enable the WDT clear, and then writes the power saving (PS) control register after. Completely finishes the two write steps will clear the watch dog timer. User should well arrange the two command steps for avoiding the dead lock loop. *User should keep in minds that always reset WDT at main program and never clear the WDT in the interrupt routine.*

The max period of WDT =(TPCAOV cycle time *2) * 8

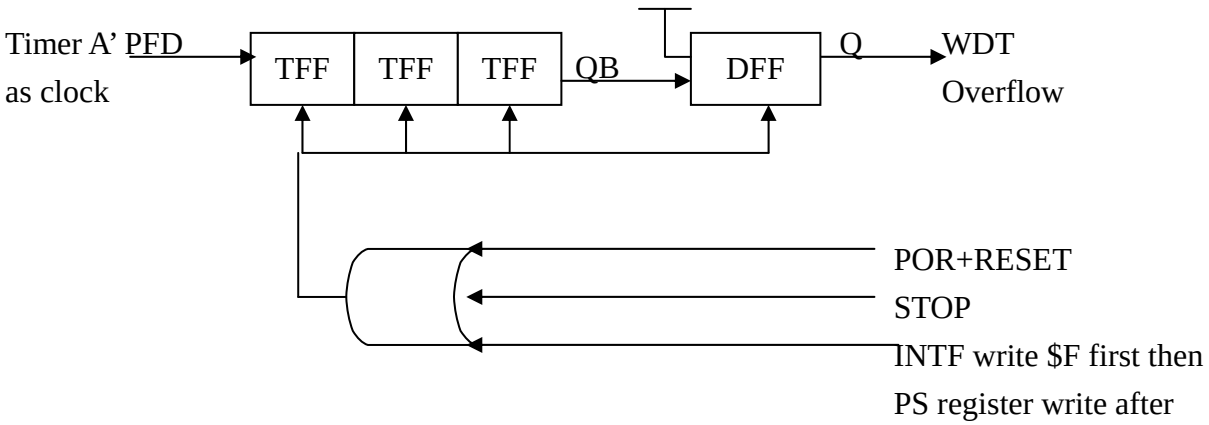


Figure: Watch Dog Timer control circuit

7. RESET

The chip has three kinds of reset sources: POR (power on reset), Watch dog timer reset, LVR (low voltage reset). The reset feature can be divided into 2 kind groups that one is system reset and the other is CPU reset. The system reset will initialize the CPU and peripheral device with default state. The CPU reset only initializes the CPU state and keeps the peripheral state no change.

S-7a System reset

.POR (power on reset)

The chip provides automatic reset function when the power is turned on. The VDD should be below 1.4V and its rising slope (from 0.1VDD up to o.9VDD) needs less than 10ms.

S-7b CPU reset

.Watch Dog Timer Reset

The reset signal will generate automatically when the watchdog timer runs overflow. If the watchdog timer is cleared regularly by user's program, no watchdog reset will occur. Unless the MCU is forced into abnormal state, the software controlled procedure is disrupted and causing watch dog timer overflow, then it will generate reset signal to initializes the chip returning to normal operation.

. **LVR (low voltage reset)**

The LVR is a low system voltage detector. As the operating voltage falls below the detected window then the system reset will start the system reset procedure.

LVR	System RESET	Detected Vop
0→1	active	1.2V~1.6V
1→0	disable	>1.6V

For OTP type, hardware needs to down load the mask options into register and the events are caused by power on reset, watch dog overflow reset and LVR reset.

§ Peripheral function description:

1. 8 bits Carrier Timer (TCP) for TCPB

One 8-bits timer (TCPB) with system clock source and preload data buffer can implement as a timer, IRO is programmable frequency divider can support IR carrier generator. TCPBOV is the timer overflow signal and the rising edge will set the relative INT flag.

✧ TCPBC: Timer control register [W], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	-
Read/Write	-	-	-	-

As writing the TCPBC address, the timer will reload the low latch data into counter that means IRCO will be initialized for choosing low latch data.

✧ TCPBLL: TCPB low nibble for low data register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPBL3	TCPBL2	TCPBL1	TCPBL0
Read/Write	W	W	W	W

TCPB3~TCPB0: TCPB low nibble of data buffer.

✧ TCPBLH: TCPB high nibble for low data register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPBL7	TCPBL6	TCPBL5	TCPBL4
Read/Write	W	W	W	W

TCPB7~TCPB4: TCPB high nibble of data buffer.

✧ TCPBHL: TCPB low nibble for high data register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPBH3	TCPBH2	TCPBH1	TCPBH0
Read/Write	W	W	W	W

TCPBH3~TCPBH0: TCPBH low nibble of data buffer.

✧ TCPBHH: TCPB high nibble for high data register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPBH7	TCPBH6	TCPBH5	TCPBH4
Read/Write	W	W	W	W

TCPBH7~TCPBH4: TCPBH high nibble of data buffer.

✧ TCPBL: Like a 8 bit TCPB low data register, default value [00H]

TCPBL	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPBL7	TCPBL6	TCPBL5	TCPBL4	TCPBL3	TCPBL2	TCPBL1	TCPBL0

✧ TCPBH: Like a 8 bit TCP high data register, default value [00H]

TCPBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPBH7	TCPBH6	TCPBH5	TCPBH4	TCPBH3	TCPBH2	TCPBH1	TCPBH0

.Timer

When TCPB works as a Timer, user needs give the preload data TCPBH (output high level)/TCPBL (output low level) for periodic waveform generation. After initial setting, user starts the TCPB counting by writing the TCPBC address, the TCPB cycle period is:

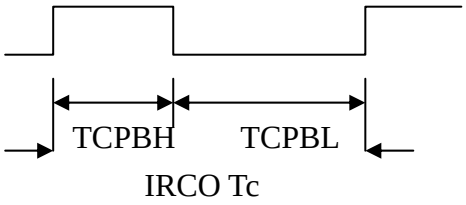
Tc = (selected clock cycle) * (TCPBH+TCBDL)

When user writes data to the TCPBH & TCPBL, the data just keep in TCPBL/H register. During writing the TPCBC address command executed, the TCPB 1's complement value will load the TCPBL into counter TCPB as initial value and start the timer function. TCPB run with reload feature as TCPB up counts and reaches the value of "FF_H" or 255. The next reload data is TCPBH for carrier high level. The procedure keeps alternately and Infrared carrier generation is easily implemented.

.IRO

The IRCO Mode includes in timer mode and the output frequency is:

IRCO frequency= OSCH / (TCPBH+TCPBL)



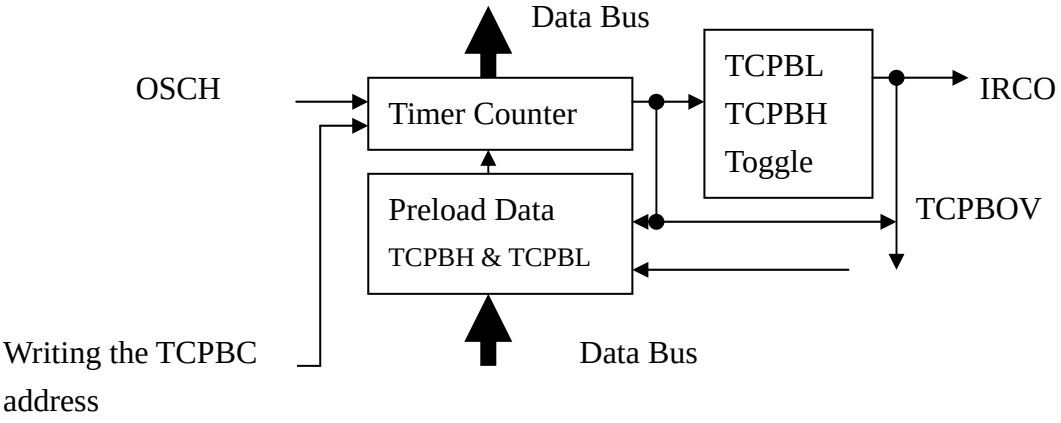


Figure: 8 bits Timer for IRCO

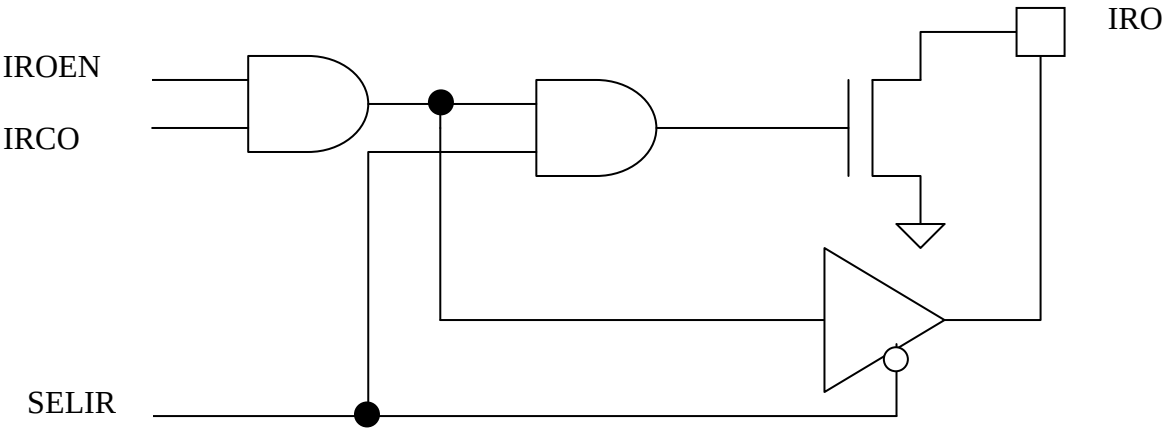


Figure: IRO type

2. 12 bits Timer/Counter (TCP) for TCPA

One 12-bits timer (TCPA) with IRCO clock source and preload data buffer can implement as a timer feature. TCPAOV is the timer overflow signal and the rising edge will set the relative INT flag.

✧ TCPAC: Timer/counter/PFD control register [W], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	-
Read/Write	-	-	-	-

As writing the TCPAC address, the timer will reload the latch data into counter.

✧ TCPAL: TCPA low nibble data register [W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPA3	TCPA2	TCPA1	TCPA0
Read/Write	W	W	W	W

TCPA3~TCPA0: TCPA low nibble of data buffer.

✧ TCPAM: TCPA middle nibble data register [W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPA7	TCPA6	TCPA5	TCPA4
Read/Write	W	W	W	W

TCPA7~TCPA4: TCPA middle nibble of data buffer.

✧ TCPAH: TCPA high nibble data register [W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPA11	TCPA10	TCPA9	TCPA8
Read/Write	W	W	W	W

TCPA11~TCPA8: TCPA high nibble of data buffer.

✧ TCPA: Like a 12 bit TCP data register [W], default value [000H]

Register	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPA11	TCPA10	TCPA9	TCPA8	TCPA7	TCPA6	TCPA5	TCPA4	TCPA3	TCPA2	TCPA1	TCPA0
Read/Write												

.Timer

When TCPA works as a Timer, user needs give the preload data TCPA for periodic interrupt. After initial setting, user starts the TCPA counting by writing the TCPAC adress, the TCPA cycle period is:

Tc = (IRCO frequency) * (TCPA)

When user writes data to the TCPA, the data just keep in TCPAL/H register. During writing the TCPAC address command executed, the TCPA 1's complement value will load into counter TCPA as initial value and start the timer function. TCPA run with reload feature as TCPA up counts and reaches the value of "FFF_H" or 4095. At the same time, interrupt request flag TCPAF will set activated, if software enables the corresponding interrupt enable bit, INT hardware will cause MCU interrupt service routine.

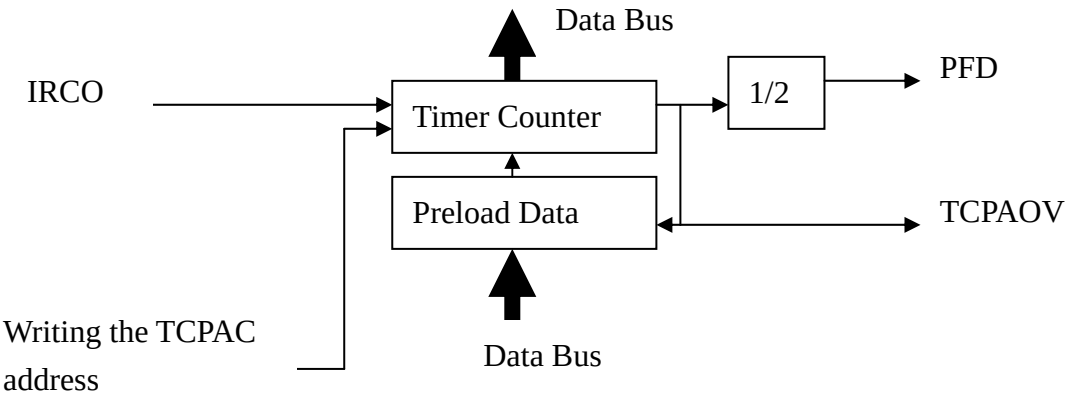


Figure: 12 bits Timer

. I/O File Register

✧ PA: Port A input port [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PA3	PA2	PA1	PA0
Read/Write	R	R	R	R

PA3~PA0: port A input port.

✧ PB: Port B input port [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PB3	PB2	PB1	PB0
Read/Write	R	R	R	R

PB3~PB0: port B input port.

✧ PC: Port C data register [R/W], default value [0000]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PC3	PC2	PC1	PC0
Read/Write	R/W	R/W	R/W	R/W

PC3~PC0: port C data register NMOS output only.

✧ PD: Port D data register [R/W], default value [0000]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PD3	PD2	PD1	PD0
Read/Write	R/W	R/W	R/W	R/W

PD3~PD0: port D data register.

PD1~PD0 NMOS output only

PD3~PD2 with weak PMOS (CMOS)/NMOS only select by mask option

✧ PE: Port E data register [R/W], default value [---0]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	-	-	-	PE0
Read/Write	-	-	-	R/W

PE0: port E data register CMOS output.

✧ PEC: Port E control register [R/W], default value [---0]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	-	-	-	PEC0
Read/Write	-	-	-	R/W

PEC0: port E control register.

Controlling I/O mode, when being high, is input mode.

. I/O PAD Cell Structure & Function Description

.. Input Port

The input port always has the pull high resistor and input data can read by port reading command. A wake-up function also offers the system wake up feature for keys or special external triggers.

Input Data	**Read Data**	**Wake-up**
0	**0**	**Active**
1	**1**	**Non-active**
Floating	**1**	**Non-active**

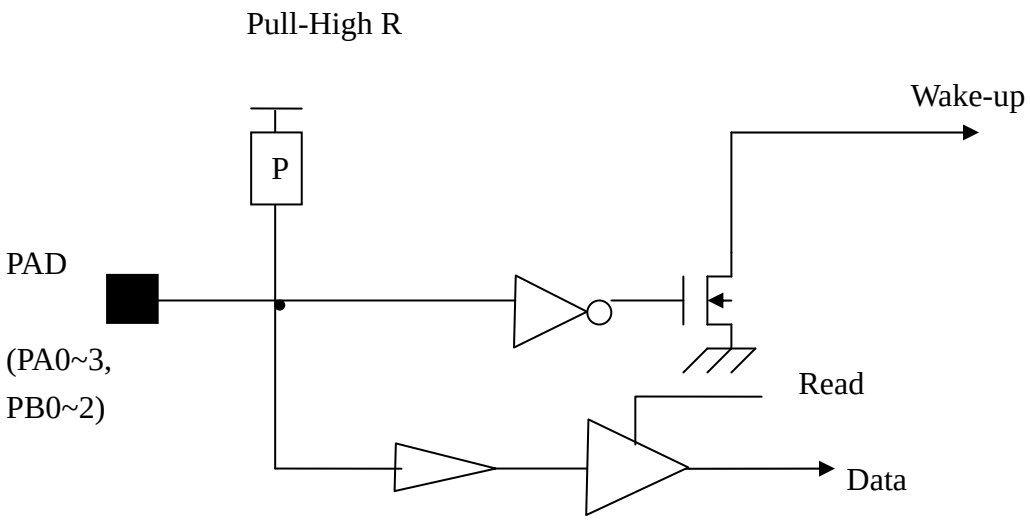


Figure IO-E: Input Port

.. Output Port

The output driver has drive capability for heavy load. The output enable option is a control signal for disable output feature and pad can release to use as input or another request.

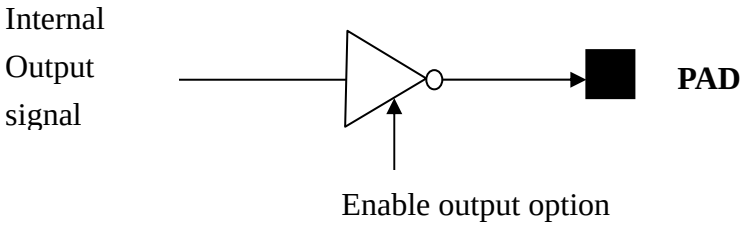


Figure IO-G: Output Driver Port

Internal signal Data	Output option enable	**PAD Data**
x	disable	**Floating**
0	enable	**0**
1	enable	**1**

.. Standard open drain IO Port

The standard open drain IO port has no I/O control register for switching input or output mode and use output data register to change the IO mode. If output data=1, the I/O port is programmed as input with pull-up resister or not dependant on CMOS type or NMOS type output.

Output Type	Output Register data	PAD data	**Pull-up**
CMOS	0	0	**No**
CMOS	1	Input mode	**Yes**
NMOS	0	0	**No**
NMOS	1	Input mode	**No**

Note: In the STOP mode IO port data register will be cleared that is for key scan with wake up feature.

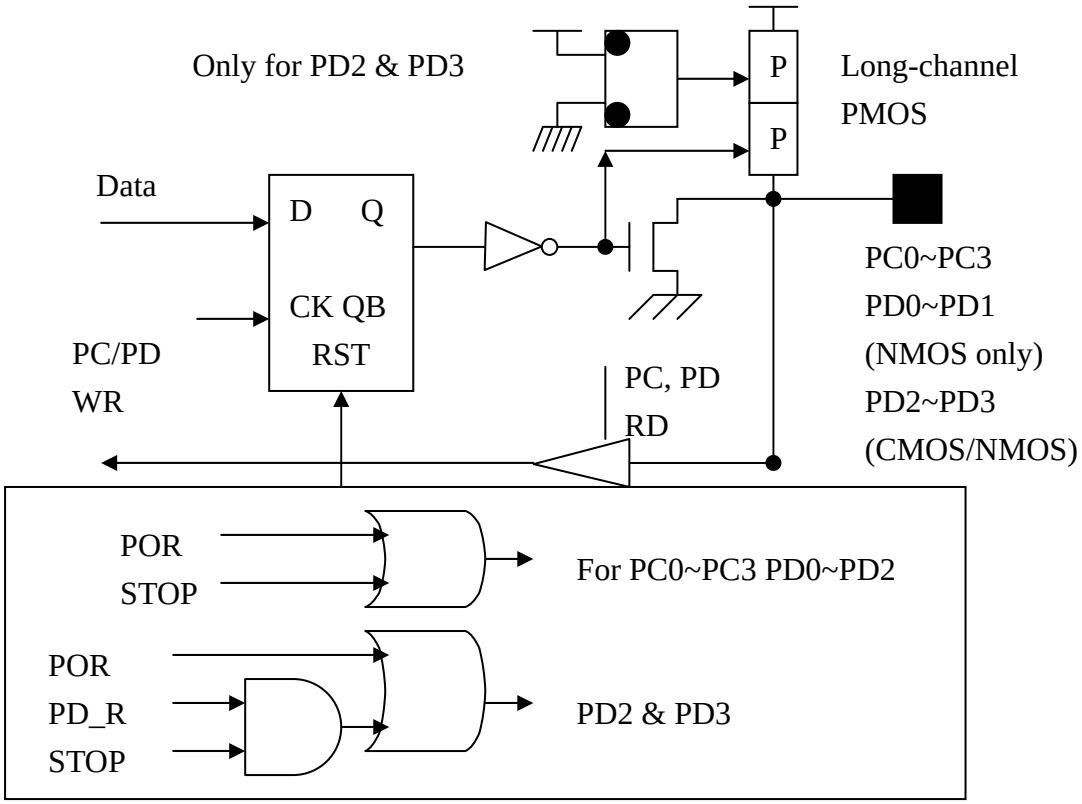


Figure IO-F: Standard open drain IO Port

.. Input Port shared with oscillator

The port can play a role of input port that has the pull high resistor and input data can read by port reading command. A wake-up function also offers the system wake up feature for keys or special external triggers. The port can also act as resonator oscillator input that does not have pull high resistor but input data reads always as high and can not wake up system.

Input Data	**Read Data**	**Wake-up**
0	**0**	**Active**
1	**1**	**Non-active**
Floating	**1**	**Non-active**
OSCI	**1**	**Non-active**

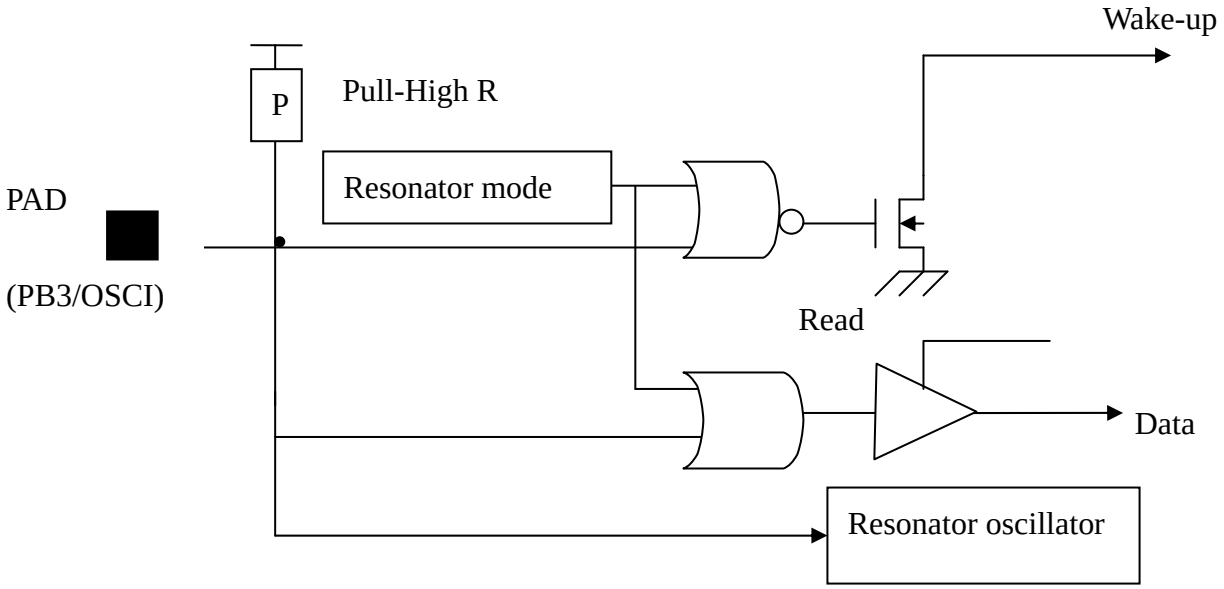


Figure IO-H: Input Port shared with oscillator

Standard IO Port shared with oscillator

The standard input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. When port plays a role as input, the read port data that is reading data comes from PAD input data. When it is as output, that port read the data register. The port can also act as resonator oscillator output that input data reads always as high when control data is high and can not output data.

I/O control DATA	Mode	PAD data
0	Output mode	Output Register data Q
1	Input mode	Input data
X	Resonator mode	OSCO

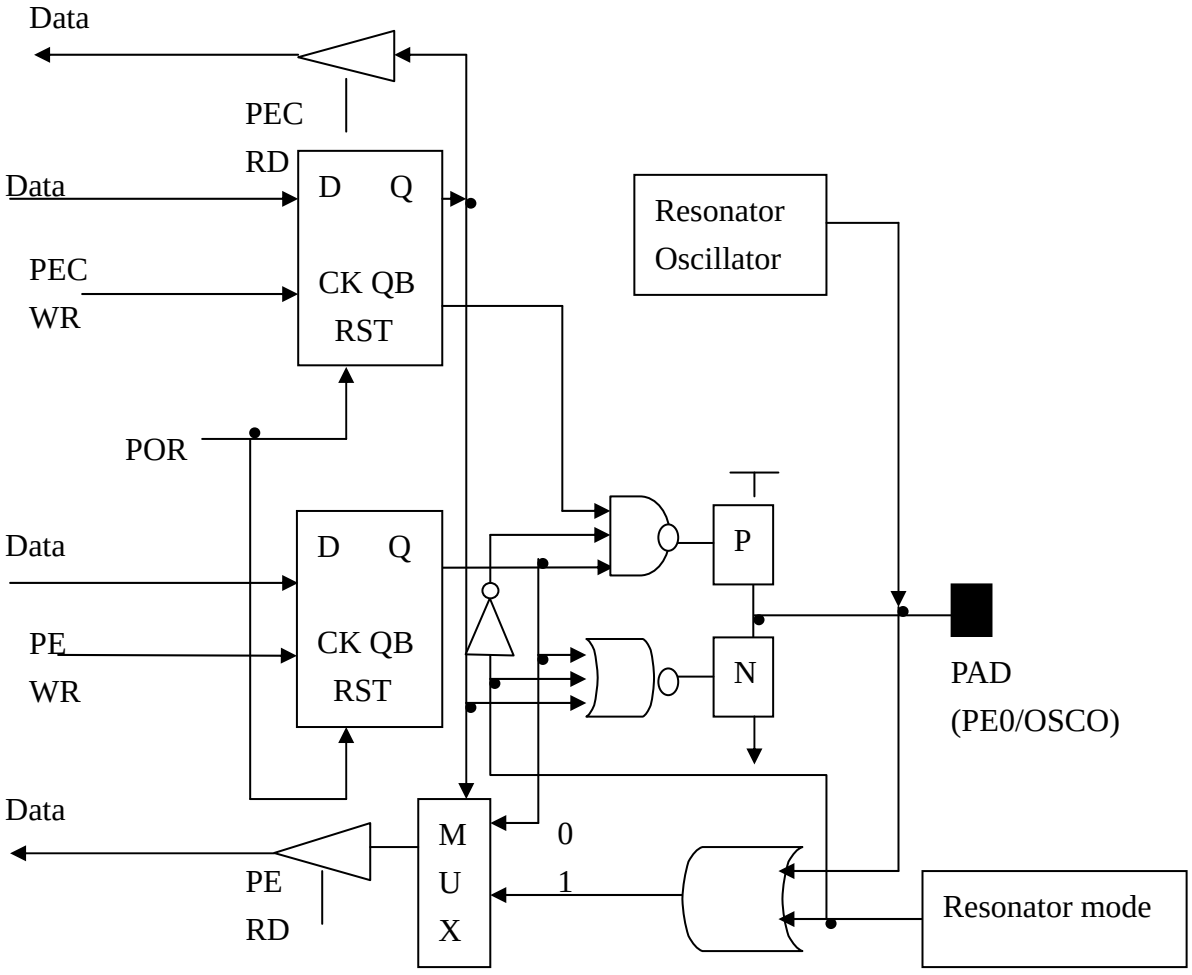


Figure IO-I: Standard IO Port share with oscillator

§ Mask Option Table:

The following table shows the mask option in this chip. All the mask options must define to ensure proper function.

Function	Option	
Oscillator mode	Built-in RC oscillator	Resonator
PD2 type	NMOS	CMOS
PD3 type	NMOS	CMOS
MTP type	2Kx16	1Kx16

MTP type: The standard Program ROM is all 2Kx16, but it can be program twice. First program, selects the MTP option as 2Kx16 and keep the page1 are all blank. Second program, selects the MTP option as 1Kx16, the program ROM size is only 1Kx16.

MTP: 2Kx16:

000	Page0
. .	
3FF	
400	Page1
. .	
7FF	

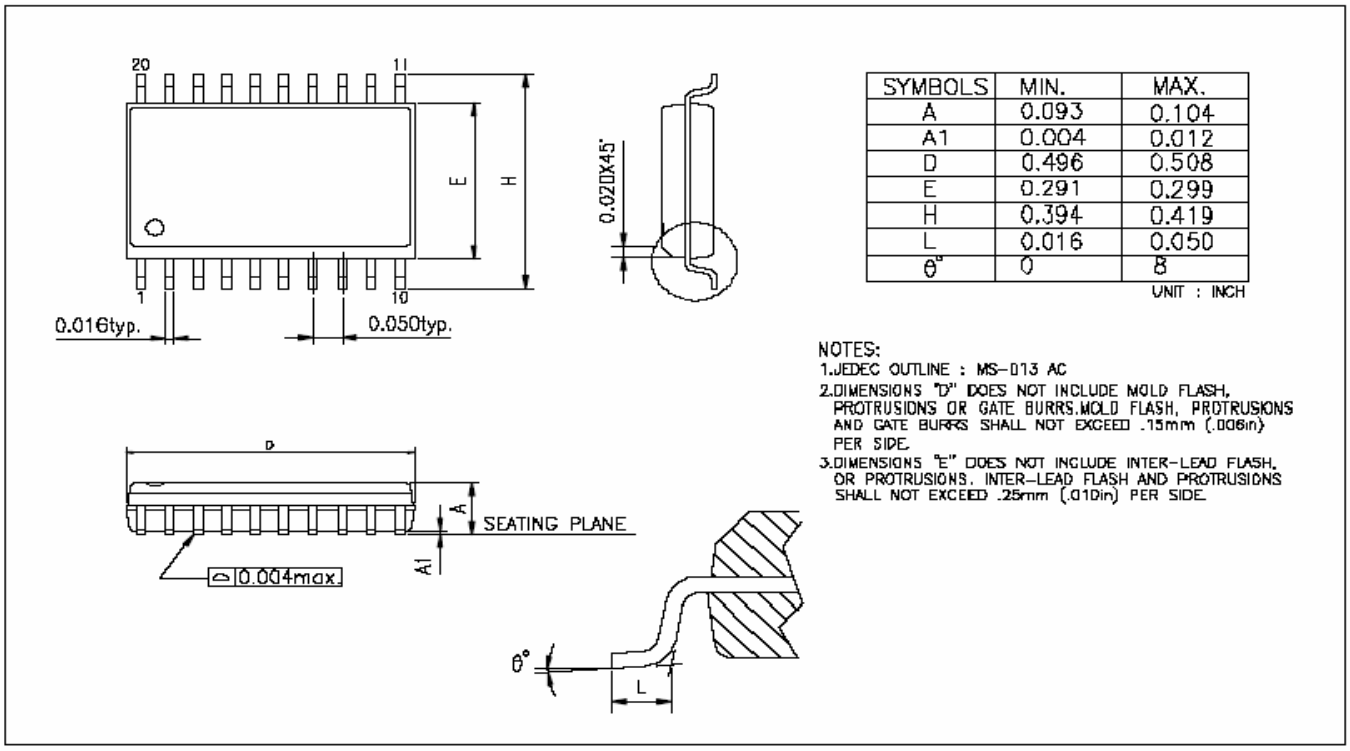
MTP: 1Kx16

000
. .
3FF

Preliminary

§ Package & PAD Information:

20-SOP

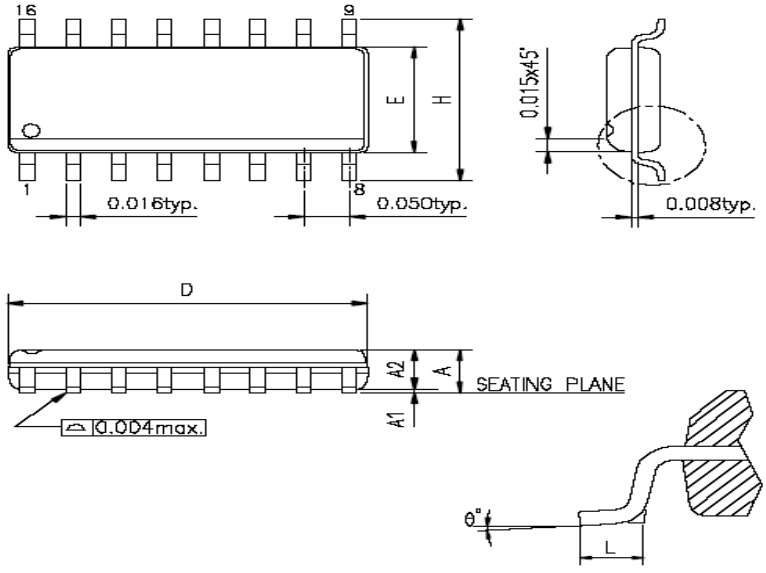


SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.496	0.508
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-013 AC
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.01Din) PER SIDE.

16-SOP



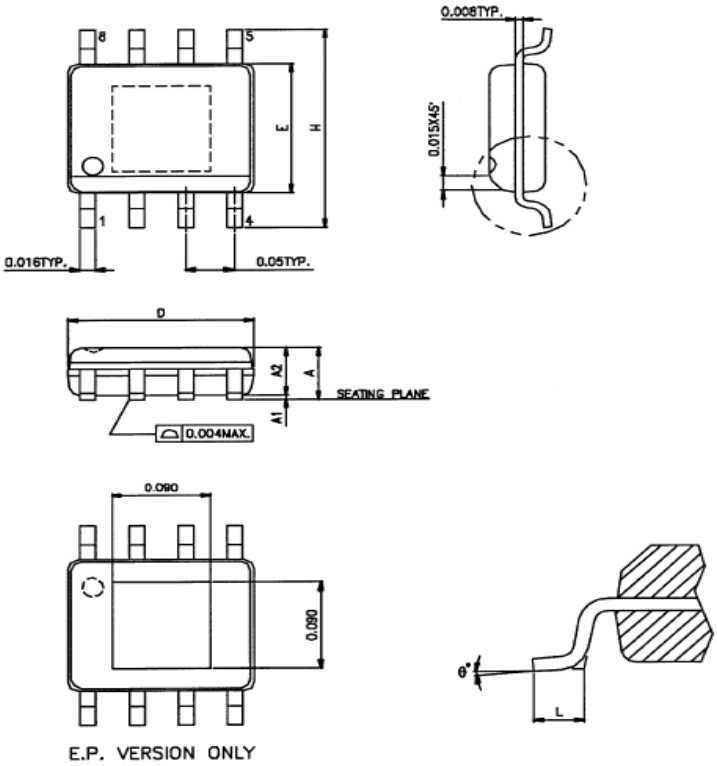
SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-012 AC
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

Preliminary

8-SOP

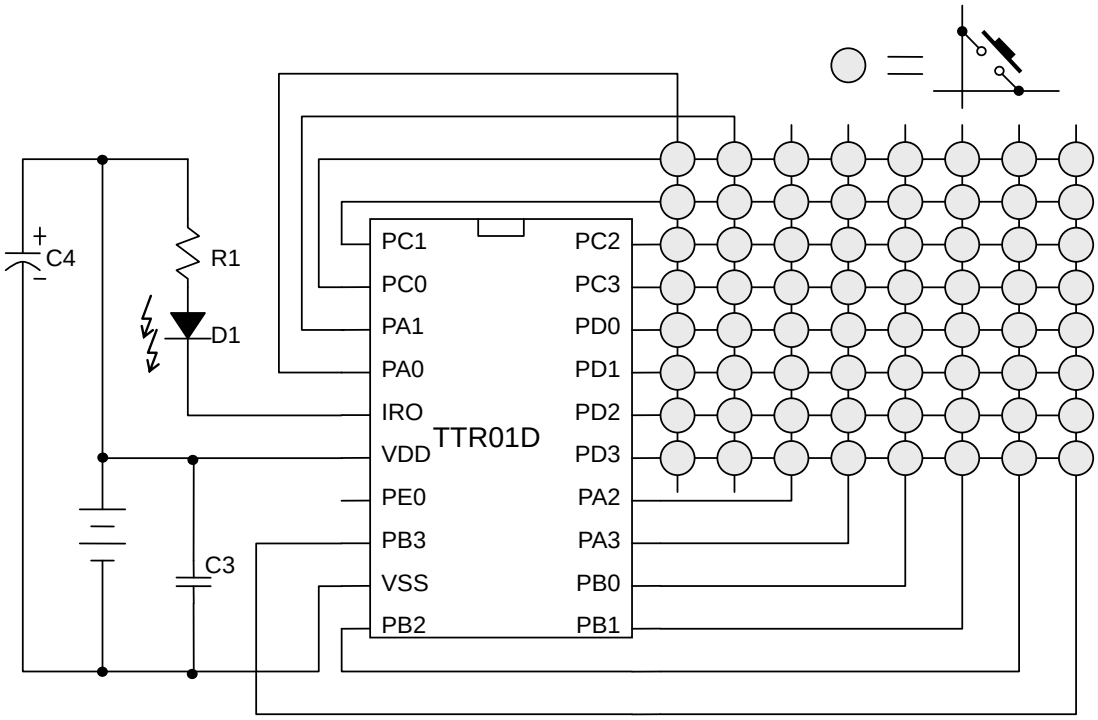


SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	—	0.059
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

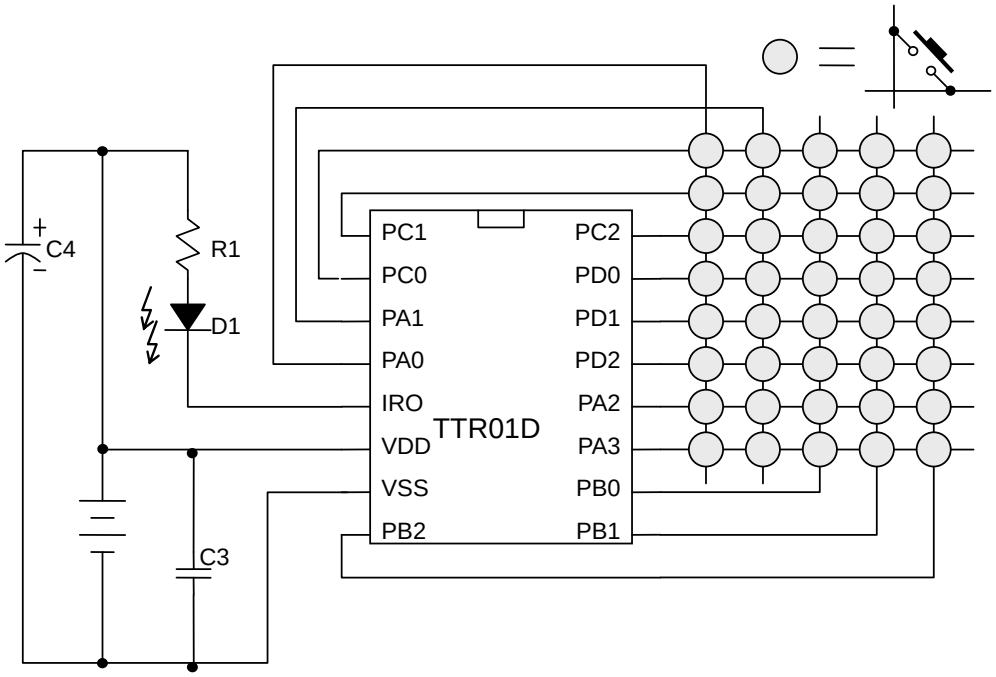
NOTES:
1. JEDEC OUTLINE : MS-012 AA / E.P. VERSION : N/A
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

§ Application Circuit



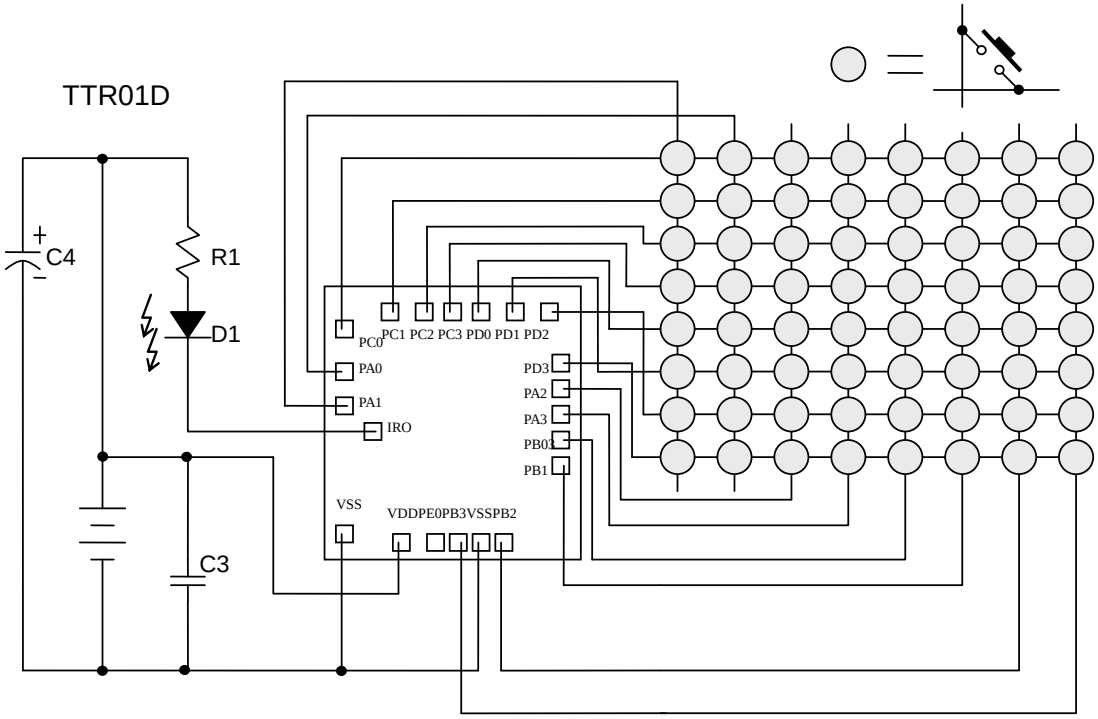
20 SOP application circuit example

Device	Recommended constant
R1	3.3~10 Ω
C3	0.1 μF
C4	4.7 μF
D1	IR LED



16 SOP application circuit example

Device	Recommended constant
R1	3.3~10 Ω
C3	0.1 μF
C4	4.7 μF
D1	IR LED



DICE application circuit example

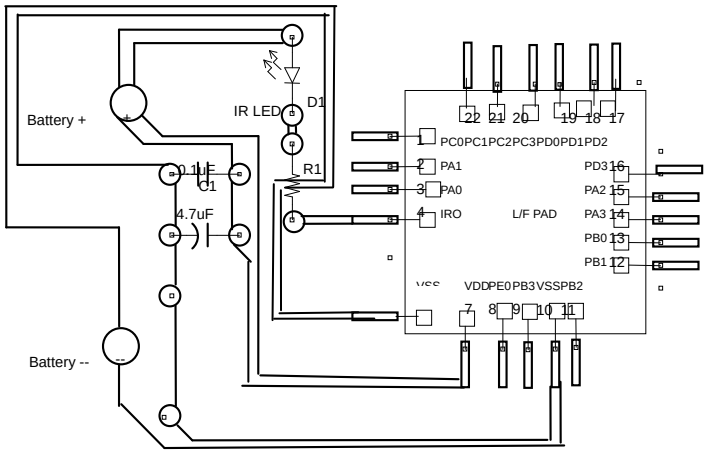
Device	Recommended constant
R1	3.3~10 Ω
C3	0.1 μF
C4	4.7 μF
D1	IR LED

Appendix:

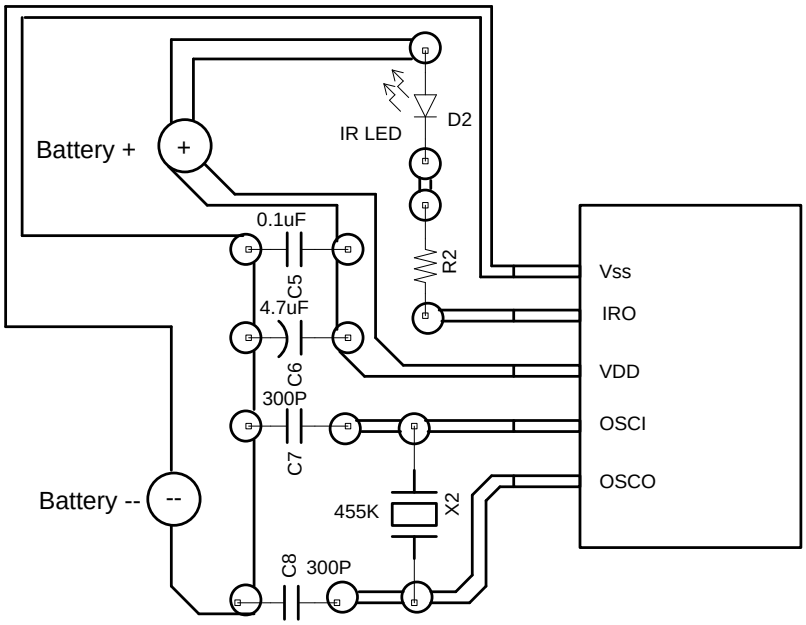
For the remote control application, the IR transmission may cause the variations in current from a few hundred uA to a few hundred mA. This current variation will generate overshoot and undershoot noise on the power line to cause the system malfunction.

To reduce the noise and stabilize the operation of the chip, we recommend the application designer design the PCB for the remote controller as follows to reduce the overshoot and undershoot of the IR LED drive current.

- ✧ Oscillator circuit (resonator & capacitors) should be located as near as possible to the chip
- ✧ PCB pattern for V_{DD} & V_{SS} should be as wide and short as possible
- ✧ IR LED should be located as far as possible from the chip
- ✧ Power supply battery and power capacitor (0.1uF & 4.7uF) should be located as near as possible to the chip
- ✧ The V_{DD} pattern of the IR LED and the power pins of the chip (V_{DD} & V_{SS}) should be separated and connected directly with the battery terminal
- ✧ The power capacitors (0.1uF & 4.7uF) is recommend to reduce the noise
- ✧ Keeping substrate floating and L/F pad connects to V_{SS} power line in dice form
- ✧ The recommended R1/R2 is 15Ω



Recommended PCB layout for dice



Recommended PCB layout for package

Preliminary

§ Ordering Form:

a. Package form : TTR01D-zzz
b. Chip form : TCR01D-zzz
c. Wafer base : TDR01D-zzz

Modified Record:

Date	Name	Version	Page	Content
2012/9/11	Hans Yang	V3.0-000	1~34	
2012/10/17	Hans Yang	V3.1-000		
2012/10/29	Hans Yang	V3.2-000	27	
2013/2/05	Ricky Chang	V3.3	2	SOP 8 Update
2015/10/08	Benson Chang	V3.4	2	Remove 16-SOP-A, 16-SOP-B, 8-SOP package.