8 keys Touch Pad Detector IC

Outline

- The TTP239 TonTouch™ IC is capacitive sensing design specifically for touch pad controls. The device built in regulator for touch sensor. Stable sensing method can cover diversity conditions. Human interfaces control panel links through non-conductive dielectric material. The main application is focused at replacing of the mechanical switch or button. The ASSP can independently handle the 8 touch pads with 8 direct output pins.

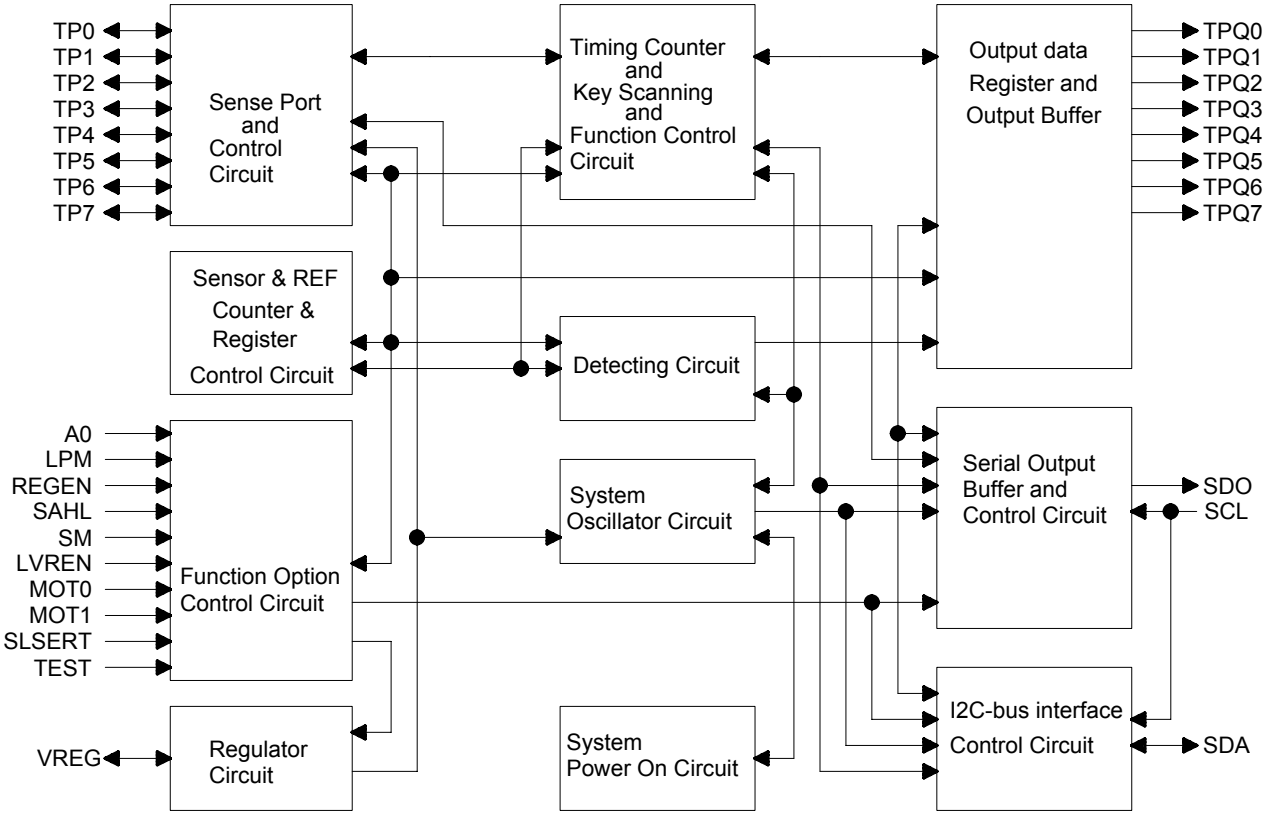
Characteristic

- Operating voltage 2.4V ~ 5.5V
- Built-in regulator with external enable/disable option (REGEN pin)
- Built-in low voltage reset(LVR) function with external enable/disable option (LVREN pin)
- Operating current, @VDD=3V no load, LDO enable
  At low power mode typical 5.0uA, At fast mode typical 30uA
- @VDD=3V operating voltage :
  The response time about 160mS at low power mode, 60mS at fast mode
- Sensitivity can adjust by the capacitance（1~50pF）outside for each touch pad
- Provides Fast mode and Low Power mode selection by pad option (LPM pin)
- Provides 8 direct outputs for 8 direct input keys. And all can select active high or active low by pad option (SAHL pin)
- Provides two kinds of serial output interface
  Include 2-wires and I^2C-bus slave serial interface that can be selected by pad option (SLSERT pin)
- Have the maximum on time 120sec/64sec/16sec/infinite by pad option (MOT1, MOT0 pin)
- Provides Single-key and Multi-key functions by pad option (SM pin)
- 2-wires serial interface can select active high or low by pad option (SAHL pin)
- After power-on have about 0.5sec stable-time, during the time do not touch the key pad, and the function is disabled
- Auto calibration for life
  The re-calibration period is about 1 sec within 8 sec after power-on. When key has been touched within 8 sec or key has not been touched more than 8 sec after power-on, then the re-calibration period change to 4 sec

Applications

- Wide consumer products
- Button key replacement

Block diagram



Pin Description

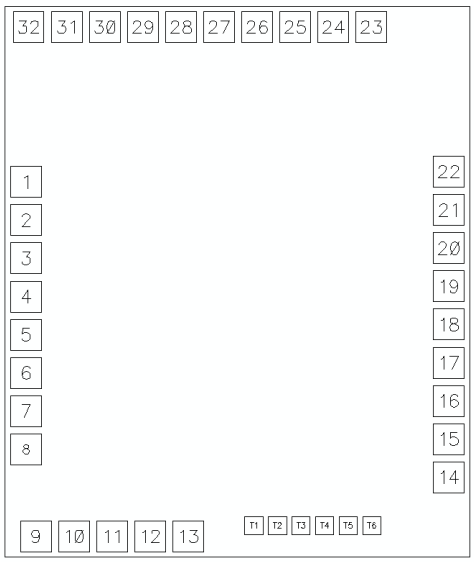
Pad NO	Pad Name	Type	Pad Description
1	TP7	I/O	Touch pad input pin
2	TP6	I/O	Touch pad input pin
3	TP5	I/O	Touch pad input pin
4	TP4	I/O	Touch pad input pin
5	TP3	I/O	Touch pad input pin
6	TP2	I/O	Touch pad input pin
7	TP1	I/O	Touch pad input pin
8	TP0	I/O	Touch pad input pin
9	LPM	I-PH	Low power/fast mode option 1(Default)=>Low power mode; 0=>Fast mode
10	REGEN	I-PH	Internal regulator enable/disable function option 1(Default)=>enable; 0=>disable
11	TEST	I-PL	Only for test
12	TPQ0	O	Direct output for TP0 touch input pin
13	TPQ1	O	Direct output for TP1 touch input pin
14	VDD	P	Positive power supply

<table>
<tr><td>15</td><td>VREG</td><td>P</td><td>Internal regulator output pin</td></tr>
<tr><td>16</td><td>TPQ2</td><td>O</td><td>Direct output for TP2 touch input pin</td></tr>
<tr><td>17</td><td>TPQ3</td><td>O</td><td>Direct output for TP3 touch input pin</td></tr>
<tr><td>18</td><td>SDA</td><td>I/OD</td><td>Data pin for the I^{2}C-bus serial data interface</td></tr>
<tr><td>19</td><td>SDO</td><td>O</td><td>Data pin for the 2-wires serial output
Option active Low/High by SAHL</td></tr>
<tr><td>20</td><td>SCL</td><td>I</td><td>Serial clock input pin for serial type
At 2-wires serial type can be set active Low/High by SAHL
When does not use serial interface type, the SCL pin must be connected to VDD or VSS, it does not float</td></tr>
<tr><td>21</td><td>TPQ4</td><td>O</td><td>Direct output for TP4 touch input pin</td></tr>
<tr><td>22</td><td>TPQ5</td><td>O</td><td>Direct output for TP5 touch input pin</td></tr>
<tr><td>23</td><td>TPQ6</td><td>O</td><td>Direct output for TP6 touch input pin</td></tr>
<tr><td>24</td><td>TPQ7</td><td>O</td><td>Direct output for TP7 touch input pin</td></tr>
<tr><td>25</td><td>VSS</td><td>P</td><td>Negative power supply, ground</td></tr>
<tr><td>26</td><td>SAHL</td><td>I-PH</td><td>Output active high or low option
1(Default)=>active-high for TPQ0~7, active-low for 2-wires serial type(SCL and SDO)
0=>active-low for TPQ0~7, active-high for 2-wires serial type(SCL and SDO)</td></tr>
<tr><td>27</td><td>A0</td><td>I-PH</td><td>A0 is input pin for the I^{2}C-bus device address selection I^{2}C ID Address=1010 10X, default:1</td></tr>
<tr><td>28</td><td>SM</td><td>I-PH</td><td>Multi-key/Single-key option
1(Default)=>Multi-key mode; 0=>Single-key mode</td></tr>
<tr><td>29</td><td>LVREN</td><td>I-PH</td><td>LVR function enable/disable option
1(Default)=>enable; 0=>disable</td></tr>
<tr><td>30</td><td>MOT1</td><td>I-PH</td><td rowspan="2">Key maximum on time function option, 11(Default)
<table>
<tr><th>MOT0</th><th>MOT1</th><th>Maximum on time</th></tr>
<tr><td>1</td><td>1</td><td>Infinite</td></tr>
<tr><td>0</td><td>1</td><td>16sec</td></tr>
<tr><td>1</td><td>0</td><td>64sec</td></tr>
<tr><td>0</td><td>0</td><td>120sec</td></tr>
</table></td></tr>
<tr><td>31</td><td>MOT0</td><td>I-PH</td></tr>
<tr><td>32</td><td>SLSERT</td><td>I-PH</td><td>The option pin for serial output type selection, Defaut:1</td></tr>
</table>

Pin Type

- I CMOS input only
- O CMOS push-pull output
- I／O CMOS I／O
- P Power／Ground
- I-PH CMOS input and pull-high resister
- I-PL CMOS input and pull-low resister
- OD Open drain output

Pad's Diagram



CHIP SIZE: 1360um x 1595um
Substrate floating (recommend) or VSS

Pad's Coordinate

Pad NO.	Pad Name	X	Y	Pad NO.	Pad Name	X	Y
1	TP7	-582.50	274.40	17	TPQ3	582.50	-222.60
2	TP6	-582.50	169.40	18	SDA	582.50	-177.60
3	TP5	-582.50	64.40	19	SDO	582.50	-12.60
4	TP4	-582.50	-40.60	20	SCL	582.50	92.40
5	TP3	-582.50	-145.60	21	TPQ4	582.50	197.40
6	TP2	-582.50	-250.60	22	TPQ5	582.50	302.40
7	TP1	-582.50	-355.60	23	TPQ6	369.40	700.00
8	TP0	-582.50	-460.60	24	TPQ7	264.40	700.00
9	LPM	-555.50	-700.00	25	VSS	159.40	700.00
10	REGEN	-450.50	-700.00	26	SAHL	54.40	700.00
11	TEST	-345.50	-700.00	27	A0	-50.60	700.00
12	TPQ0	-240.50	-700.00	28	SM	-155.60	700.00
13	TPQ1	-135.50	-700.00	29	LVREN	-260.60	700.00
14	VDD	582.50	-537.60	30	MOT1	-365.60	700.00
15	VREG	582.50	-432.60	31	MOT0	-470.60	700.00
16	TPQ2	582.50	-327.60	32	SLSERT	-575.60	700.00

Electrical Characteristics

- **Absolute maximum ratings**

Parameter	Symbol	Conditions	Rating	Unit
Operating Temperature	T_{OP}	—	-40～+85	℃
Storage Temperature	T_{STG}	—	-50～+125	℃
Supply Voltage	VDD	Ta=25°C	VSS-0.3～VSS+5.5	V
Input Voltage	V_{IN}	Ta=25°C	VSS-0.3～VDD+0.3	V
Human Body Mode	ESD	—	5	KV
Note：VSS symbolizes for system ground				

- **DC / AC characteristics：（Test condition at room temperature = 25 ℃）**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	Internal regulator disable	2.0		5.5	V
		Internal regulator enable	2.4		5.5	V
Internal Regulator Output	VREG		2.2	2.3	2.4	V
Operating Current	I_{OPL}	VDD=3V, At low power mode(regulator enable)		5.0		uA
	I_{OPF}	VDD=3V, At fast mode (regulator enable)		30.0		uA
Input Ports	V_{IL}	Input Low Voltage	0		0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8		1.0	VDD
Output Port Sink Current	I_{OL}	VDD=3V, V_{OL}=0.6V		8		mA
Output Port Source Current	I_{OH}	VDD=3V, V_{OH}=2.4V		-4		mA
Input Pin Pull-high Resistor	R_{PH}	VDD=3V		30K		ohm
Input Pin Pull-low Resistor	R_{PL}	VDD=3V		30K		ohm
Output Response Time	T_R	VDD=3V、At fast mode		60		mS
		VDD=3V、At low power mode		160		

Function Description

Ⅰ. Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP239 offers some methods for adjusting the sensitivity outside

1. by the electrode size

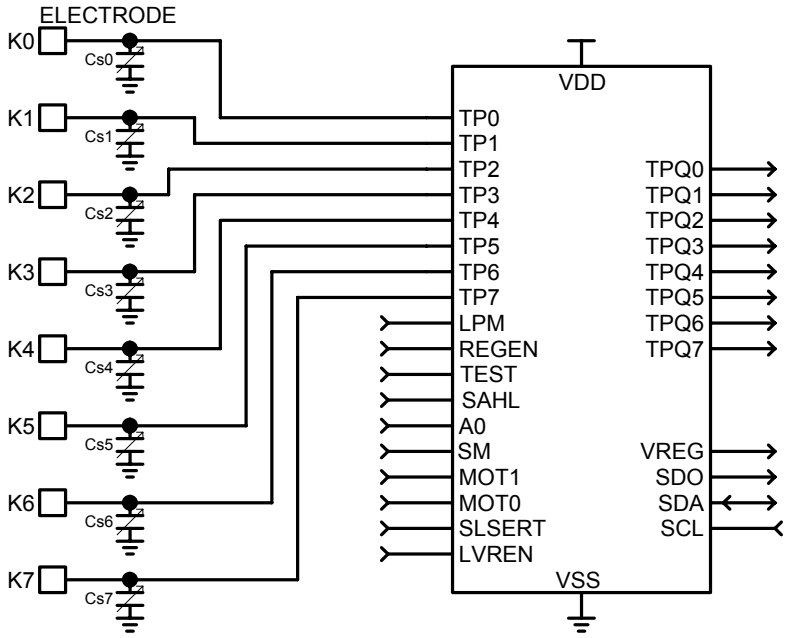
   Under other conditions are fixed. Using a larger electrode size can increase sensitivity. Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope

2. by the panel thickness

   Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value

3. by the value of Cs0~Cs7（please see the below figure）

   Under other conditions are fixed. Add the capacitors Cs0~Cs7 can fine tune the sensitivity for single key, that lets all key's sensitivity identical. When do not use any capacitor to VSS, the sensitivity is most sensitive. When adding the values of Cs0~Cs7 will reduce sensitivity in the useful range（1≦Cs0~Cs7≦50pF）



Ⅱ. Output mode（By SAHL pad option）

The TTP239 outputs（TPQ0~TPQ7）has direct mode active high or low by SAHL pad option, and 2-wires serial interface can select active high or low by SAHL pad option

SAHL	Pad TPQ0～TPQ7 and SCL SDO option features	Remark
1	Direct mode, CMOS output active high 2-wires serial type, SDO and SCL active low	Default
0	Direct mode, CMOS output active low 2-wires serial type, SDO and SCL active high	

Ⅲ. Key operating mode（By SM pad option）

The TTP239 has the Single-key and Multi-key functions by SM pad option

SM	Option features	Remark
1	Multi-key mode	Default
0	Single key mode	

Multi-key mode：The TP0-TP7 can be detected 2 keys or above 2 keys at the same time

Single-key mode：The TP0-TP7 can be detected 1 key only at the same time, when any key be detected, the other 7 keys can not be detected

Ⅳ. Maximum key on duration time（By MOT1、MOT0 pad option）

If some objects cover in the sense pad, and causing the change quantity enough to be detected. To prevent this, the TTP239 sets a timer to monitor the detection. The timer is the maximum on duration time. When the detection is over the timer, the system will return to the power-on initial state, and the output becomes inactive until the next detection

MOT1	MOT0	Option features	Remark
0	0	Maximum on time 120 sec	
0	1	Maximum on time 64 sec	
1	0	Maximum on time 16 sec	
1	1	Infinite（Disable maximum on time）	Default

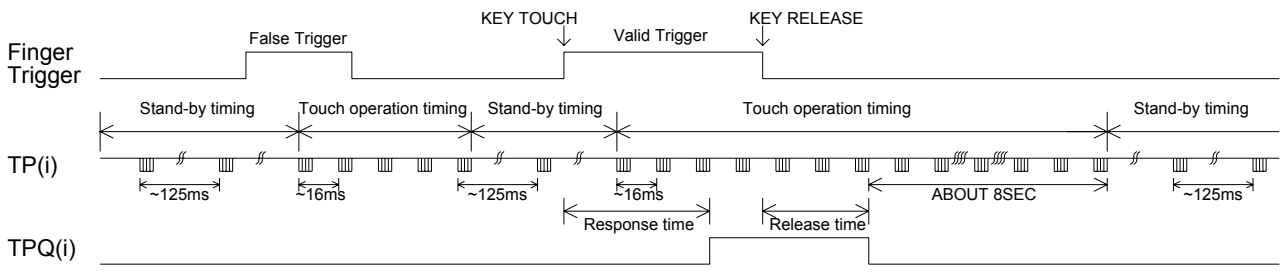
Ⅴ. Fast and Low power mode select（By LPM pad option）

The TTP239 has Fast mode and Low Power mode to be selected. It depends on the state of LPM pad. When the LPM pin is connected to VSS, the TTP239 runs in Fast mode. When the LPM pin is opened or connected to VDD, the TTP239 runs in Low Power mode.

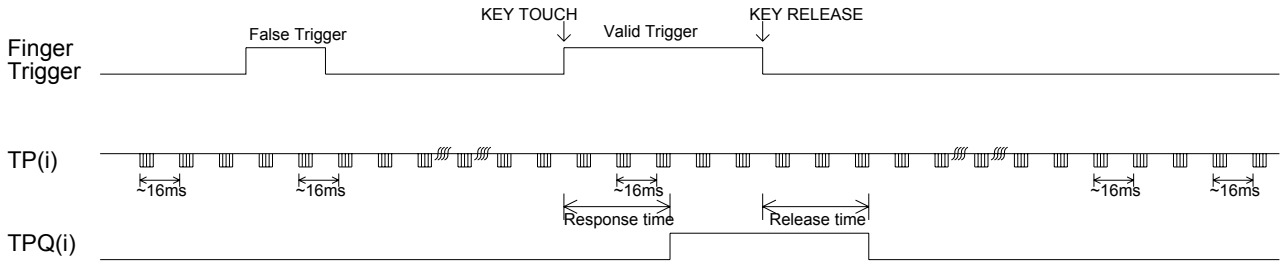
In the Fast mode response time is faster, but the current consumption will be increased. In the Low Power mode it will be saving power, but will be slowing response time for first touch. When it awaked in fast mode, the response time is the same the fast mode. In this mode when detecting key touch, it will switch to Fast mode. Until the key touch is released and will keep a time about 8sec. Then it returns to Low Power mode.

The states and timing of two modes please see below figure.

Low Power Mode timing diagram:



Fast Mode timing diagram:



LPM	Option features	Remark
1	Low Power mode	Default
0	Fast mode	

Ⅵ. Internal regulator enable/disable

The TTP239 built in regulator in the chip. The regulator can be set enable or disable by the REGEN pin. The REGEN pin is opened or connected to VDD, the regulator is enabled. The REGEN pin is connected to VSS, the regulator is disabled. When the internal regulator is disabled, the VREG pin must be connected to external VDD.

REGEN	Option features	Remark
1	Enable internal regulator	Default
0	Disable internal regulator	

Ⅶ. Serial output interface

SLSERT	Option features	Remark
1	2-wires serial type	Default
0	I^2C-bus serial type	

7-1 The 2-wires serial output interface mode can be selected by the SLSERT pin that it has to be floated or connected to VDD. At the mode the SDO pin is data output pin, the SCL is clock input pin, both can be set active-high and active-low by SAHL pin. The default is active-low that SAHL pin is open or connected to VDD. Another it is active-high that is connected to VSS.
The 2-wires serial mode supports always polling data for other device on the system. Or other device can wait that TTP239 outputs the data valid (DV) signal by the SDO pin, and it can give the clock signal to TTP239 SCL pin and get the keys data from SDO pin.
The TTP239 2-wires serial interface supports a timeout mechanism for SCL pin. If the SCL pin has no signal edge change over 2ms, the 2-wires serial interface will reset itself and return to stand-by state.

2-wires serial interface mode timing please see below.
The D0~D7 correspond to data of the TP0~7.

7-1-1 When SAHL=0：Set active-high

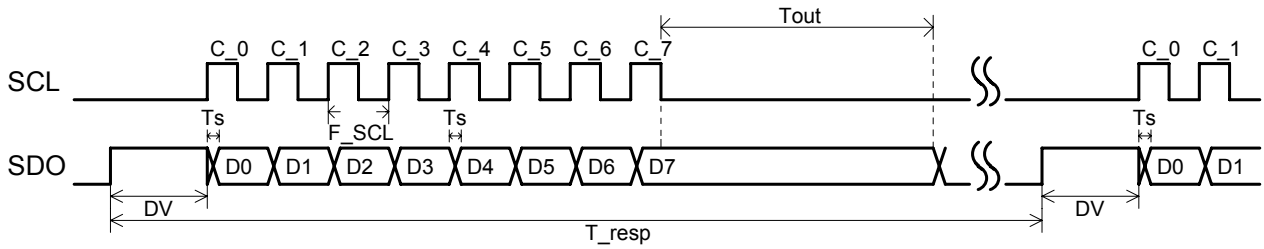


Figure 7-1-1：The timing for active-high

7-1-2 When SAHL=1：Set active-low

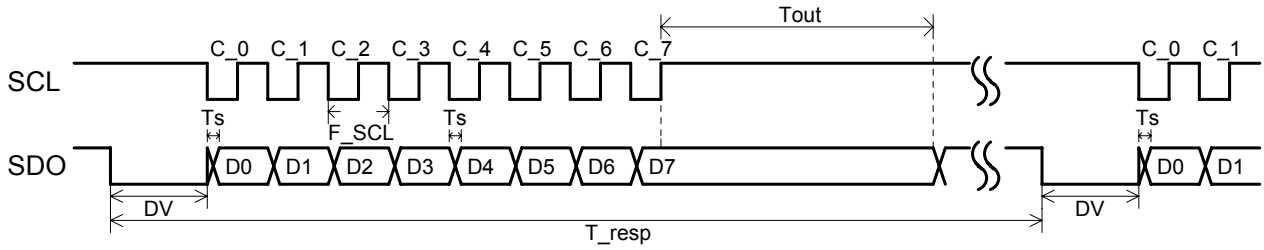


Figure 7-1-2：The timing for active-low

The parameters for figure 7-1-1~2：

Parameter	Min.	Typ.	Max.	Unit
DV(Time out)	-	2	-	ms
Ts	200	-	-	ns
Tout	-	2	-	ms
T_resp	-	16	-	ms
F_SCL	1K	-	512K	Hz

Note：

(1) When any data of the TP0~TP7 change, the SDO pin output DV signal, the time out of DV signal is about 2msec. But other device can not wait that the DV signal time is over, after it detect the DV signal, and then can give the clock signal to the TTP239 by the SCL pin at the duration of DV signal. When the TTP239 detect the first clock edge changing, and the DV signal is over, and the SDO pin change to output the data of TP0~TP7.

(2) The parameter Ts is data set-up time, it means that the data change time for SDO pin.

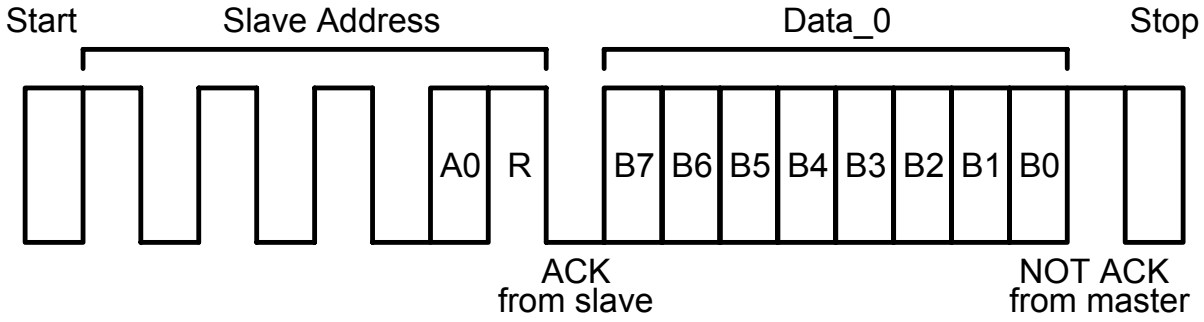
7-2 For I2C-bus slave interface mode selection, the SLSERT pin has to be connected to VSS.
At the mode the SDA pin is a serial data pin, the SCL is a serial clock input pin. The SDA and SCL pins must be pulled-high with an external resistor.
And the 4-bits identify code for the TTP239 is〝(1010)〞. The device address is defined 10 and A0. The A0 pin has pull-high resistor internal, can be set to 0 external. The TTP239 8-bits slave device address includes 4-bits identifier, 3-bits option address and R/W bit (see the Table 7-2-1).
The TTP239 IC uses the I^2C-bus slave interface data transmission protocol to output the data of the touch pads (TP0~TP7 pins), so the TTP239 only accepts the read operation that R/W bit is〝1〞. If it is〝0〞, the TTP239 will not respond the write operation. Otherwise, the I^2C-bus slave interface of TTP239 conforms to the communication protocols. It supports the fast mode that the maximum SCL clock frequency is 400KHz.
The I^2C-bus slave interface supports the following communication protocols:
Bus not busy : The SDA and the SCL lines remain High level when the bus is not active.
Start condition : Start condition is SDA 1 to 0 transition when SCL=1.(see figure 7-2-2)
Stop condition : Stop condition is SDA 0 to 1 transition when SCL=1.(see figure 7-2-2)
Data valid : Following a start condition, the data on the SDA line must be stable during the High period of SCL. The High or Low state of the data line can only change when the clock signal on the SCL line is Low.(see figure 7-2-2)
ACK (Acknowledge) : An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the ninth clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data. But the slave does not send an ACK if it does not successfully received the eight bits of data.
In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the ninth clock period. If an ACK is detected, the slave will continue to transmit next data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.
Slave Address : The identify code for the TTP239 is〝(1010)〞. The device address is 10 and A0 pin.
Read/Write : The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is〝1〞, a read operation is executed. If it is〝0〞, a write operation is executed. But the TTP239 only accepts read operation.
The sequence of read data operation please see figure 7-2-1.

Table 7-2-1. Slave Device Addressing

Device	Device Identifier				Device Address			R/W Bit
	B7	B6	B5	B4	B3	B2	B1	B0
TTP239	1	0	1	0	1	0	A0	R

Note：

The SDA and SCL pins have Diode protective circuit. So when use two pins of TTP239 in the I2C-bus interface system. Do not propose to use the different voltage with the other devices in the I2C-bus interface system. That avoids to occurring the leakage current in the system.



Note : Data_0 : B7~B0 are TP0~TP7 on/off status. 0 is key off, 1 is key on.

Figure 7-2-1. Read Operation Sequence

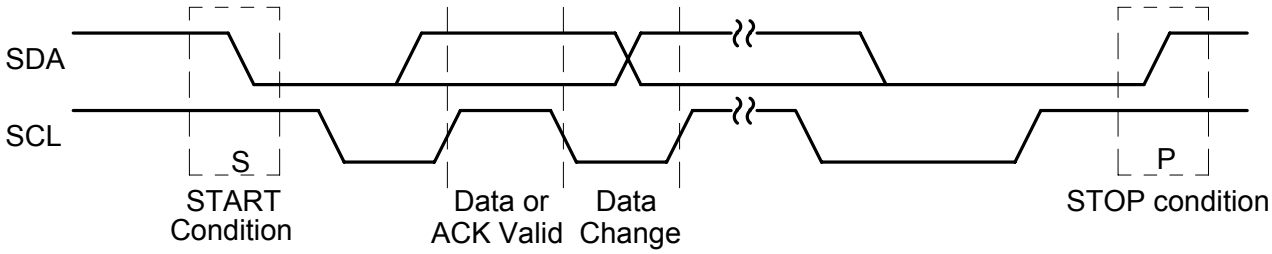


Figure 7-2-2. Data Transmission Sequence

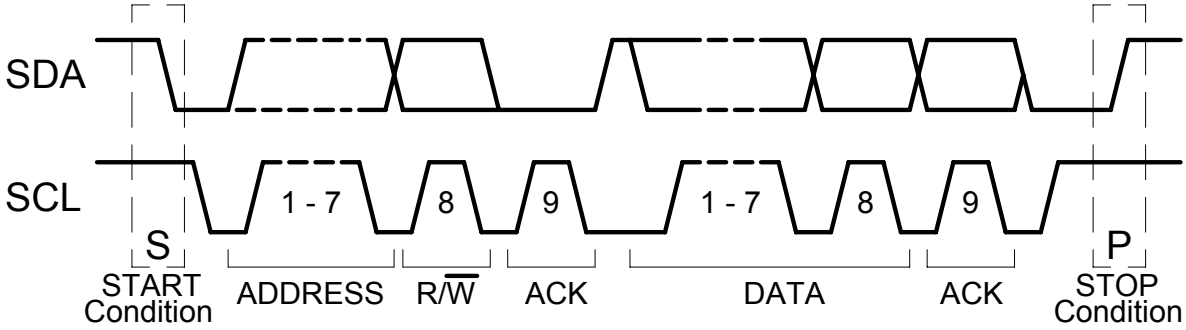


Figure 7-2-3. A complete data transfer

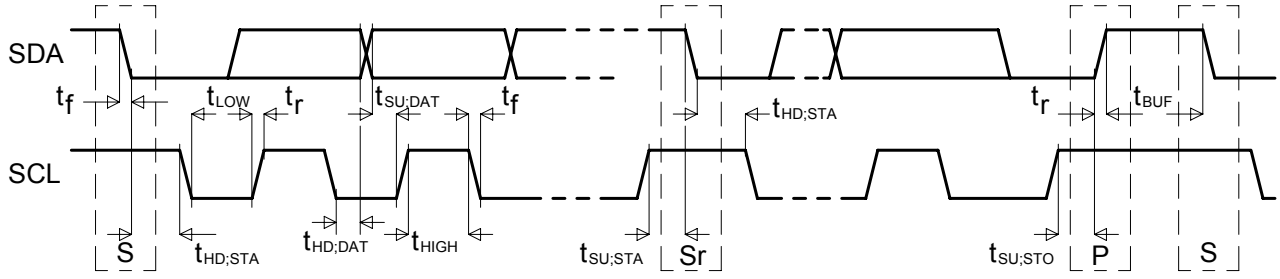
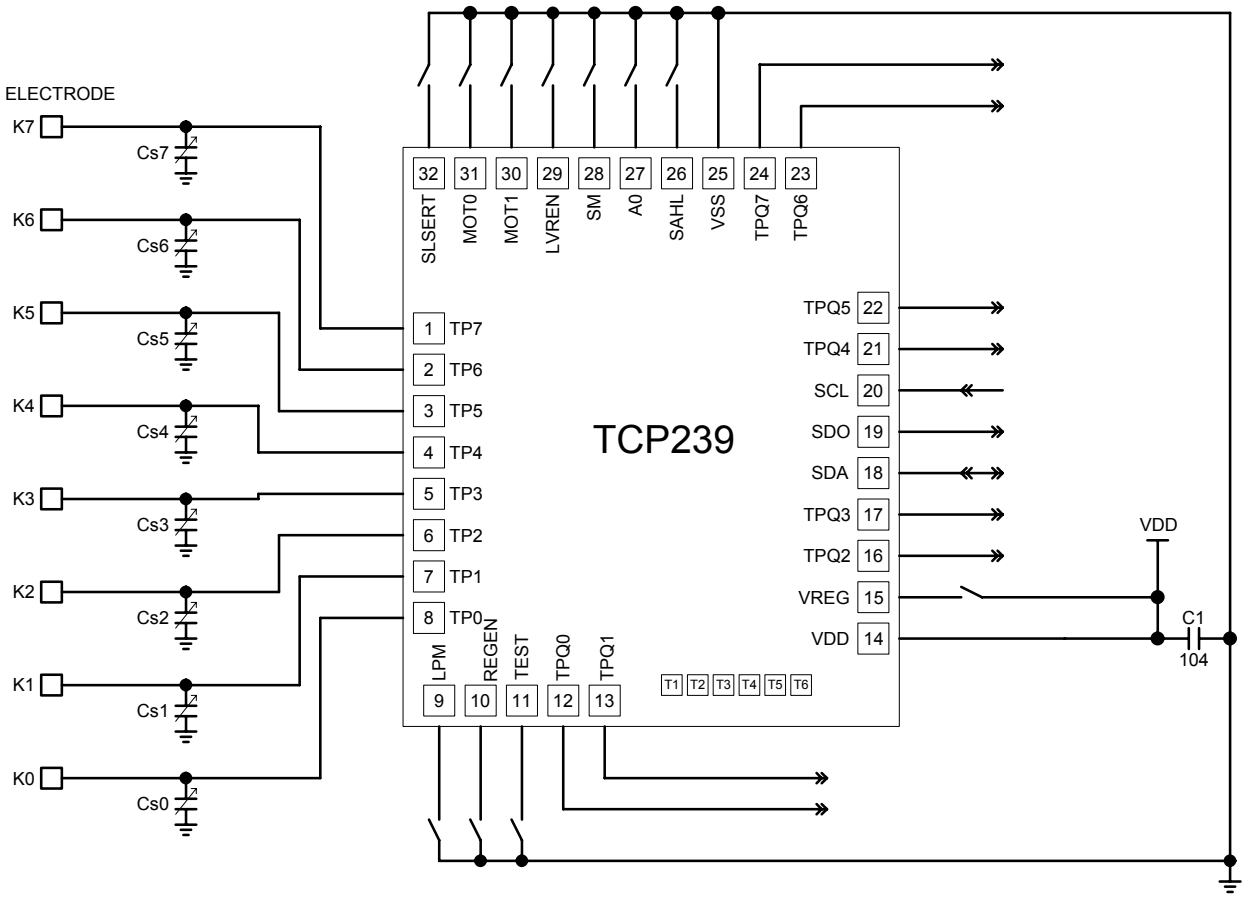


Figure 7-2-4. Definition of timing for F/S-mode devices on the I^2C-bus

Table 7-2-2. Characteristics of the SDA and SCL bus lines for F/S-mode I^2C-bus devices

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}		100		400	KHz
LOW period of the SCL clock	t_{LOW}	4.7		1.3		us
HIGH period of the SCL clock	t_{HIGH}	4.0		0.6		us
Hold time (repeated) START condition	$t_{HD;STA}$	4.0		0.6		us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7		0.6		us
Data hold time	$t_{HD;DAT}$	0		0		us
Data set-up time	$t_{SU;DAT}$	250		100		ns
Rise time of both SDA and SCL signals	t_r		1000		300	ns
Fall time of both SDA and SCL signals	t_f		300		300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0		0.6		us
Bus free time between a STOP and START condition	t_{BUF}	4.7		1.3		us
Capacitive load for each bus line	C_b		400		400	pF

Application circuit



P.S.：

1. On PCB, the length of lines from touch pad to IC pin shorter is better.
   And the lines do not parallel and cross with other lines.
2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
3. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
4. The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP239).
5. The capacitance Cs0~Cs7 can be used to adjust the sensitivity. The value of Cs0~Cs7 use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range of Cs0~Cs7 value are 1~50pF.
6. The sensitivity adjustment capacitors（Cs0~Cs7）must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.
7. When the system doesn't use the serial output interface for TTP239, the SCL pin of TTP239 must be connected to VDD or VSS.

Ordering Information

TTP239		
Package Type	**Chip Type**	**Wafer Type**
TTP239-XXX	TCP239	TEP239

REVISE HISTORY

1. 2015/12/07
   - Original version：V1.0
2. 2016/3/7
   - Add the Serial output interface function and pins SDA, SCL, SDO, A0, SLSERT, Change the package outline and configuration.
3. 2016/6/21
   -Change the page-6=> Ⅱ**. Output mode description.**
   Delete the page-14,15=> Package outline and Package configuration.