Reference Only
Version ： 1.2
Date：2010/08/05

TCU981B 8 Bits TV game system

General Description：

TCU981B is a single chip microprocessor for use in TV game. It is composed of CPU(6502), PPU(picture processor unit), PSG(programmable sound generator), 2KB working RAM, 2KB video RAM, DMA unit, and other control circuit.

The IC apply to display variable animated cartoon. In background picture, it supply 2-page size in the screen; In sprite picture, it also supply 64 sprites per frame. Besides, the X and Y coordinate positions is programmable to display the actual area (Resolution : 256 x 240 pixels).

The IC apply to multi-mix sound output. It with 5 channels programmable sound generator, include 3 rhythm channels, 1 noise channel, and 1 PCM voice channel.

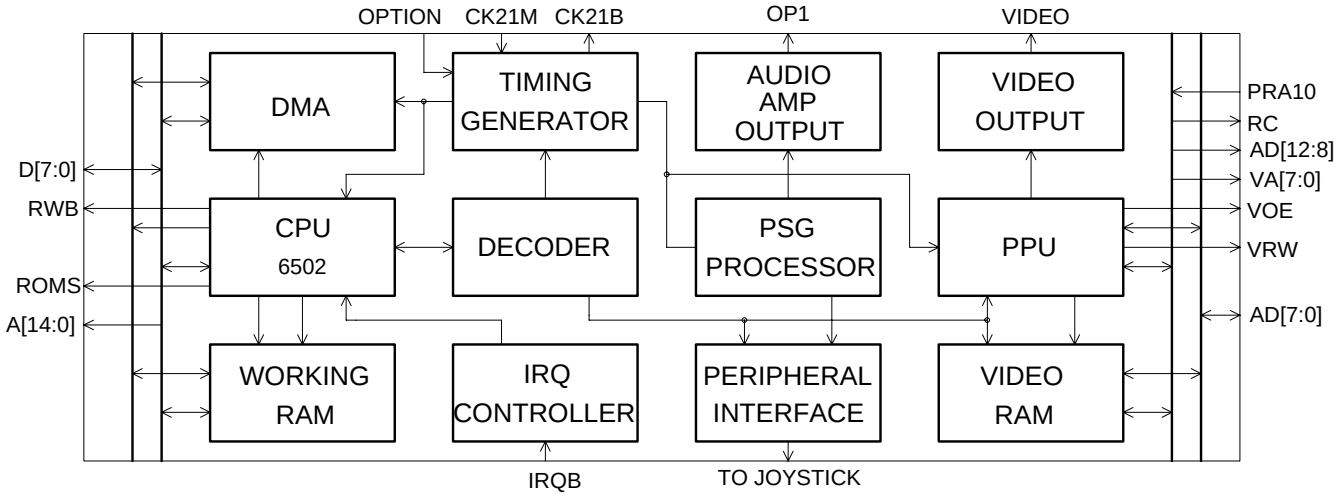
The IC apply to following TV system : include PAL-B , NTSC , PAL-M , and PAL-N. System select by bonding option.

The IC apply to following interface product : include keyboard, joystick, mouse, light gun, etc.

Features：

- 8 Bits single chip TV game system.
- Built-in 6502 CPU.
- Built-in PPU(picture processor unit).
- Built-in PSG(programmable sound generator).
- Built-in RAM: Working RAM(2K Bytes) & Video RAM(2K Bytes).
- Built-in DMA unit.
- Apply to many kind TV system(PAL-B, NTSC, PAL-M, PAL-N)
- TV system can select by bonding option.
- 5 sound channels(3 rhythm, 1 noise, and 1 voice).
- Few external components needed.
- Simple application circuit.
- Low power consumption.

Block Diagram：

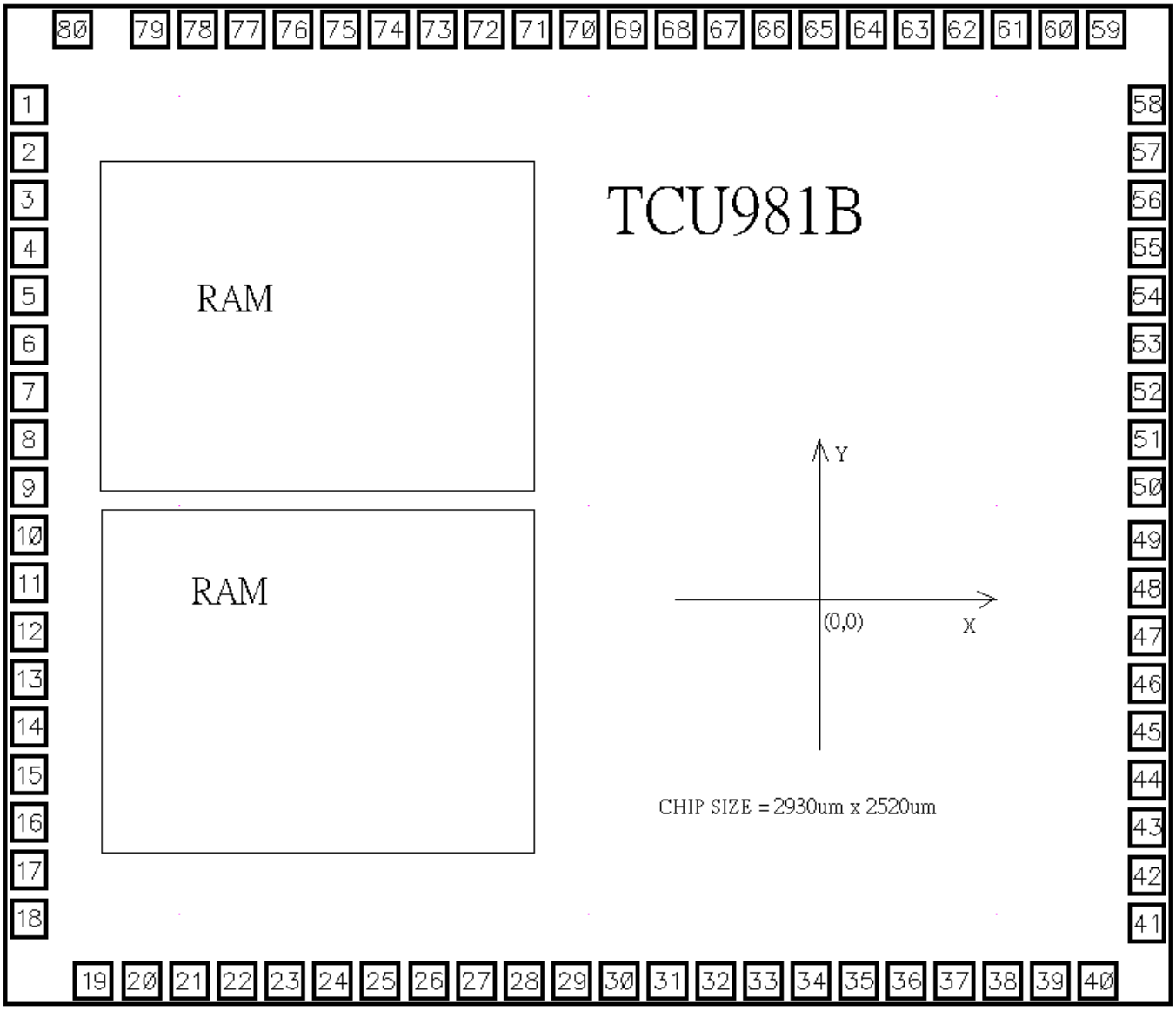


Pad / Pin Description：

PAD No.	PAD Name	I/O	DESCRIPTION
1	VRW	O	Read/Write control signal of PPU memory
2	VOE	O	Data read-out enable control signal of PPU memory
3	PRA10	I	Address BUS of PPU ; MSB of VRAM address
4	VA6	O	Address BUS of PPU(picture process unit)
5	VA7	O	Address BUS of PPU(picture process unit)
6	VA5	O	Address BUS of PPU(picture process unit)
7	AD8	O	Address BUS of PPU(picture process unit)
8	VA4	O	Address BUS of PPU(picture process unit)
9	AD9	O	Address BUS of PPU(picture process unit)
10	VA3	O	Address BUS of PPU(picture process unit)
11	VSS	P	VSS power pin
12	AD10	O	Address BUS of PPU(picture process unit)
13	VA2	O	Address BUS of PPU(picture process unit)
14	AD11	O	Address BUS of PPU(picture process unit)
15	VA1	O	Address BUS of PPU(picture process unit)
16	AD12	O	Address BUS of PPU(picture process unit)
17	VA0	O	Address BUS of PPU(picture process unit)
18	RC	O	Address BUS of PPU(picture process unit)
19	AD0	I/O	Data BUS of PPU(picture process unit)
20	AD7	I/O	Data BUS of PPU(picture process unit)
21	AD1	I/O	Data BUS of PPU(picture process unit)
22	AD6	I/O	Data BUS of PPU(picture process unit)
23	AD2	I/O	Data BUS of PPU(picture process unit)
24	AD5	I/O	Data BUS of PPU(picture process unit)
25	AD3	I/O	Data BUS of PPU(picture process unit)
26	AD4	I/O	Data BUS of PPU(picture process unit)
27	CK21B	O	System clock output , to crystal oscillator
28	CK21M	I	System clock input , to crystal oscillator
29	VDD	P	VDD power pin
30	VIDEO	O	Video signal output
31	OP1	O	Audio AMP output (only for test)
32	PORN	I	TV system select (PAL/NTSC)
33	F50R6	I	TV system select (50Hz/60Hz)
34	VSS	P	VSS power pin
35	VSS	P	VSS power pin
36	RESTB	I	System reset input , “0” = Reset ; “1” (NC)= Normal
37	D046	I	Port $4016 input pin (bit 0) , connect to Joystick
38	D047	I	Port $4017 input pin (bit 0) , connect to Joystick
39	D147	I	Port $4017 input pin (bit 1) , connect to Joystick
40	CUP46	O	Port $4016 output CLK pin , connect to Joystick
41	D247	I	Port $4017 input pin (bit 2) , connect to Joystick
42	D146	I	Port $4016 input pin (bit 1) , connect to Joystick
43	D347	I	Port $4017 input pin (bit 3) , connect to Joystick

44	Q0	O	Port $4016 output pin (bit 0) , connect to Joystick
45	D447	I	Port $4017 input pin (bit 4) , connect to Joystick
46	Q1	O	Port $4016 output pin (bit 1) , connect to Joystick
47	Q2	O	Port $4016 output pin (bit 2) , connect to Joystick
48	CUP47	O	Port $4017 output CLK pin , connect to Joystick
49	VDD	P	VDD power pin
50	VDD	P	VDD power pin
51	A11	O	Address BUS of CPU
52	CK18	O	Ø2 single of CPU (clock output)
53	A10	O	Address BUS of CPU
54	A12	O	Address BUS of CPU
55	A9	O	Address BUS of CPU
56	A13	O	Address BUS of CPU
57	A8	O	Address BUS of CPU
58	A14	O	Address BUS of CPU
59	TESTB	I	Test mode control pin , ‘0” = Test mode , “1” (NC) = Normal
60	A7	O	Address BUS of CPU
61	D7	I/O	Data BUS of CPU
62	A6	O	Address BUS of CPU
63	D6	I/O	Data BUS of CPU
64	A5	O	Address BUS of CPU
65	D5	I/O	Data BUS of CPU
66	A4	O	Address BUS of CPU
67	D4	I/O	Data BUS of CPU
68	A3	O	Address BUS of CPU
69	D3	I/O	Data BUS of CPU
70	A2	O	Address BUS of CPU
71	D2	I/O	Data BUS of CPU
72	A1	O	Address BUS of CPU
73	D1	I/O	Data BUS of CPU
74	A0	O	Address BUS of CPU
75	D0	I/O	Data BUS of CPU
76	VDD	P	VDD power pin
77	RWB	O	Read/Write control signal of CPU
78	ROMS	O	Program ROM chip enable control signal
79	IRQB	I	Interrupt signal input of CPU
80	VSS	P	VSS power pin

PAD's Diagram：



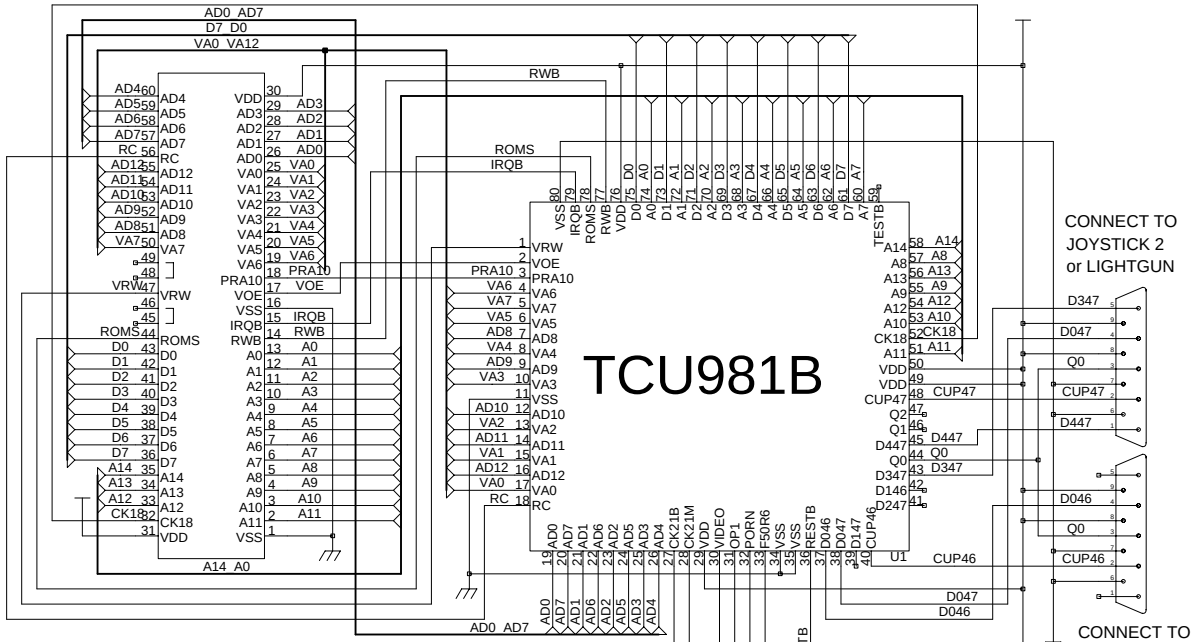
PAD's Coordinate:

PAD NO	PAD NAME	X	Y	PAD NO	PADNAME	X	Y
1	VRW	-1367.50	978.95	41	D247	1367.50	-1021.65
2	VOE	-1367.50	861.95	42	D146	1367.50	-904.65
3	PRA10	-1367.50	744.95	43	D347	1367.50	-787.65
4	VA6	-1367.50	627.95	44	Q0	1367.50	-670.65
5	VA7	-1367.50	510.95	45	D447	1367.50	-553.65
6	VA5	-1367.50	393.95	46	Q1	1367.50	-436.65
7	AD8	-1367.50	267.95	47	Q2	1367.50	-319.65
8	VA4	-1367.50	159.95	48	CUP47	1367.50	-202.65
9	AD9	-1367.50	42.95	49	VDD	1367.50	-85.65
10	VA3	-1367.50	-74.05	50	VDD	1367.50	43.55
11	VSS	-1367.50	-191.05	51	A11	1367.50	160.55
12	AD10	-1367.50	-308.05	52	CK18	1367.50	277.55
13	VA2	-1367.50	-425.05	53	A10	1367.50	394.55
14	AD11	-1367.50	-542.05	54	A12	1367.50	511.55
15	VA1	-1367.50	-659.05	55	A9	1367.50	628.55
16	AD12	-1367.50	-776.05	56	A13	1367.50	745.55
17	VA0	-1367.50	-893.05	57	A8	1367.50	862.55
18	RC	-1367.50	-1010.05	58	A14	1367.50	979.55
19	AD0	-1209.45	-1162.25	59	TESTB	1267.60	1162.25
20	AD7	-1092.45	-1162.25	60	A7	1150.60	1162.25
21	AD1	-975.45	-1162.25	61	D7	1033.60	1162.25
22	AD6	-858.45	-1162.25	62	A6	916.60	1162.25
23	AD2	-741.45	-1162.25	63	D6	799.60	1162.25
24	AD5	-624.45	-1162.25	64	A5	682.60	1162.25
25	AD3	-507.45	-1162.25	65	D5	565.60	1162.25
26	AD4	-390.45	-1162.25	66	A4	448.60	1162.25
27	CK21B	-273.45	-1162.25	67	D4	331.60	1162.25
28	CK21M	-156.45	-1162.25	68	A3	214.60	1162.25
29	VDD	-39.45	-1162.25	69	D3	97.60	1162.25
30	VIDEO	77.55	-1162.25	70	A2	-19.40	1162.25
31	OP1	194.55	-1162.25	71	D2	-136.40	1162.25
32	PORN	311.55	-1162.25	72	A1	-253.40	1162.25
33	F50R6	428.55	-1162.25	73	D1	-370.40	1162.25
34	VSS	545.55	-1162.25	74	A0	-487.40	1162.25
35	VSS	662.55	-1162.25	75	D0	-604.40	1162.25
36	RESTB	779.55	-1162.25	76	VDD	-721.40	1162.25
37	D046	896.55	-1162.25	77	RWB	-838.40	1162.25
38	D047	1013.55	-1162.25	78	ROMS	-955.40	1162.25
39	D147	1130.55	-1162.25	79	IRQB	-1072.40	1162.25
40	CUP46	1247.55	-1162.25	80	VSS	-1261.30	1162.25

CHIP SIZE = 2930um x 2520um

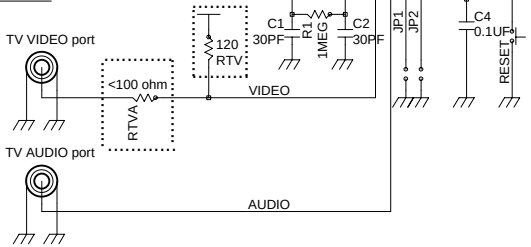
Reference Only
Version ： 1.2
Date：2010/08/05

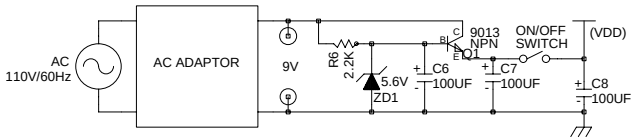
TCU981B APPLICATION (1)



1** : RTV resister adjust TV screen brightness, can be not used
(RTV more small, then brightness more lightness)

2** : C4 capacitor use 0.1uF (TCU981 : C4=1uF)

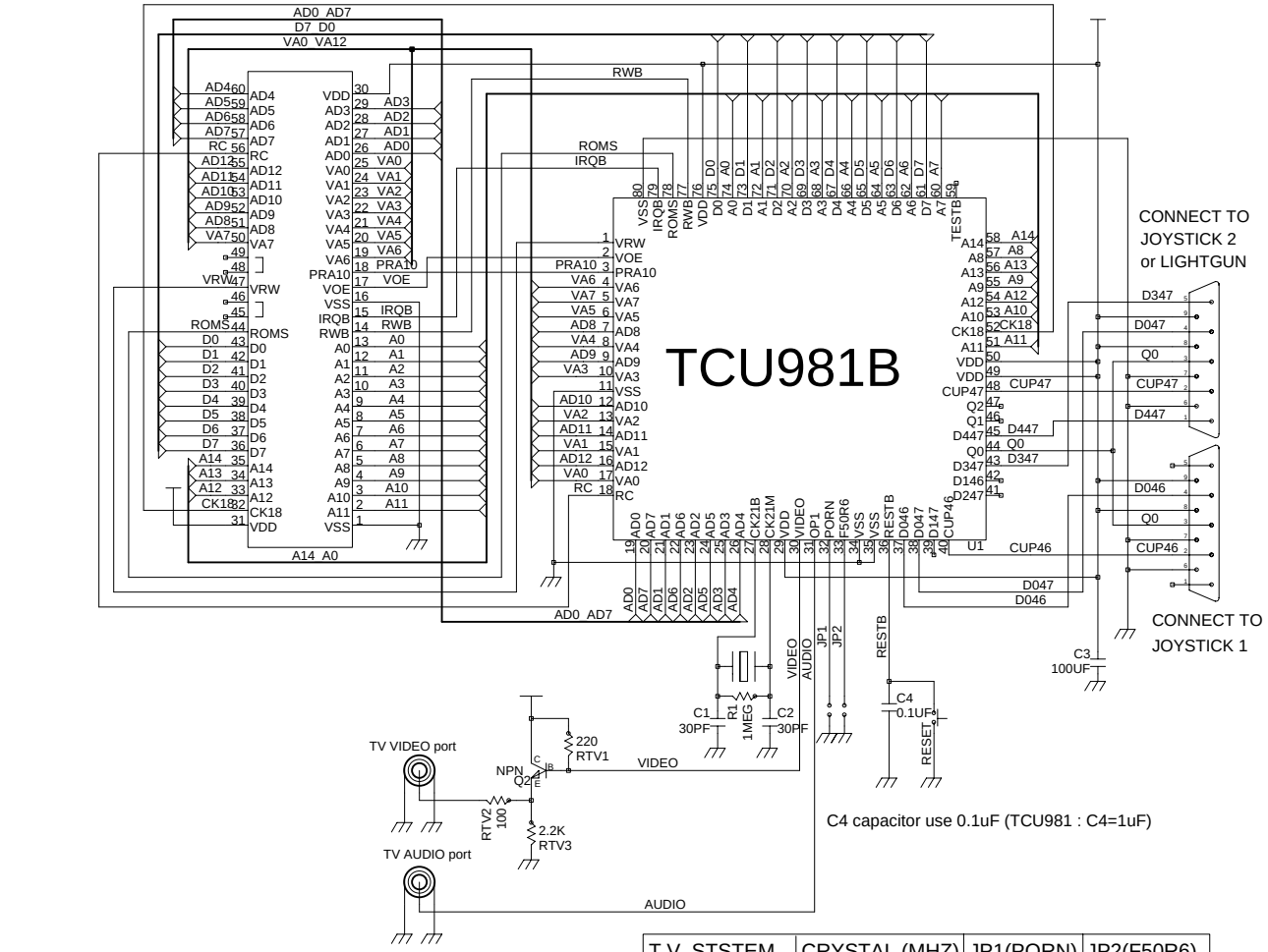




T V. STSTEM	CRYSTAL (MHZ)	JP1(PORN)	JP2(F50R6)
PAL B	26.601712	OPEN	OPEN
NTSC	21.477270	SHORT	SHORT
PAL M	21.453669	OPEN	SHORT
PAL N	21.492337	SHORT	OPEN

Reference Only
Version ： 1.2
Date：2010/08/05

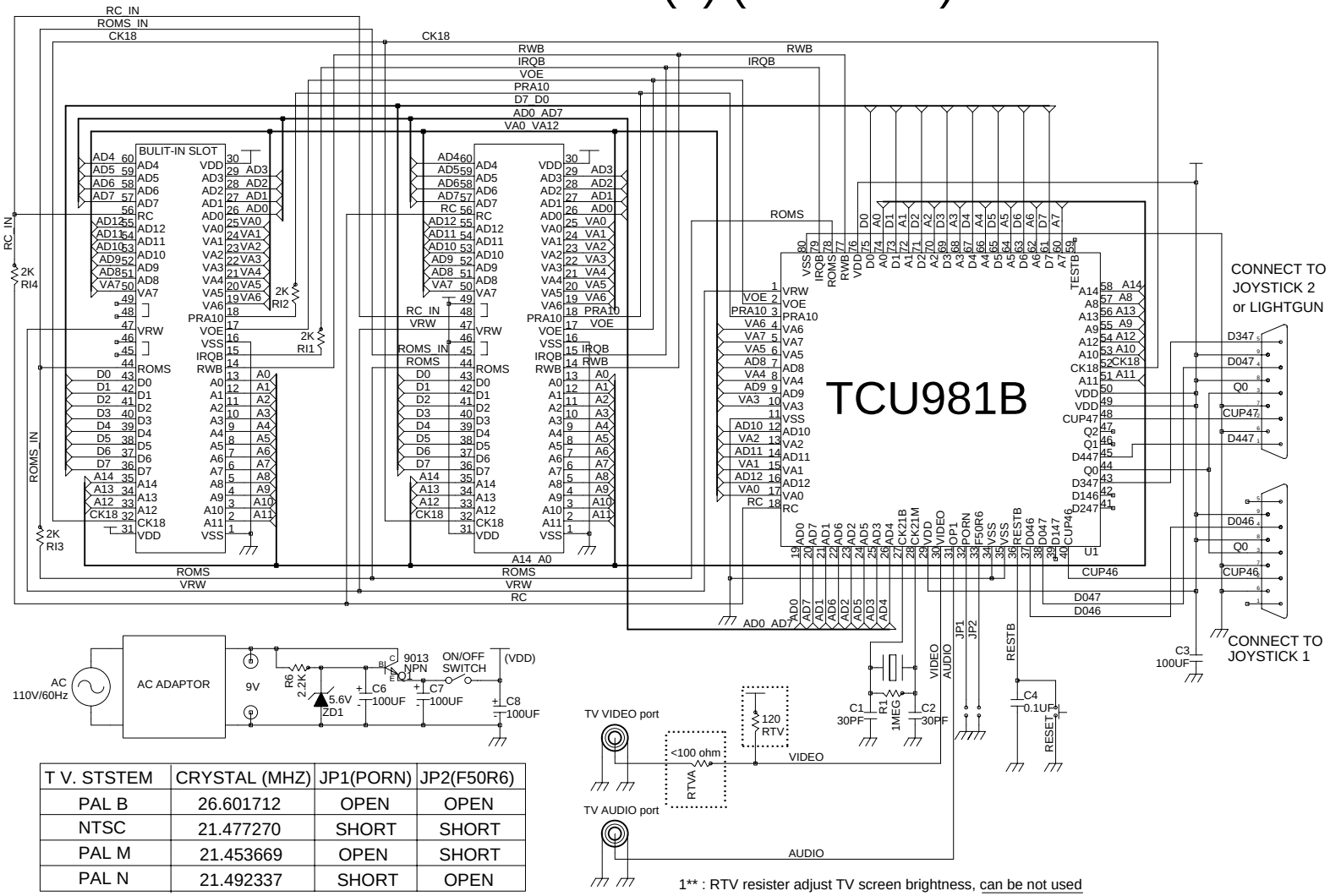
TCU981B APPLICATION (2)



C4 capacitor use 0.1uF (TCU981 : C4=1uF)

T V. STSTEM	CRYSTAL (MHZ)	JP1(PORN)	JP2(F50R6)
PAL B	26.601712	OPEN	OPEN
NTSC	21.477270	SHORT	SHORT
PAL M	21.453669	OPEN	SHORT
PAL N	21.492337	SHORT	OPEN

TCU981B APPLICATION (1) (BUILT-IN)

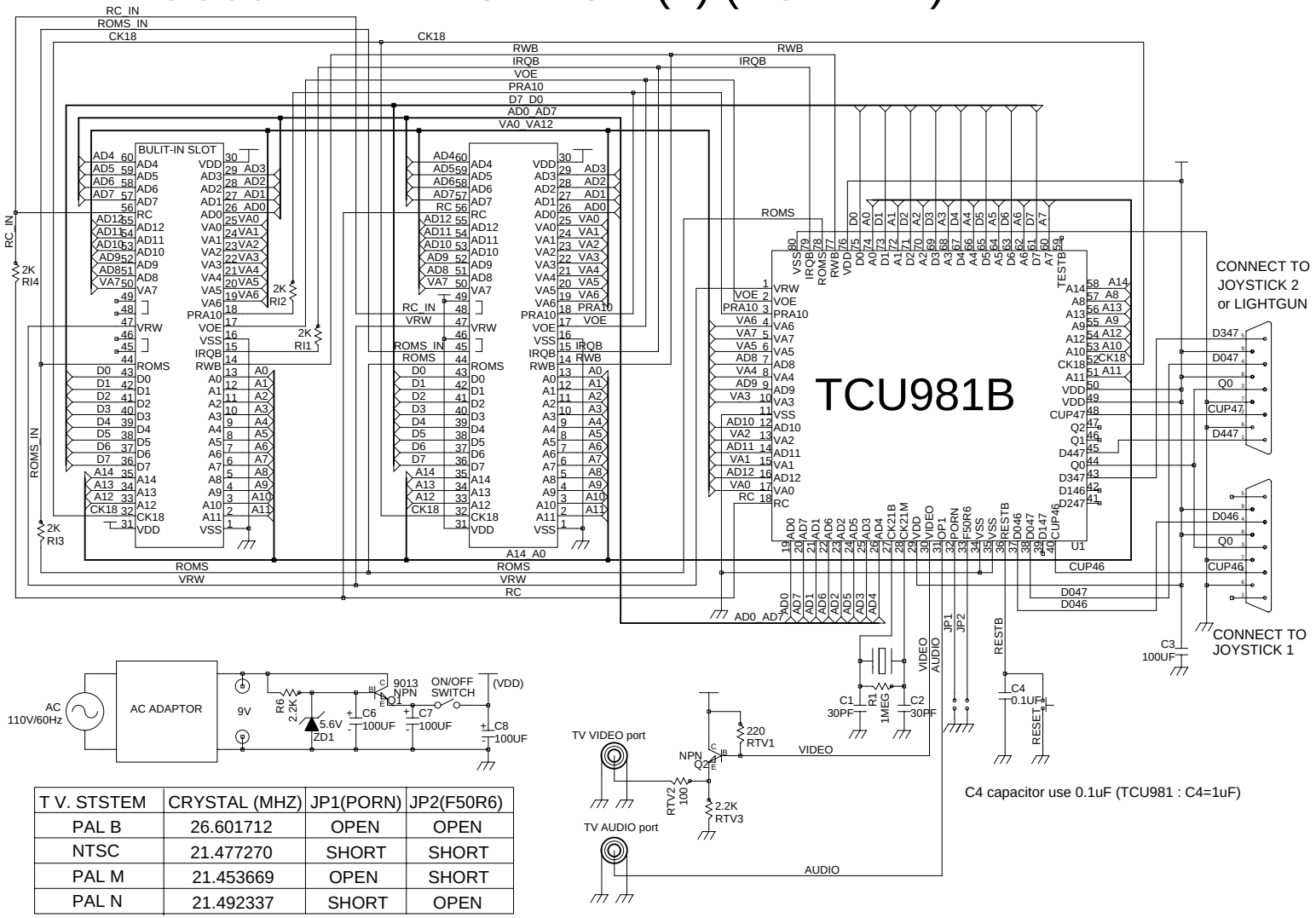


T V. STSTEM	CRYSTAL (MHZ)	JP1(PORN)	JP2(F50R6)
PAL B	26.601712	OPEN	OPEN
NTSC	21.477270	SHORT	SHORT
PAL M	21.453669	OPEN	SHORT
PAL N	21.492337	SHORT	OPEN

1** : RTV resister adjust TV screen brightness, can be not used
(RTV more small, then brightness more lightness)

2** : C4 capacitor use 0.1uF (TCU981 : C4=1uF)

TCU981B APPLICATION (2) (BUILT-IN)



T V. STSTEM	CRYSTAL (MHZ)	JP1(PORN)	JP2(F50R6)
PAL B	26.601712	OPEN	OPEN
NTSC	21.477270	SHORT	SHORT
PAL M	21.453669	OPEN	SHORT
PAL N	21.492337	SHORT	OPEN