§ PATENTEN

1. PATENT：『電流源控制及補償觸控電容感測方法及其裝置』
   PAT NO. I339356 (Taiwan)
   PAT NO. ZL 2007 1 0202087. 0 (CHINA)
2. PATENT：『具環境變化校正的電容式觸控感測裝置』
   PAT NO. M383780 (Taiwan)
   PAT NO. ZL 2010 2 0141537. 7 (CHINA)
3. PATENT：『省電型多鍵觸摸開關感測裝置』
   PAT NO. M375250 (Taiwan)
   PAT NO. ZL 2010 2 0302392. 4 (CHINA)

§ General Description:

TTP275 MCU is an easy-used 4-bit CPU base microcontroller. It contains 1984-word ROM、144-nibble RAM、timer/Counter、interrupt service 、IO control hardware、LVR and touch pad feature for specified applications. The device is also suitable for diverse simple applications in control appliance and consumer product.

§ Features:

1. Tontek RISC 4-bit CPU core
2. Total 26 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
4. advance CMOS process
5. Working memory with 1984*16 program ROM and 144*4 SRAM
6. 2-level stacks
7. Operating voltage: 5.5V~2.7V
8. System operating frequency: (at VDD=5V)
   . High-speed system oscillator (OSCH):
   - ✧ Built-in RC oscillator: 4MHz(typical) ± 5%

   .Low speed peripheral oscillator (OSCL):
   - ✧ Built-in RC oscillator: 16KHz(typical) ± 30%

9. Offer 3 IO+3 touch pad or 6 general programmable I/O
   - ✧ IO port built-in key wake-up feature enable by software setting
   - ✧ Providing external interrupt inputs

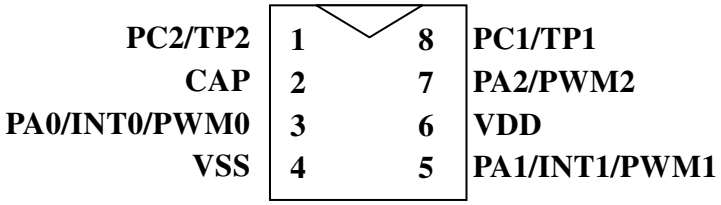
- ✧ Offering internal signal outputs, like buzzer(PWM)

10. One 8-bit TCP1 auto-reload timer/counter & onetime base counter
    - ✧ 4 timer clock sources selected by software
11. One 8-bit TCP2 auto-reload timer/counter, can improve PWM function
    - ✧ 4 timer clock sources selected by software
12. Two time base
    - ✧ Time base offers 2 various period interrupt request
13. Built-in 3 set 8-bit PWM output
14. MCU system protection and power saving controlled mode:
    - ✧ Built-in watch dog timer (WDT) circuit
    - ✧ ROM code error detection
    - ✧ Out of user program's range detection
    - ✧ Providing high/low system operating speed、sleep mode for power saving control
    - ✧ Built-in low voltage reset (LVR) function
15. 3 pins with touch pad detection
16. Provides 8 interrupt sources
    - ✧ External: INT0, INT1 shared with IO pad
    - ✧ Internal: two Timer/counter, two Time base timer
    - ✧ Two touchpad's interrupt
17. Provide package types
    - ✧ SOP 8

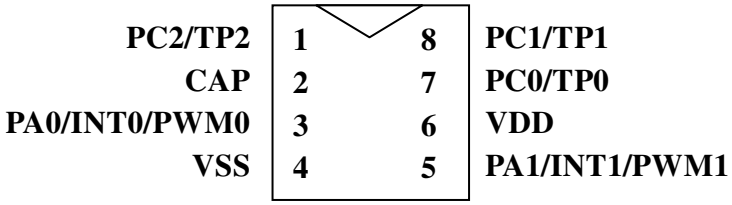
§ Applications:

1. Household electric appliances
2. Consumer products
3. Measurement controller

§ Package Description:

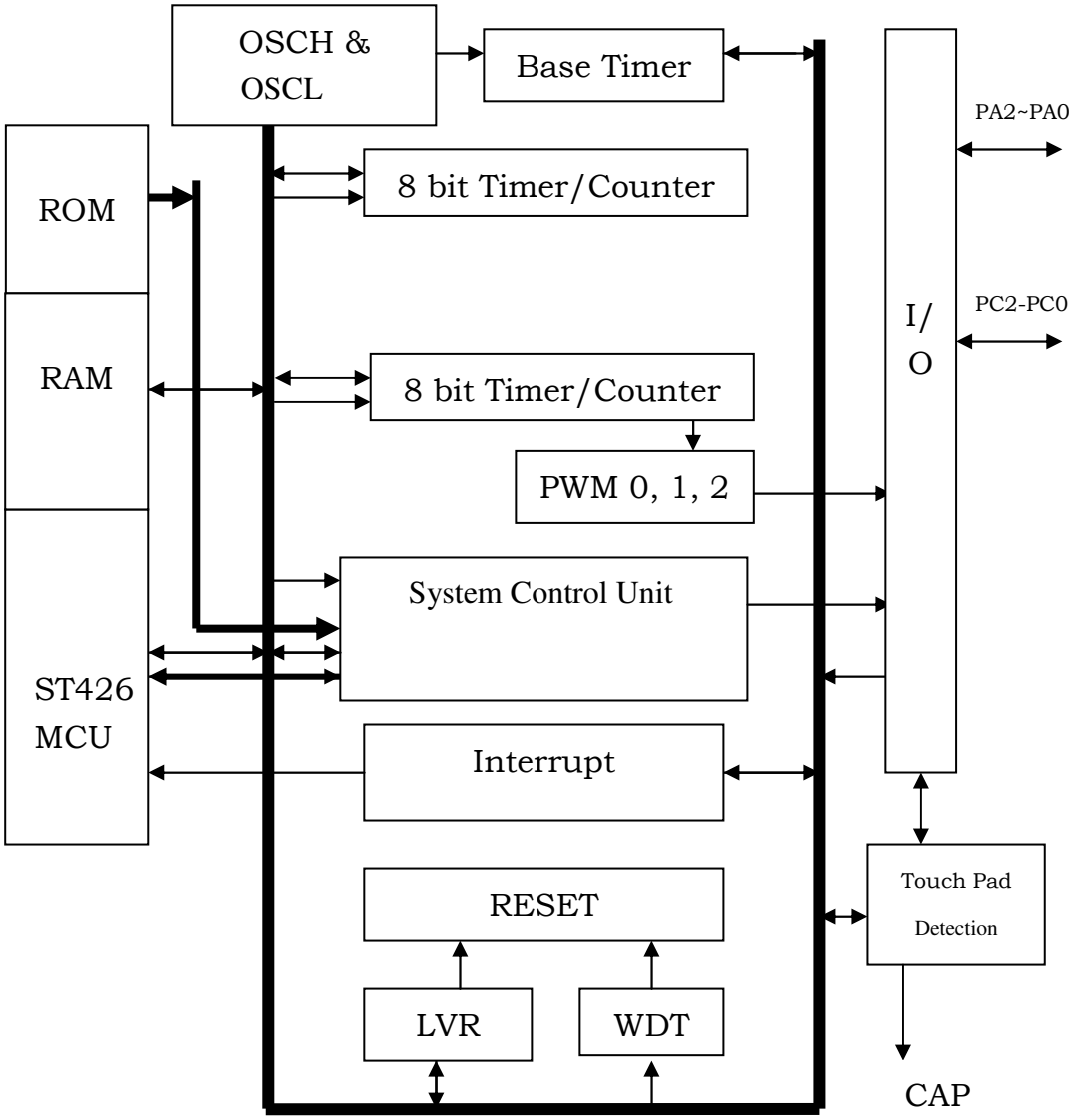


TTP275-AO8N
SOP8-A



TTP275-PO8N
SOP8-B

§ Block Diagram:



§ Pin Description:

Pin Name	Share Pin	I/O	Pin no.	Mask Option	Pin Description
V_{DD}	-	Power	+1	-	Positive power supply
V_{SS}	-	Power	+1	-	Negative power supply, ground
PA0 PA1 PA2	INT0/PWM0/VPP INT1/PWM1 PWM2	IO IO IO	+3	-	I/O port with external interrupt input and PWM output (PA0,PA1). PA2 is shared with internal PWM2 output.
PC0 PC1 PC2	TP0 TP1 TP2	IO/I IO/I IO/I	+3	-	IO port or touch pad input.
CAP	-	O	+1	-	Touch signal output
			9	-	

§ IO Cell type Description:

Pin Name	I/O Type	Description
PA0~PA1	Figure IO-C	STD IO with internal output & external input
PA2	Figure IO-B	STD IO with internal output
PC0~PC2	Figure IO-A	STD IO with external input

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-40 ~ +85	℃
Storage Temperature	Tst	-40 ~ +125	℃
OTP Supply Voltage	VPP	VSS-0.3 ~ VSS+12.5	V
Input Voltage	Vin	VSS -0.3 ~ VDD+0.3	V
Human Body Mode	ESD	>5	KV
Note: VSS symbolizes for system ground			

DC & AC Characteristics

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		2.7	-	5.5	V
Operating Current (Normal Mode, CPU working, I/O no load)	I_{nd1}	VDD=5.0V, no load, F_{OSCH}=4MHz,	-	2.5	3.0	mA
	I_{nd2}	VDD=5.0V, no load, F_{OSCL} on, F_{OSCH} off,	-	30	50	uA
Operating Current (Sleep Mode, CPU stop, I/O no load)	I_{sd1}	VDD=5.0V, no load, F_{OSCH}=4MHz,	-	0.7	1.0	mA
	I_{sd2}	VDD=3.0V, no load, F_{OSCL} on, F_{OSCH} off,	-	5	10	uA
LVR Current	I_{LVR}	VDD=5.0V	-	2	2.5	uA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
PA0 Sink Current	I_{OL}	VDD=5.0V, VOL=0.6V	-	2	-	mA
PA0 Source Current	I_{OH}	VDD=5V, VOH=VDD-0.7V	-	-1	-	mA
Output port Sink Current (exclude PA0)	I_{OL}	VDD=5.0V, VOL=0.6V	-	8	-	mA
Output Port Source Current (exclude PA0)	I_{OH}	VDD=5V, VOH=VDD-0.7V	-	-4	-	mA
I/O Port Pull-up Resistor	R_{PH}	VDD=5.0V	100	150	200	KΩ

§ AC Characteristics: (Test condition at room temperature=25°C)

Parameter	Test Condition		Min.	Typ.	Max.	Unit
External Reset	Low active pulse width tRES		2	-	-	CPU clock
Interrupt input	Low active pulse width tINT		2	-	-	
Wake up input	Low active pulse width $t_{wkup,}$ Application de-bounce should be manipulated by user' software		2	-	-	OSCL
System Oscillator Frequency	F_{OSCH} (Built-in RC)	VDD=5.0V	-	4M	-	Hz
Peripheral Oscillator Frequency	Built-in F_{OSCL}(RC)	VDD=5.0V	12K	16K	21K	Hz
Startup Period of Oscillators	T_{OSCH} (Built-in RC)	wake-up from off mode	8	-	-	F_{OSCH}
	T_{OSCL} (Built-in RC)	Wake-up from off mode	8	-	-	F_{OSCL}
Stable Time Of System Clock Switching	T_{OSCH} (Built-in RC)	OSCL→OSCH & OSCH off	8	-	-	F_{OSCH}
	(If H/L=0 then OSCH stop)					
	T_{OSCL} (Built-in RC)	OSCH→OSCL & OSCL on	8	-	-	F_{OSCL}
Timer/Counter input clock frequency	Input frequency rating, no de-bounce circuit built-in ,at VDD=5V		DC	-	4M	Hz
System Stable Time after Power up	After power up, the system needs to initialize the configured state and OST.		-	-	40	ms

§ Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~$7BF_H$	-	Program ROM [1984*16]
-	000_H ~007_H	File Registers
-	008_H~$01F_H$	Peripheral registers (I)
-	020_H~$0AF_H$	Working RAM [144*4]
-	200_H~303_H	Peripheral registers (II)

§ Interrupt Vectors:

Interrupt Vectors	Function Description
$000	hardware RESET
$001	Hardware IRQ

§ File registers:

Address	Symbol	R/W	Default	Description
000_H	(DP1)	R/W	-	Indirect addressing register
001_H	ACC	R/W	-	Accumulator & Read Table 1st data
002_H	TB1	R/W	-	Read Table 2nd data
003_H	TB2	R/W	-	Read Table 3rd data
004_H	TB3	R/W	-	Read Table 4th data
005_H	DPL	R/W	-	Data Pointer low nibble
006_H	DPM	R/W	-	Data Pointer middle nibble
007_H	DPH	R/W	-	Data Pointer high nibble

§ Peripheral registers: Interrupt request flag register

Address	Symbol	R/W	Default	Description
008_H	PS	R/W	-10-	CPU power saving control register
009_H	-	-	-	
$00A_H$	INTC	R/W	0000	Interrupt enable control register
$00B_H$	INTF	R/W	0000	Interrupt request flag register
$00C_H$	INTC1	R/W	--00	Extended interrupt enable register
$00D_H$	INTF1	R/W	--00	Extended interrupt request flag register
$00E_H$	PWMC	R/W	-000	PWM control register
$00F_H$	PWM0L	R/W	xxxx	PWM0 duty low nibble data register
010_H	PWM0H	R/W	xxxx	PWM0 duty high nibble data register
011_H	-	-	-	
012_H	PAC	R/W	-111	I/O port A control register

013_H	PA	R/W	-111	I/O port A data register
014_H	-	-	-	
015_H	-	-	-	
016_H	PCC	R/W	-111	I/O port C control register
017_H	PC	R/W	-111	I/O port C data register
018_H	-	-	-	
019_H	-	-	-	
$01A_H$	PWM1L	R/W	xxxx	PWM1 duty low nibble data register
$01B_H$	PWM1H	R/W	xxxx	PWM1 duty high nibble data register
$01C_H$	PWM2L	R/W	xxxx	PWM2 duty low nibble data register
$01D_H$	PWM2H	R/W	xxxx	PWM2 duty high nibble data register
$01E_H$	TPINTC	R/W	00--	Touchpad interrupt enable control register
$01F_H$	TPINTF	R/W	00--	Touchpad interrupt request flag register
200_H	TCP1C	R/W	0000	TCP1 Timer/counter control register
201_H	TCP1L	R/W	xxxx	TCP1 Timer/counter data low register
202_H	TCP1H	R/W	xxxx	TCP1 Timer/counter data high register
203_H	TCP2C	R/W	0000	TCP2 Timer/counter control register
204_H	TCP2L	R/W	xxxx	TCP2 Timer/counter data low register
205_H	TCP2H	R/W	xxxx	TCP2 Timer/counter data high register
206_H	PAI	R	----	Port A pad data reading address
207_H	-	-	-	
208_H	PCI	R	----	Port C pad data reading address
209_H	-	-	-	
$20A_H$	-	-	-	-
$20B_H$	-	-	-	-
$20C_H$	TCPFS	R/W	-000	TCP clock source FS pre-scale register
$20D_H$	TBC	R/W	1111	Time base control register
$20E_H$	MCKS	R/W	-111	Modulation clock selector register
$20F_H$	TPCHS0	R/W	-000	Touch pad channel selector register
210_H	-	-	-	
211_H	-	-	-	
212_H	TPCTL	R/W	-000	Touch pad control register
213_H	TPCT0	R/W	xxxx	Touch pad Duty counter 1st nibble
214_H	TPCT1	R/W	xxxx	Touch pad Duty counter 2nd nibble
215_H	TPCT2	R/W	xxxx	Touch pad Duty counter 3rd nibble
216_H	-	-	-	
217_H	-	-	-	
218_H	-	-	-	
219_H	SPCON1	R/W	-000	Special control register 1
$21A_H$	-	-	-	
$21B_H$	ADJSTAT	R	--1-	Frequency Adjustment Status flag register
$21C_H$	OSCHADJ	R/W	-001	OSCH frequency adjustment register
300_H	RESETF	R/W	0000	Reset flag
301_H	TBRB	W	xxxx	Time base counter clear address
302_H	MRO	W	xxxx	Mask option register write enable address
303_H	CLRWDT	W	xxxx	Clear WDT 2nd instruction

Note:
a. Default means initial value after power on or reset.
b. R is "read" only, W is "write" only, R/W is both of "read" & "write".

§ System function description:

S-1: System Oscillator

The high-speed oscillator is operated in built-in RC mode. Built-in RC oscillator is fixed 4MHz

S-2: Peripheral Oscillator

The low speed oscillator was built-in an internal RC oscillator that is for low power consumption consideration and fixed peripheral device timing control. Built-in RC oscillator and the frequency range between 12 KHz ~ 21 KHz.

S-3: CPU clock

The CPU clock comes from system/peripheral oscillator which was controlled by H/L bit in PS register. In the normal operation, the system clock comes from high-speed system oscillator (OSCH/2). The low speed operation frequency (OSCL/2) comes from RC oscillator.

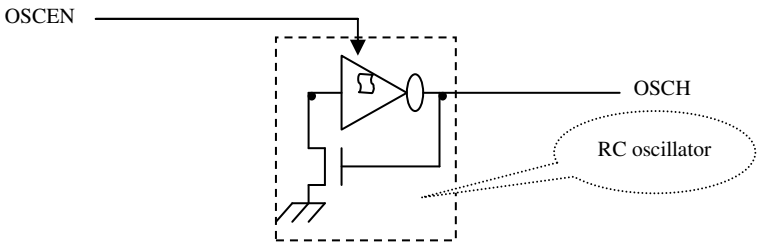


Figure: System High Speed Oscillator

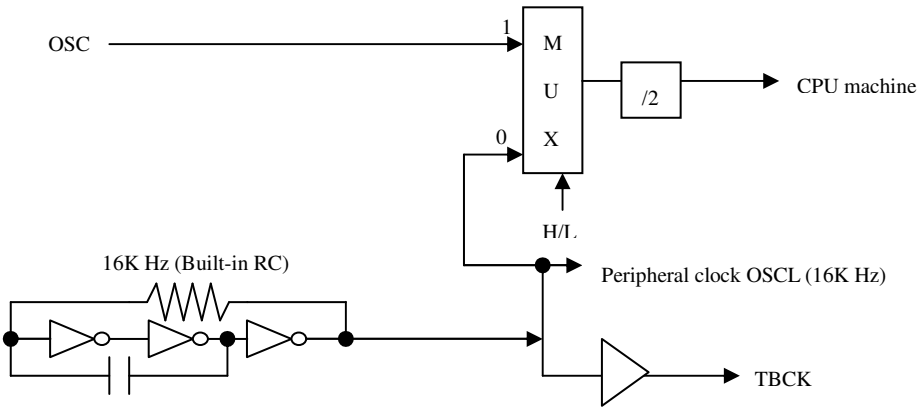


Figure: System Oscillator & CPU Clock Sources

S-4: Power saving mode (Sleep mode)

The CPU enters sleep mode is operated by writing CPU power saving register (PS). During the power saving mode, CPU holds the internal status of the system.

S-5: MCU System Operation Modes

The MCU has 3 operating modes, including high-speed operation, low speed operation, sleep modes. After power on reset, the MCU will go into high-speed operation mode automatically. After wake up from sleep mode, the MCU will resume the last operation mode.

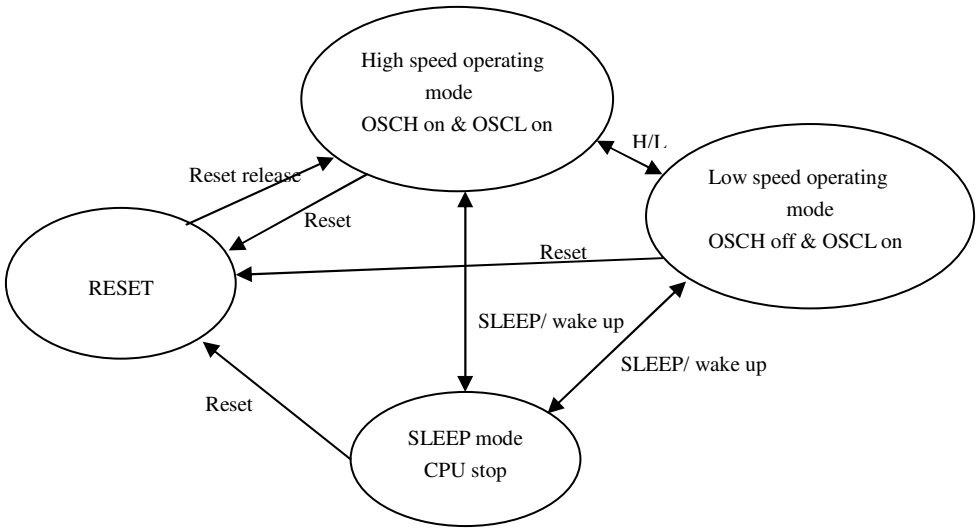


Figure: System Operation State Diagram

* Power saving mode condition & Release

Modes	Sleep mode
High speed oscillator	Stopped as H/L=0
High speed oscillator	Keep Operating as H/L=1
CPU clock	Stopped
CPU internal status	Stop & Retain the status
Memory, Flag, Register, I/O	Retain the status
Program counter	Hold the next executed address
Peripherals: Time base, Timers, Interrupts	Keep Operating
Watch Dog Timer	Disable & cleared
Release Condition	Reset, external and internal INT sources, Input Wake-up

S-6: Watch Dog Timer (WDT)

The clock of watch dog timer comes from time base 1st overflow output (TB1OV).User can use the time up signal to prevent a software malfunction or abnormal sequence from jumping to an unknown memory location causing a system fatal failure. Normally, if the watch dog timer time up signal active that will reset the chip. At the same time, program and hardware can be initialized and resume system under normal operation. The chip also provides 2 steps clear watch dog command as the programmer writes INTF with F_H data first that will enable the WDT clear, and then writes CLRWDT register after. Completely finishes the two write steps will clear the watch dog timer. User should well arrange the two command steps for avoiding the dead lock loop. Watch dog timer will be clear when reset, CPU enter sleep mode.

User should keep in minds that always clear the WDT at main program and never clear the WDT in the interrupt routine.

The maximum period of WDT =(TB1OV cycle time) * 8

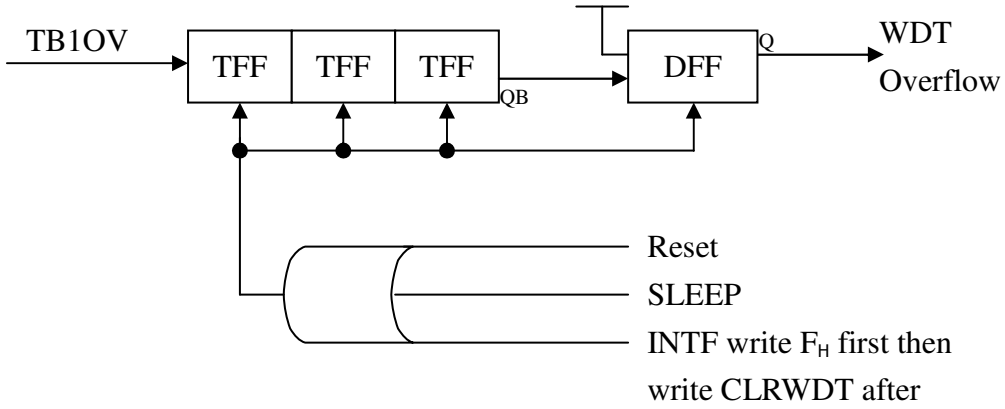


Figure: Watch Dog Timer control circuit

S-7: Low Voltage Reset (LVR)

The low voltage reset (LVR) forces the MCU in reset state during power failure, especially as MCU working in AC power application, preventing from abnormal state is the key issue. The LVR voltage is 2.7V and can not be turn off.

S-8: RESET

The chip has five kinds of reset sources: POR (power on reset), Watch dog timer reset, LVR (low voltage reset) , Burn out reset and ROM fail reset. The reset feature can be divided into 2 kind groups that one is system reset and the other is CPU reset. The system reset will initialize the CPU and peripheral device with default state. The CPU reset only initializes the CPU state and keeps the peripheral state no change.

.POR (power on reset)

The chip provides automatic reset function when the power is turned on. The VDD should be below 0.5V and its rising slope (from 0.1VDD up to 0.9VDD) needs less than 10ms.

.Watch Dog Timer Reset

The reset signal will generate automatically when the watchdog timer runs overflow. If the watchdog timer is cleared regularly by users' program, no watchdog reset will occur. Unless the MCU is forced into abnormal state, the software-controlled procedure is disrupted and causing watchdog timer overflow, then it will generate reset signal to initializes the chip returning to normal operation.

.Low Voltage Reset (LVR)

The LVR function is used to monitor the supply voltage of MCU, it will generate a reset signal (with 4*OSCL de-bounce time) to reset the microcontroller as the VDD power falls below the default setting level V_{LVR}.

.Burn out Reset (Program sequence abnormal)

As CPU out of program area, the CPU can detect the abnormal condition and generate a system reset request.

.ROM fail reset

As ROM fail, the CPU can detect the abnormal condition and generate a system reset request.

✧ RESETF[300H]: reset source flag register[R/W], power on value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	ROMF	BOF	LVRF	WDTF
Read/Write	R/W	R/W	R/W	R/W

WDTF: Watch dog timer overflow reset flag (0: no active; 1: active)
LVRF: Low voltage reset flag (0: no active; 1: active)
BOF: Burn out flag (0: no active; 1: active)
ROMF: ROM fail flag (0: no active; 1: active)
(The RESETF is cleared by power on reset)

S-9. Power saving control register

✧ PS[008H]: Power saving register[R/W] , default value [-10-]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	H/L	SLEEP	-
Read/write	-	R/W	R/W	-

SLEEP: Into sleep mode. (0: inactive; 1: active)
H/L: System clock selection. (1: System clock; 0: peripheral clock)

The SLEEP bits will be cleared to "0" automatically, when the release conditions occur from reset, interrupt, or input wake up.

S-10. OST time

The system/peripheral oscillator generates the system control timing for CPU core or peripheral devices with fixed control phase, so the waveform of oscillator becomes sensitive to noise, abnormal duty especially fatal for CPU. Any switching of clock source needs oscillation stable time (OST) to make sure the oscillation is stable and synchronized with CPU timing phase. The relative OST for different oscillator with reference value as below table:

OST	System clock(OSCH)	Peripheral clock(OSCL)
High speed SLEEP wakeup	8	-
Low speed SLEEP wakeup	-	8
Low speed to High speed	-	8

S-11. Interrupts

The CPU provides only 1 interrupt vector ($001H) and no priority, but can expand to multi-sources. Interrupt source includes external interrupts (INT0, INT1), timer/counter interrupts (TCP1,TCP2), Time base timer interrupt (TBxINT) or other peripheral device interrupt request (PERINT). The interrupt control registers (INTC or INTC1) contain the interrupt control bits to enable and disable corresponding interrupt request and the corresponding interrupt request flags in the (INTF or INTF1) registers. Before finishing the INT service routine, another INT request will keep waiting until program return from interrupt routine.

If the interrupt request needs service, the programmer may set the corresponding INT enable bit to allow interrupt active. External interrupts are triggered by both falling and rising edge trigger and set the related interrupt request flag (INTFx). The internal timer/counter interrupt is setting the TCPxF to 1, resulting from the timer/counter overflow. The time base interrupt TBxINT was provided 2 periodic interrupt request cycles for user operating a periodic routine.

When the corresponding interrupt enable and flag bits is set to 1, the CPU will active the interrupt service routine. Then CPU reads the service flag and check the request priority then proceeds with the relative interrupt service. After CPU writes the corresponding bits to 0 in the INTFx register, the service flag will be cleared to 0(using STX #n, $m instruction). The INTF & INTF1 registers' bit can only write "0" to clear the flag. User writes "1" to Flag bit with no effect.

INTC[00AH]: Interrupt control register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TB2IE	TCP2IE	TCP1IE	TB1IE
Read/Write	R/W	R/W	R/W	R/W

TB1IE: Enable time base 1st interrupt. (0: disable; 1: enable)
TCP1IE: Enable interrupt of TCP1 timer/counter. (0: disable; 1: enable)
TCP2IE: Enable interrupt of TCP2 timer/counter. (0: disable; 1: enable)
TB2IE: enable time base 2nd interrupt. (0: disable; 1: enable)

✧ INTF[00BH]: Interrupt request flag register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TB2F	TCP2F	TCP1F	TB1F
Read/Write	R/W	R/W	R/W	R/W

TB1F: Time base timer 1st interrupt request flag. (0: inactive; 1: active)
TCP1F: TCP1 Timer/counter interrupt request flag. (0: inactive; 1: active)
TCP2F: TCP2 Timer/counter interrupt request flag. (0: inactive; 1: active)
TB2F: Time base 2nd interrupt request flag. (0: inactive; 1: active)

✧ INTC1[00CH]: Extended interrupt control register [R/W], default value [--00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	INT1IE	INT0IE
Read/Write	-	-	R/W	R/W

INT0IE: enable INT0 external interrupt. (0: inactive; 1: active)
INT1IE: enable INT1 external interrupt. (0: inactive; 1: active)

✧ INTF1[00DH]: Extended interrupt request flag register [R/W], default value [--00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	INT1F	INT0F
Read/Write	-	-	R/W	R/W

INT0F: INT0 external interrupt request flag. (0: inactive; 1: active)
INT1F: INT1 external interrupt request flag. (0: inactive; 1: active)

INTxS1 INTxS0	Trigger type
00	Low active
01	Falling edge
10	Rising edge
11	Dual edge trigger

Note: INTxF Trigger type are selected by mask option

✧ TPINTC[01EH]: Touchpad interrupt control register [R/W], default value [00--]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTIE	TPCMPIE	-	-
Read/Write	R/W	R/W	-	-

TPCMPIE: Capacitor overcharge interrupt enable. (0: disable; 1: enable)
TPCTIE: Duty counter overflow interrupt enable. (0: disable; 1: enable)

✧ TPINTF[01FH]: Touchpad request flag register [R/W], default value [00--]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTF	TPCMPF	-	-
Read/Write	R/W	R/W	-	-

TPCMPF: Capacitor overcharge's flag. (0: inactive; 1: active)
TPCTF: Duty counter's overflow flag. (0: inactive; 1: active)

§ Peripheral function description:

P-1: System clock pre-scale

The system clock almost is the most high frequency of MCU. For various peripherals, application needs different clock source divided from system clock. TCPFS register is a selector for choosing suitable frequency (FS).

✧ TCPFS[20CH]: System clock pre-scale register[R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	FS2	FS1	FS0
Read/Write	-	R/W	R/W	R/W

FS2~FS0: the selector of TCPFS

FS2 ~ FS0	FS	FS2 ~ FS0	FS
0	OSCH/1	4	OSCH/16
1	OSCH/2	5	OSCH/32
2	OSCH/4	6	OSCH/64
3	OSCH/8	7	OSCH/128

OSCH: 4MHz

P-1-1: OSC Frequency Adjustment

✧ ADJSTAT[21BH]: Frequency Adjustment Status flag register [R], default value [--1-]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	OSCHADJF	-
Read/write	-	-	R	-

OSCHADJF: OSCH frequency adjustment status flag. (0: busy, 1: idle)

✧ SPCON1 [219H]: Special control register 1 [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	FST2	FST1	FST0
Read/write	-	R/W	R/W	R/W

FST2~FST0: Frequency Shift Time selector.

FST2~FST0	Frequency Shift Time (us)
000	OFF
001	4
010	6
011	8
100	12
101	24
110	32
111	64

✧ OSCHADJ [21CH]: OSCH frequency adjustment register [R/W], default value [-001]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	ADJ2	ADJ1	ADJ0
Read/write	-	R/W	R/W	R/W

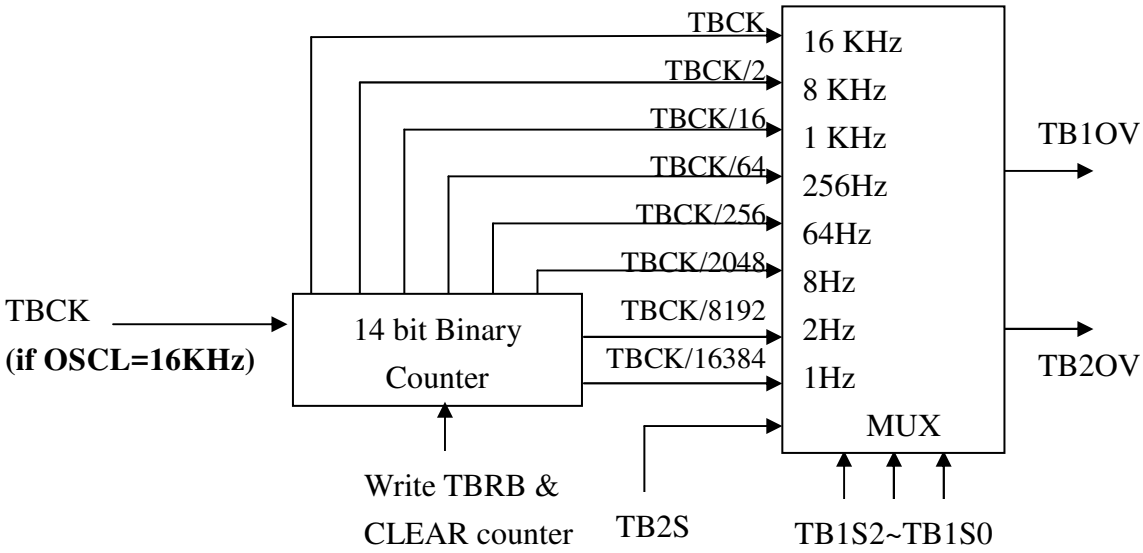
ADJ2~ADJ0: OSCH frequency adjustment data.

ADJ2~ADJ0	OSCH frequency adjustment data
001	±1
010	±2
011	±3
100	±4
101	±5
110	±6
111	±7

OSCHADJ set the frequency swing range, when the change time in register FST is set, frequency shift function will be activated. Swing shift back and forth from the center frequency. Set FST=0 to off frequency shift function. When frequency shift function is executing, OSCHADJF will be set 0. Then user can not change OSCHADJ and FST, but only can be set 0 to off function. Frequency shift function will not immediately stop, when FST is set to 0, the need to wait until the frequency back to the original frequency, while OSCHADJF will be set to 1.

P-2: Time Base Counter

The time base counter has 2 interrupt sources and both of them come from the peripheral internal RC oscillator. The time base 1st overflow output (TB1OV) can cause interrupt and the period is selected by TB1S2~TB1S0 in TBC register. The time base 2nd overflow output (TB2OV) also offers two sample frequency options by TB2S bit in the TBC register.



✧ TBC[20DH]: Time base control register[R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TB2S	TB1S2	TB1S1	TB1S0
Read/Write	R/W	R/W	R/W	R/W

TB1S2 ~ TB1S0: Base timer1 overflow frequency selection bits.
TB2S: Base timer2 overflow frequency selection (0: 32Hz; 1:16Hz)
(Every time writing the TBRB will clear the time base counter)

TB2S	**Base timer overflow frequency (TB1OV)**	**TB2OV (if OSCL=16KHz)**
0	TBCK/512	32Hz
1	TBCK/1024	16Hz

TB1S2	**TB1S1**	**TB1S0**	**Base timer overflow frequency (TB1OV)**	**TB1OV (if OSCL=16KHz)**
0	0	0	TBCK	16KHZ
0	0	1	TBCK/2	8KHZ
0	1	0	TBCK/16	1KHZ
0	1	1	TBCK/64	256HZ
1	0	0	TBCK/256	64 HZ
1	0	1	TBCK/2048	8HZ
1	1	0	TBCK/8192	2HZ
1	1	1	TBCK/16384	1HZ

P-3: 8 bits Timer/Counter (TCP) for TCP1

One 8-bit timer/counters (TCP) with 4 kind clock sources and preload data buffer can implement as a timer or counter feature. The clock sources of TCP1 are selected by TCP1S0 & TCP1S1 two bits of the timer control registers (TCP1C). TCP1OV is the timer or counter overflow signal and the rising edge will set the relative INT flag.

✧ TCP1C[200H]: TCP1 Timer/counter control register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP1LD	TCP1S1	TCP1S0	TCP1EN
Read/Write	R/W	R/W	R/W	R/W

TCP1EN: TCP1 counting enabled. (0: disable; 1: enable)
TCP1LD: TCP1 auto-reload enabled. (0: disable; 1: enable)
TCP1S1 & TCP1S0: TCP1 clock source selection bits.

TCP1S1	TCP1S0	Selected Clock source
0	0	FS
0	1	OSCH
1	0	TBCK
1	1	TB1OV

✧ TCP1L[201H]: TCP1 low nibble data register[R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP1_3/TCP1D3	TCP1_2/TCP1D2	TCP1_1/TCP1D1	TCP1_0/TCP1D0
Read/Write	R/W	R/W	R/W	R/W

TCP1_3~TCP1_0: reading the counter low nibble data.
TCP1D3~TCP1D0: writing TCP1D low nibble of data buffer.

✧ TCP1H[202H]: TCP1 high nibble data register[R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP1_7/TCP1D7	TCP1_6/TCP1D6	TCP1_5/TCP1D5	TCP1_4/TCP1D4
Read/Write	R/W	R/W	R/W	R/W

TCP1_7~TCP1_4: reading the counter high nibble data.
TCP1D7~TCP1D4: writing TCP1D high nibble of data buffer.

* TCP1D: Like a 8 bit TCP1 data register[R/W], default value [xxH]

TCP1D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP1D7	TCP1D6	TCP1D5	TCP1D4	TCP1D3	TCP1D2	TCP1D1	TCP1D0

The special R/W function for TCP1 has different Target, AS writing TCP1H/L registers that are updating preload data of the TCP1D. As read TCP1H/L registers that are the brand new TCP1 counter value.

P-4: 8 bits Timer/Counter/PWM for TCP2

One 8-bit timer/counters (TCP2) with 4 kind clock sources and preload data buffer can implement as a timer or counter feature. The clock sources of TCP2 are selected by TCP2S0 & TCP2S1 two bits of the timer control registers (TCP2C). TCP2OV is the timer or counter overflow signal and the rising edge will set the relative INT flag.

✧ TCP2C[203H]: TCP2 Timer/counter/PWM control register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP2LD	TCP2S1	TCP2S0	TCP2EN
Read/Write	R/W	R/W	R/W	R/W

TCP2EN: TCP2 counting enabled. (0: disable; 1: enable)
TCP2LD: TCP2 auto-reload enabled. (0: disable; 1: enable)
TCP2S1 & TCP2S0: TCP2 clock source selection bits.

TCP2S1	TCP2S0	Selected Clock source
0	0	FS
0	1	OSCH
1	0	TBCK
1	1	TCP1OV

✧ TCP2L[204H]: TCP2 low nibble data register[R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP2_3/TCP2D3	TCP2_2/TCP2D2	TCP2_1/TCP2D1	TCP2_0/TCP2D0
Read/Write	R/W	R/W	R/W	R/W

TCP2_3~TCP2_0: reading the counter low nibble data.
TCP2D3~TCP2D0: writing TCP2D low nibble of data buffer.

✧ TCP2H[205H]: TCP2 low high data register[R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP2_7/TCP2D7	TCP2_6/TCP2D6	TCP2_5/TCP2D5	TCP2_4/TCP2D4
Read/Write	R/W	R/W	R/W	R/W

TCP2_7~TCP2_4: reading the counter high nibble data.
TCP2D7~TCP2D4: writing TCP2D high nibble of data buffer.

* TCP2D: Like a 8 bit TCP2 data register[R/W], default value [xxH]

TCP2D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP2D7	TCP2D6	TCP2D5	TCP2D4	TCP2D3	TCP2D2	TCP2D1	TCP2D0

The special R/W function for TCP2 has different Target, AS writing TCP2H/L registers that are updating preload data of the TCP2D. As read TCP2H/L registers that are the brand new TCP2 counter value.

P-5: 16-bit Timer/Counter (TCP1 and TCP2 cascade)

Two sets TCP can be cascaded to form a 16-bit timer/counter when TCP2 chooses TCP1OV as clock source (TCP2S1=1 and TCP2S0=1). In the 16-bit timer application, user should use TCP1EN to control the starting or stopping counting of 16-bit timer/counter, data load is controlled by writing TCP1EN=1. The rising TCP2OV will reload the contents in the preload register into timer/counter if TCP2LD=1. The interrupt feature is different, in this case, the TCP1 interrupt will be inhibit when TCP1OV occur, the TCP2 interrupt is normally.

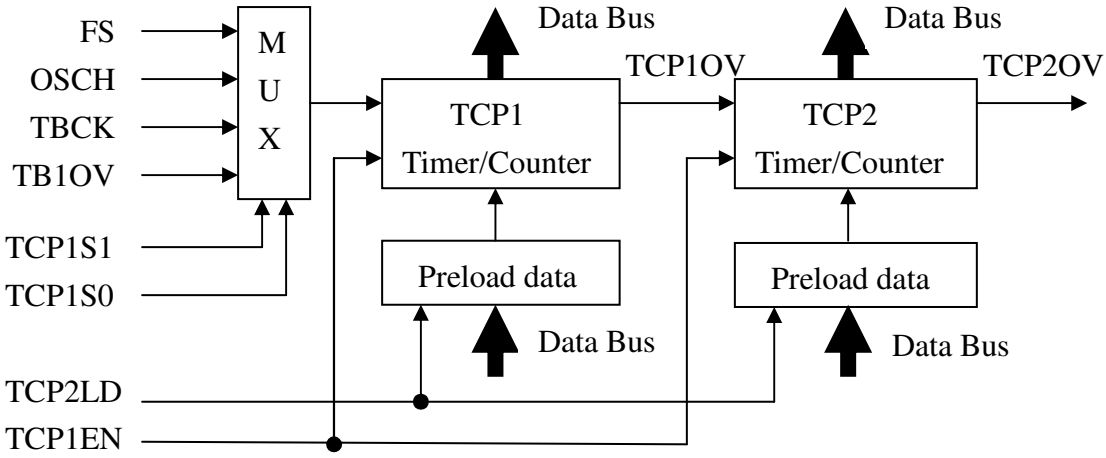


Figure: 16-bit Timer/Counter (TCP1 and TCP2 cascade)

.Timer

When TCPx works as a Timer, user needs give the preload data TCPxD for periodic interrupt. After initial setting, user starts the TCPx counting by setting TCPxEN=1, the TCPx cycle period is:

Tc = (selected clock cycle) * (256) if TCPxD=00H

Tc = (selected clock cycle) * (TCPxD) otherwise

When 16 bits timer/counter:

Tc = (selected clock cycle) * (65536) if TCP1D=00H & TCP2D=00H

Tc = (selected clock cycle) * (TCP2D*256+TCP1D) otherwise

When user writes data to the TCPxD, the data just keep in TCPxL/H. During the TCPxEN=1 command executed, the TCPxD's complement value will load

into counter TCPx as initial value and start the timer function. Necessary TCPxLD=1, timer run with reload feature as TCPx up counts and reaches the value of "FF_H" or 255 for TCPx. At the same time, interrupt request flag TCPxF will set activated, if software enables the corresponding interrupt enable bit, INT hardware will cause MCU interrupt service routine.

.Counter

Counter feature is implemented only by TCPxLD=0, the TCPxD can be zero or not that depends on software needs. User starts and stops the counter by changing the TCPxEN bit value. On the save side, reading the counter value after stopping the count by disable TCPxEN=0, if reading the counter value during value changing that means clock in happening at the same time. The reading of counter value may disrupt for transient state. If counter is not enough for counting, user can enable the interrupt and using the data RAM as software counter for extending the counter stage.

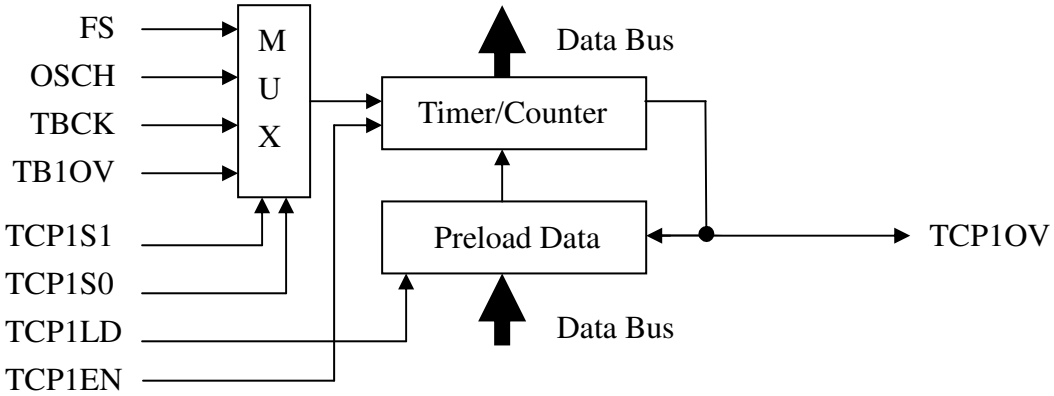


Figure: 8-bit Timer/Counter (TCP1)

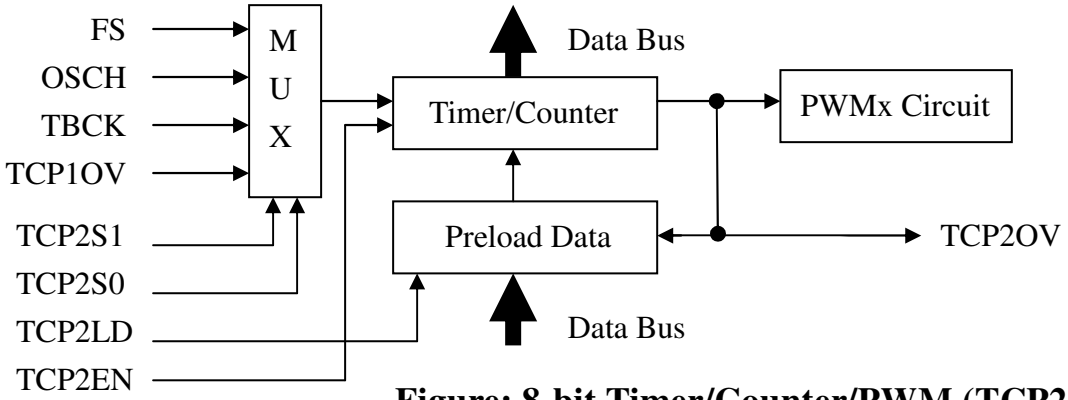


Figure: 8-bit Timer/Counter/PWM (TCP2)

TCP1S1~TCP1S0	TCP1 clock source
00	FS
01	OSCH
10	TBCK
11	TB1OV

TCP2S1~TCP2S0	TCP2 clock source
00	FS
01	OSCH
10	TBCK
11	TCP1OV

	PWM Output
TCP2	PWM0,1,2

FS: Clock scaled frequency comes from OSCH.
OSCH: Bulit-in high frequency RC oscillator 4MHz.
TBCK: Peripheral clock source, 16KHz in the RC mode.
TB1OV: Time base 1st overflow output.
TCP1OV: TCP1 overflow output.
PWM0~2: TCP2 cycle time with PWMxD duty output signal.

.PWM

The PWM period generated from TCP2. When PWMxEN (PWMC<0> or PWMC<1> or PWMC<2>) enable, and PWMOUT pin (PA0, PA1, or PA2 the PAx must be output mode and select normal IO by mask option) change to output mode, PWMx signal will output to PWMOUT pin.

The duty of PWMx value is store in PWMxL and PWMxH, user write PWMxH first, last write PWMxL. When write the PWMxL the 8 bits duty value will be load to PWMxD at the same time. PWM's duty value cannot bigger than TCP2 pre-load data. If not, PWMOUT is an unexpected signal.

User can select PWMOUT pin start with 1 or start with 0 by option. When TCP2 enable, timer start increment, if timer/counter value bigger than PWM's duty value, PWMOUT will change state. The PWMOUT back to start state, When TCP2 is overflow.

User does not use PWM in 16 bits timer/counter mode. If not, PWMOUT is an unexpected signal.

User does not use TCP2D=00H. If not, PWMOUT is an unexpected signal.

✧ PWMC[00EH]: PWM control register[R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	PWM2EN	PWM1EN	PWM0EN
Read/Write	-	R/W	R/W	R/W

PWM0EN: PWM0 output enabled. (0: disable; 1: enable)
PWM1EN: PWM1 output enabled. (0: disable; 1: enable)
PWM2EN: PWM2 output enabled. (0: disable; 1: enable)

✧ PWM0L[00FH]: PWM0 duty low nibble data register[R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM0D3	PWM0D2	PWM0D1	PWM0D0
Read/Write	R/W	R/W	R/W	R/W

PWM0D3~0: PWM0 duty low nibble data

✧ PWM0H[010H]: PWM0 duty high nibble data register[R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM0D7	PWM0D6	PWM0D5	PWM0D4
Read/Write	R/W	R/W	R/W	R/W

PWM0D7~4: PWM0 duty high nibble data

✧ PWM1L[01AH]: PWM1 duty low nibble data register[R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM1D3	PWM1D2	PWM1D1	PWM1D0
Read/Write	R/W	R/W	R/W	R/W

PWM1D3~0: PWM1 duty low nibble data

✧ PWM1H[01BH]: PWM1 duty high nibble data register[R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM1D7	PWM1D6	PWM1D5	PWM1D4
Read/Write	R/W	R/W	R/W	R/W

PWM1D7~4: PWM1 duty high nibble data

✧ PWM2L[01CH]: PWM2 duty low nibble data register[R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM2D3	PWM2D2	PWM2D1	PWM2D0
Read/Write	R/W	R/W	R/W	R/W

PWM2D3~0: PWM2 duty low nibble data

✧ PWM2H[01DH]: PWM2 duty high nibble data register[R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM2D7	PWM2D6	PWM2D5	PWM2D4
Read/Write	R/W	R/W	R/W	R/W

PWM2D7~4: PWM2 duty high nibble data

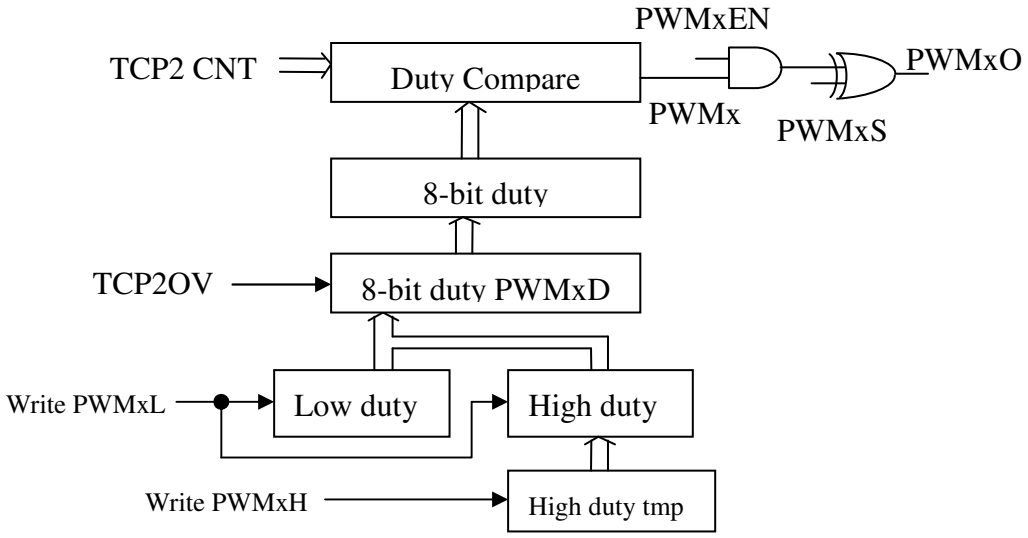


Figure: PWM (TCP2)

PWMxD	PWM duty	Note
0	(0 * clock cycle) / TCP2 timer's period	All off
1	(1 * clock cycle) / TCP2 timer's period	
2	(2 * clock cycle) / TCP2 timer's period	
….	….	
n	((n) * clock cycle) / TCP2 timer's period	
….	….	
TCP2D	((TCP2D) * clock cycle) / TCP2 timer's period	All on

Note:
1. PWMxD cannot bigger than TCP2D
2. TCP2 timer's period = (TCP2D) * clock cycle.
3. PWM can start 0 or start 1 by option.

Table: PWM duty

. I/O PAD Cell Structure & Function Description

.. IO port with touch pad input

The input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control register=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. Software can performs a configuration (output data register=0, changing the IO control register to 0 or 1) for open drain type that specifies suitable for key scan application. An additional feature supports the touch pad input.

Extern input	IO control data	Output data	Pull-up R	Wake-up feature
Disable	0	X	No	No
Disable	1	0	No	No
Disable	1	1	Enable	Enable
Enable and touch pad scan	X	X	No	No

X: don't care the value.

IO control data	IO pad
0	Output register data
1	IO pad input data

Read PxI	Read input data
1	IO pad data

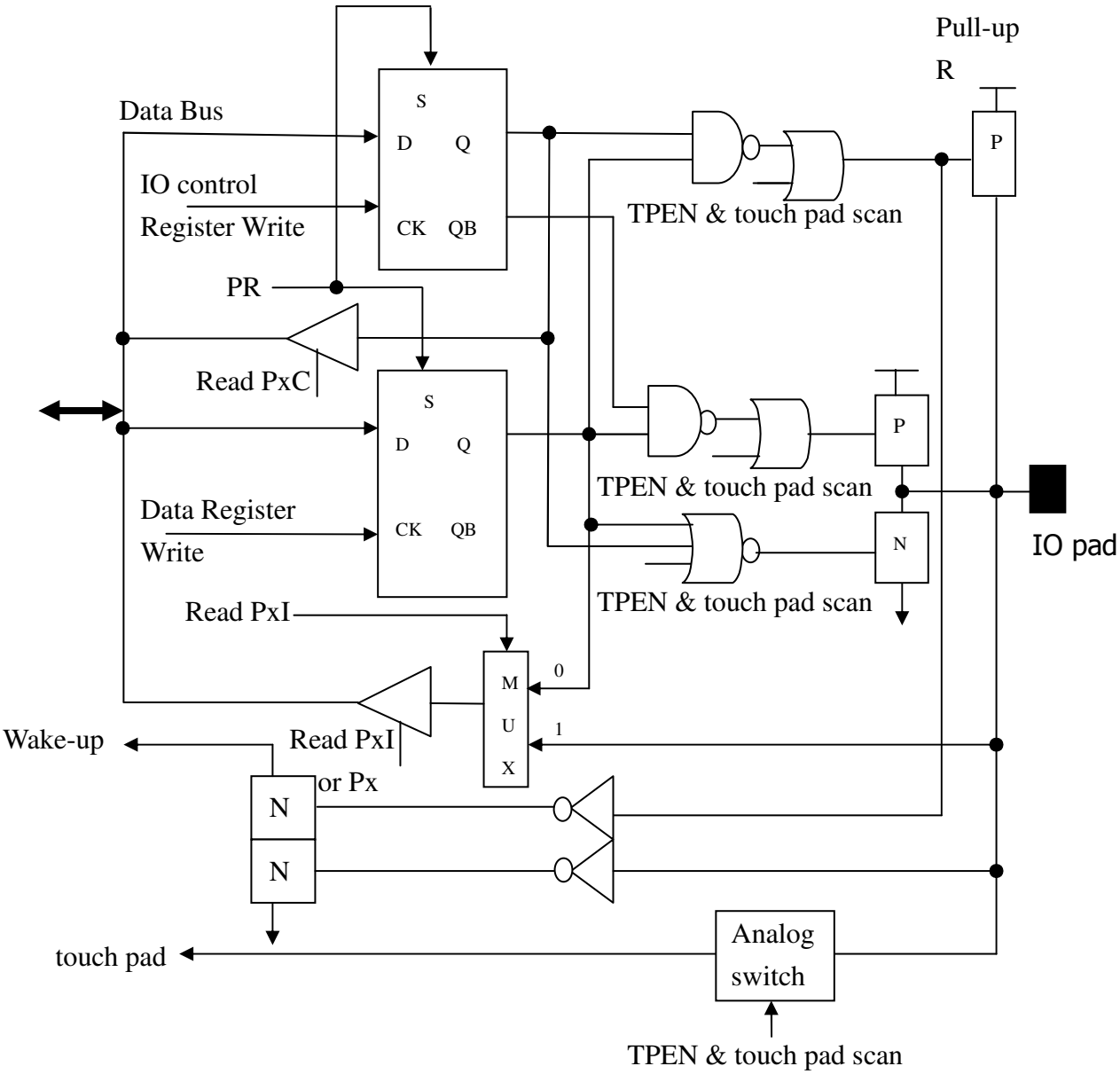


Figure IO-A: Standard IO port with touch pad input

.. IO port with internal PWM output

The standard input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control data=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. If enable internal output, the IO port must set as output (IO control data=0). An additional feature supports the internal PWM output.

IO control data	Output data	Pull-up R	Wake-up feature
0	X	No	No
1	0	No	No
1	1	Enable	Enable

X: don't care the value.

IO control data	Internal output	IO pad
0	Enable	Output internal data
0	Disable	Output register data
1	X	IO pad input data

X: don't care the value.

Read PxI	Read input data
1	IO pad data

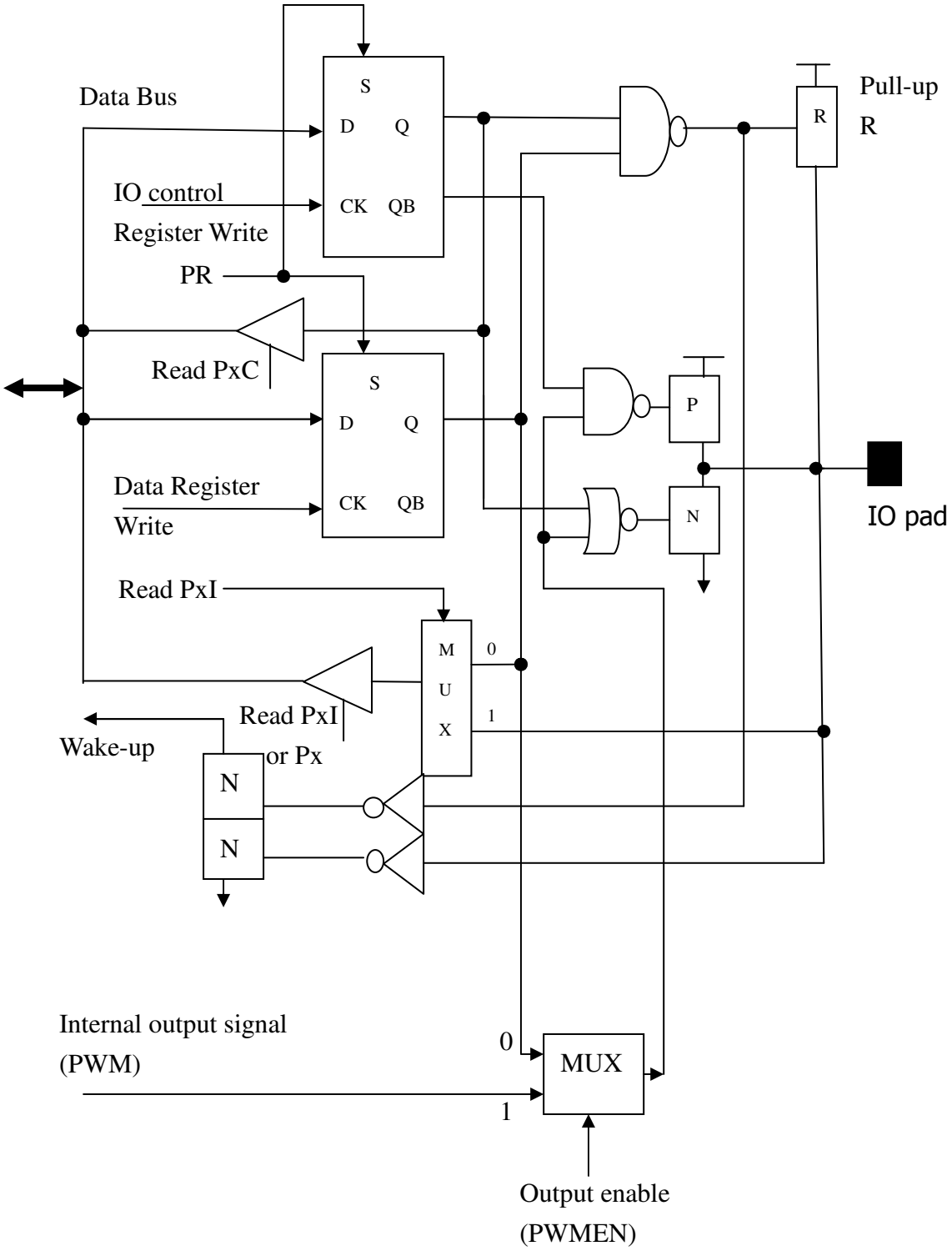


Figure IO-B: Standard IO port with internal PWM output

.. IO port with internal PWM output and external interrupt trigger input

The standard input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control data=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. If enable internal output, the IO port must set as output (IO control data=0). An additional feature supports the internal PWM output and external interrupt trigger input.

IO control data	Output data	Pull-up R	Wake-up feature	External input
0	X	No	No	No
1	0	No	No	Enable
1	1	Enable	Enable	Enable

X: don't care the value

IO control data	Internal output	IO pad
0	Enable	Output internal data
0	Disable	Output register data
1	X	IO pad input data

X: don't care the value.

Read PxI	Read input data
1	IO pad data

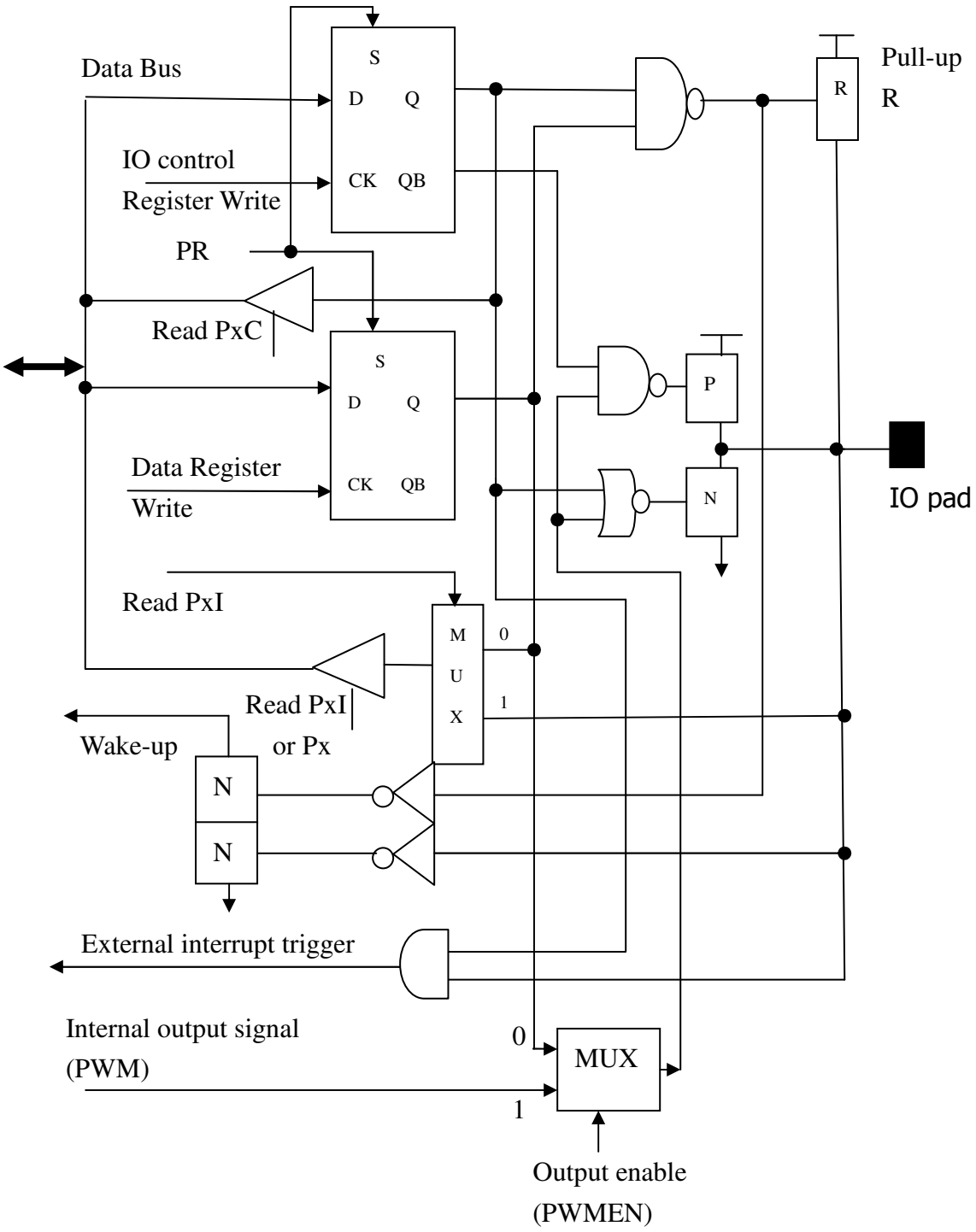


Figure IO-C: Standard IO port with internal PWM output and external interrupt trigger input

3. I/O Pad Cells

The main features of pad cell are including ESD/EFT protection and general I/O access. A general I/O pad cell can be configured as input with or without pull-up resistor, or working as a CMOS or NMOS output driver. The input pad cell must have pull-up resistor for avoiding a floating state when user doesn't care or not be used. For concerning the standby current, user can use data register or I/O control register to fit the application.

. I/O File Register

✧ PAC[012H]: Port A I/O control register [R/W], default value [-111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	PAC2	PAC1	PAC0
Read/Write	-	R/W	R/W	R/W

PAC2~PAC0: port A I/O control data

✧ PA[013H]: Port A data register [R/W], default value [-111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	PA2	PA1	PA0
Read/Write	-	R/W	R/W	R/W

PA2~PA0: port A data

✧ PCC[016H]: Port C I/O control register [R/W], default value [-111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	PCC2	PCC1	PCC0
Read/Write	-	R/W	R/W	R/W

PCC2~PCC0: port C I/O control data

✧ PC[017H]: Port C data register [R/W], default value [-111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	PC2	PC1	PC0
Read/Write	-	R/W	R/W	R/W

PC2~PC0: port C data

✧ PAI[206H]: Port A pad data reading address [R], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	PAI2	PAI1	PAI0
Read/Write	-	R	R	R

PAI2~PAI0: port A pad data

✧ PCI[208H]: Port C pad data reading address [R], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	PCI2	PCI1	PCI0
Read/Write	-	R	R	R

PCI2~PCI0: port C pad data

3 non-contact inputs touch pad detector

The touch pad detector applies the charge sharing conception. The inputs share the pad with IO ports. Built-in charge sharing control, duty detector and de-bounce feature can response the input with varied output refresh rate that dependant on the system request. For power saving concern, auto power off function and wake up de-bounce capability can support a lower average operating current.

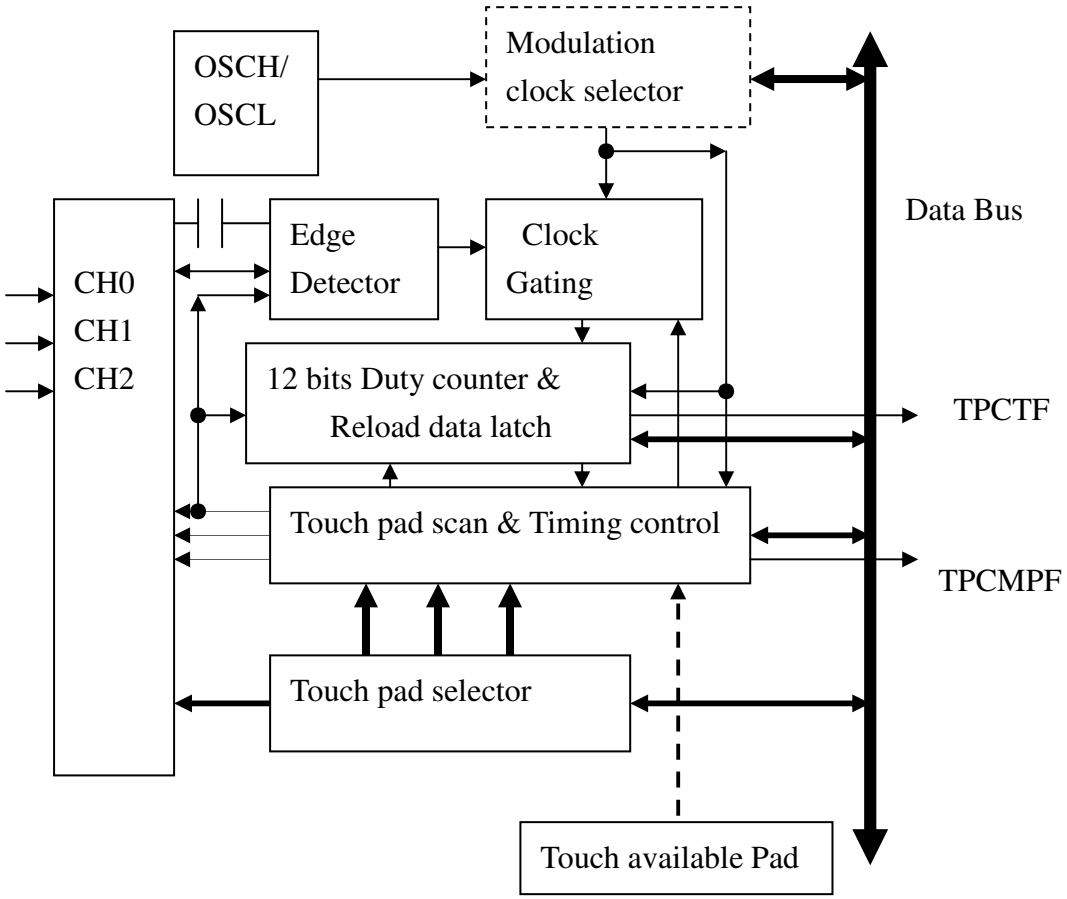
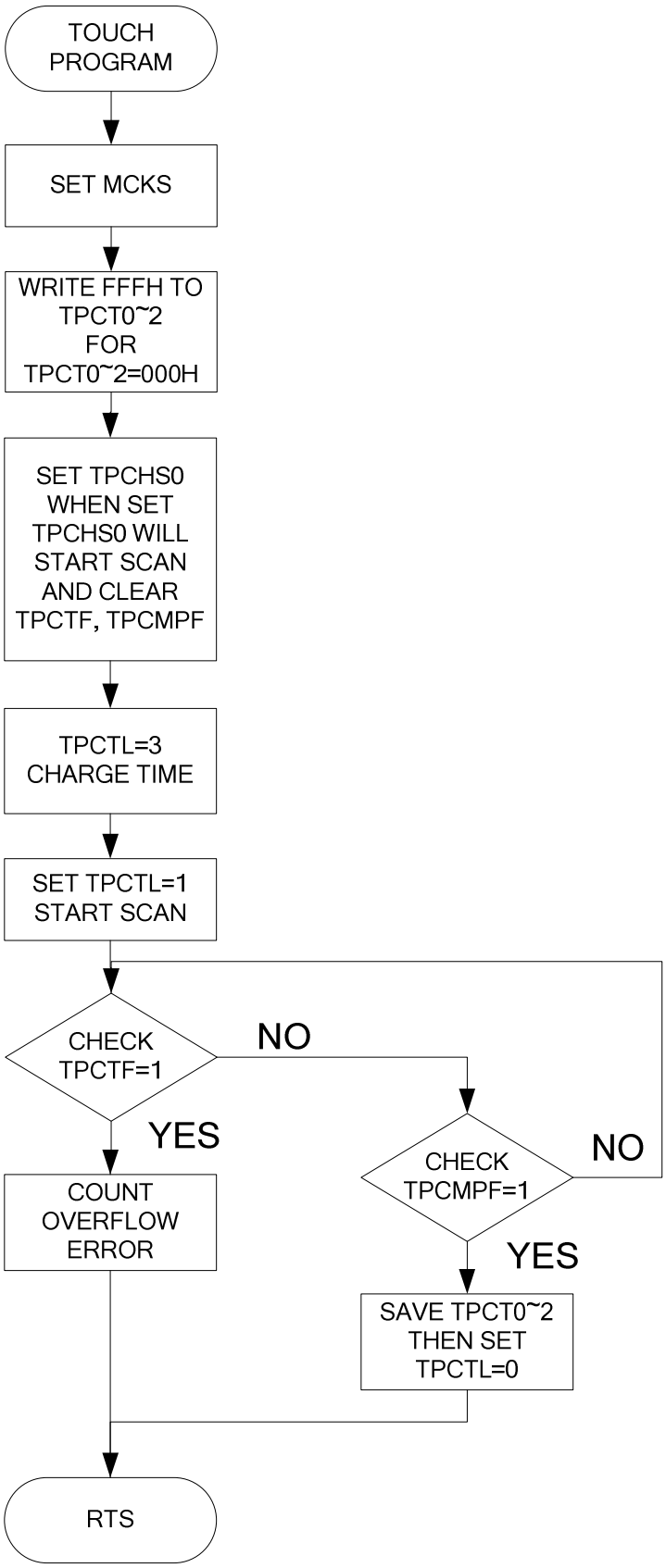


Figure: 3 keys Touch pad detector

Parameters	Target value	Remark
Touch pad clock	OSCH or OSCL	4MHz or 16KHz (typical)
Modulation clock	OSCH/N or OSCL	N=1,2,4,8,16,32,64
Duty counter	12 bits	With INT
Reload data latch	12 bit	Write only
Touch pads	1~3 keys	Mask option
Key de-bounce time	s/w implements	By application or cover thickness
Sensitivity level	Offset value by s/w	Resolution=1 modulation clock

The flowchart as follow:



✧ TPINTC[01EH]: Touchpad interrupt control register [R/W], default value [00--]

TPINTC	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTIE	TPCMPIE	-	-
Read/Write	R/W	R/W	-	-

TPCMPIE: Capacitor overcharge interrupt enable. (0: disable; 1: enable)
TPCTIE: Duty counter overflow interrupt enable. (0: disable; 1: enable)

✧ TPINTF[01FH]: Touchpad request flag register [R/W], default value [00--]

TPINTF	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTF	TPCMF	-	-
Read/Write	R/W	R/W	-	-

TPCMPF: Capacitor overcharge's flag. (0: inactive; 1: active)
TPCTF: Duty counter's overflow flag. (0: inactive; 1: active)

✧ TPCT0[213H]: Touch pad duty counter & latch data register 0 [R], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCT3/CT3	TPCT2/CT2	TPCT1/CT1	TPCT0/CT0
Read/Write	R/W	R/W	R/W	R/W

TPCT3~TPCT0: Duty counter 1st nibble for counter read
CT3~CT0: 1st nibble of reload latch data

✧ TPCT1[214H]: Touch pad duty counter & latch data register 1 [R], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCT7/CT7	TPCT6/CT6	TPCT5/CT5	TPCT4/CT4
Read/Write	R/W	R/W	R/W	R/W

TPCT7~TPCT4: Duty counter 2nd nibble for counter read
CT7~CT4: 2nd nibble of reload latch data

✧ TPCT2[215H]: Touch pad duty counter & latch data register 2 [R], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCT11/CT11	TPCT10/CT10	TPCT9/CT9	TPCT8/CT8
Read/Write	R/W	R/W	R/W	R/W

TPCT11~TPCT8: Duty counter 3rd nibble for counter read
CT11~CT8: 3rd nibble of reload latch data

Duty counter value= TPCT2*256 +TPCT1*16+TPCT0

The duty counter will be enabled by writing the TPCHS0 register and will set the TPCTF flag if duty counter overflow. As writing any of the TPCHS0 addresses will reload the 12 bit counters and clear the TPCTF & TPCMPF.

✧ MCKS[20EH]: Modulation clock selector register [R/W], default value [-111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	MCKS2	MCKS1	MCKS0
Read/Write	-	R/W	R/W	R/W

MCKS2~MCKS0: Modulation clock selector

MCKS2 ~ MCKS0	Sample time	MCKS2 ~ MCKS0	Sample time
000	OSCH/1	100	OSCH/16
001	OSCH/2	101	OSCH/32
010	OSCH/4	110	OSCH/64
011	OSCH/8	111	OSCL

The TPCMPF will be set as no modulation clock going into duty counter with de-bounce feature and will also call the interrupt as TPCMPIE=1 .

✧ TPCHS0[20FH]: Touch pad channel selector register0 [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	TPEN2	TPEN1	TPEN0
Read/Write	-	R/W	R/W	R/W

TPEN2~TPEN0: Touch pad channel selector 1st nibble

As program writes the TPCHS0 register hardware automatically discharges the external capacitor and enables the sensor clock input until period end.

Channel Enable State	TPCHS0 TPEN2~0
TP0	001
TP1	010
TP2	100

When TPCHS0 is writing, TPCTL will be set TP RUN mode, and touchpad begin to scan touchpad

Users can enable multi-channel by setting corresponding bit 1, which will turn on all enable channel at the same time.

✧ TPCTL[212H]: Touch pad control register [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	TPCTL2	TPCTL1	TPCTL0
Read/Write	-	R/W	R/W	R/W

TPCTL2~TPCTL0: Touch pad control selector

As program writes the TPCTL register hardware automatically discharges the external capacitor and enables the sensor clock input until period end.

TPCTL2 ~ TPCTL0	Channel Enable State
000	TP STOP
001	TP RUN
010	-
011	Discharge
100	-
101	-
110	-
111	-

TP STOP: STOP the touch pad feature and release pad for IO port
TP RUN: TP RUN is touchpad scan start signal, its scan the channel by TPCHS0 select.
Charge: Charge can hold touchpad in charge state, to avoid charge time too short.

As touch pad analog switch keeps on, the relative IO port should be disabled as tri-state by hardware.

In user selection table, the available touch pads will be generated a ROM code in option ROM.

§ Mask Option Table:

All the OTP mask option register can open for user to reset the initial value, but should enable the MRO. User writes MRO address first then changes the target mask option register data. The MRO enable will be cleared with other writing address.

✧ MOP1: PWM start level option register [R/W], default value [-000]

Mask option	Bit3	Bit2	Bit1	Bit0
Bit Name	-	PWM2S	PWM1S	PWM0S
Read/Write	-	R/W	R/W	R/W

✧ MOP2: INT trigger option register [R/W], default value [0000]

Mask option	Bit3	Bit2	Bit1	Bit0
Bit Name	INT1S1	INT1S0	INT0S1	INT0S0
Read/Write	R/W	R/W	R/W	R/W

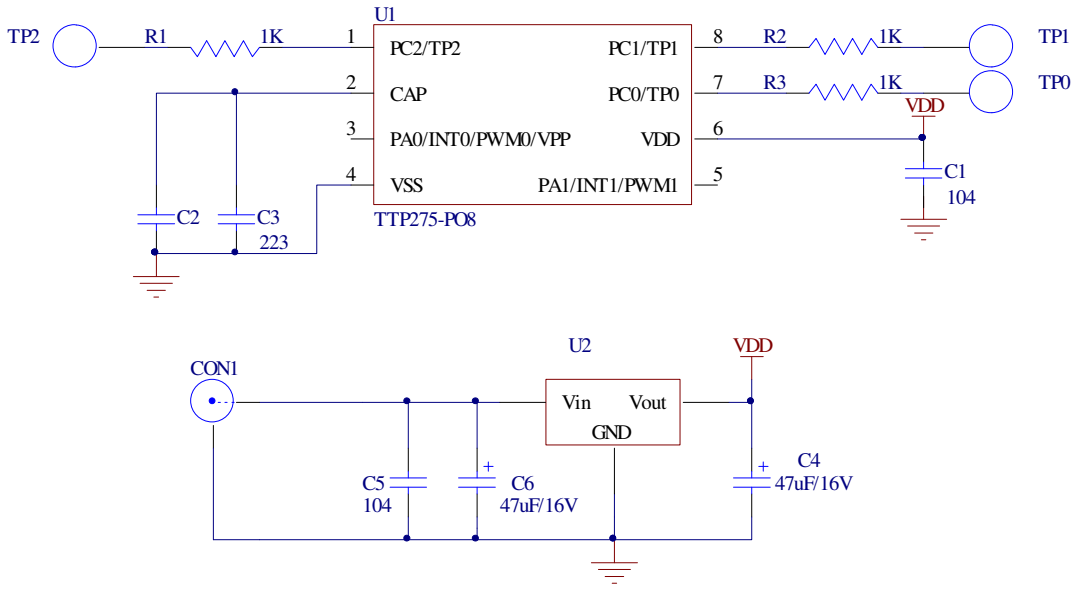
✧ MOP5: Touch pad pin option register [R/W], default value [---0]

Mask option	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	TPNIS
Read/Write	-	-	-	R/W

The following table shows the mask option in this chip. All the mask options must be defined clearly and ensure to meet user's proper function.

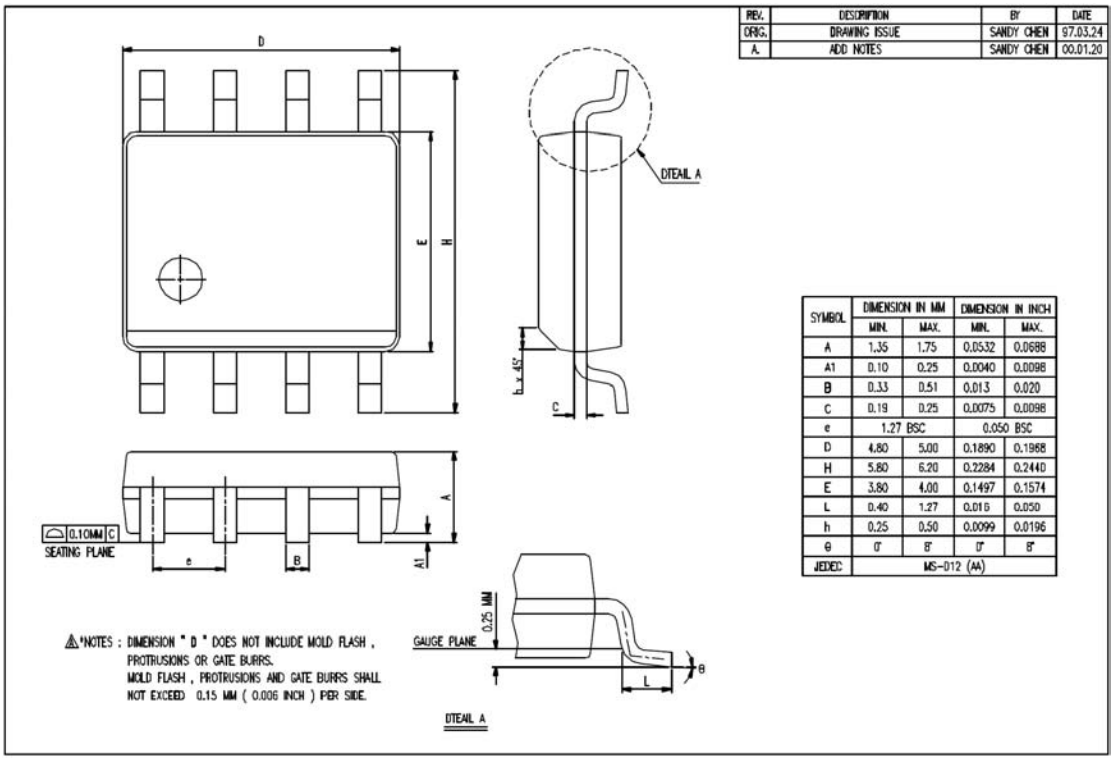
No.	Mask Option	Function Descriptions	
+1	**PWM0S**	0	Start 0
		1	Start 1
+1	**PWM1S**	0	Start 0
		1	Start 1
+1	**PWM2S**	0	Start 0
		1	Start 1
+2	**INT0F trigger type**	00	Low level trigger
	INT0S1,INT0S0	01	Falling edge trigger
		10	Rising edge trigger
		11	Dual edge trigger
+2	**INT1F trigger type**	00	Low level trigger
	INT1S1,INT1S0	01	Falling edge trigger
		10	Rising edge trigger
		11	Dual edge trigger
+1	**TPNIS**	0	TPNI use Schmitt trigger output signal
		1	TPNI use comparator output signal

§ Application Circuit



§ Package Information:

- **SOP 8**



§ Ordering Information：

	Package type
TTP275-AO8N	**SOP8**
TTP275-PO8N	**SOP8**

§ REVISION HISTORY：

2018/03/09：(Ver. 1.0) New build

2018/10/01：(Ver. 1.1) Modify Page5 Top=-40~+85