§ PATENTEN

1. PATENT：『電流源控制及補償觸控電容感測方法及其裝置』
   PAT NO. I339356 (Taiwan)
   PAT NO. ZL 2007 1 0202087. 0 (CHINA)
2. PATENT：『具環境變化校正的電容式觸控感測裝置』
   PAT NO. M383780 (Taiwan)
   PAT NO. ZL 2010 2 0141537. 7 (CHINA)
3. PATENT：『省電型多鍵觸摸開關感測裝置』
   PAT NO. M375250 (Taiwan)
   PAT NO. ZL 2010 2 0302392. 4 (CHINA)

§ General Description:

TTP275 MCU is an easy-used 4-bit CPU base microcontroller. It contains 1984-word ROM、144-nibble RAM、timer/Counter、interrupt service 、IO control hardware、LVR and touch pad feature for specified applications. The device is also suitable for diverse simple applications in control appliance and consumer product.

§ Features:

1. Tontek RISC 4-bit CPU core
2. Total 26 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
4. advance CMOS process
5. Working memory with 1984*16 program ROM and 144*4 SRAM
6. 2-level stacks
7. Operating voltage: 5.5V~2.7V
8. System operating frequency: (at VDD=5V)
   . High-speed system oscillator (OSCH):
   - ✧ Built-in RC oscillator: 4MHz(typical) ± 5%

   .Low speed peripheral oscillator (OSCL):
   - ✧ Built-in RC oscillator: 16KHz(typical) ± 30%

9. Offer 3 IO+3 touch pad or 6 general programmable I/O
   - ✧ IO port built-in key wake-up feature enable by software setting
   - ✧ Providing external interrupt inputs

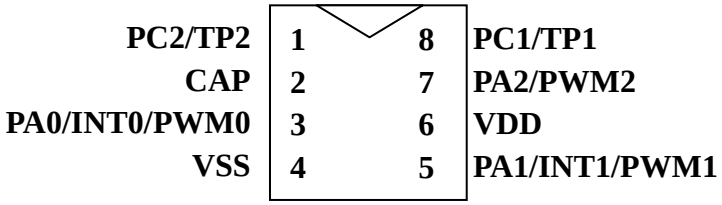
- ✧ Offering internal signal outputs, like buzzer(PWM)

10. One 8-bit TCP1 auto-reload timer/counter & onetime base counter
    - ✧ 4 timer clock sources selected by software
11. One 8-bit TCP2 auto-reload timer/counter, can improve PWM function
    - ✧ 4 timer clock sources selected by software
12. Two time base
    - ✧ Time base offers 2 various period interrupt request
13. Built-in 3 set 8-bit PWM output
14. MCU system protection and power saving controlled mode:
    - ✧ Built-in watch dog timer (WDT) circuit
    - ✧ ROM code error detection
    - ✧ Out of user program's range detection
    - ✧ Providing high/low system operating speed、sleep mode for power saving control
    - ✧ Built-in low voltage reset (LVR) function
15. 3 pins with touch pad detection
16. Provides 8 interrupt sources
    - ✧ External: INT0, INT1 shared with IO pad
    - ✧ Internal: two Timer/counter, two Time base timer
    - ✧ Two touchpad's interrupt
17. Provide package types
    - ✧ SOP 8

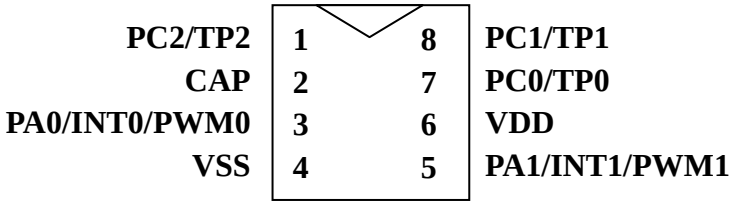
§ Applications:

1. Household electric appliances
2. Consumer products
3. Measurement controller

§ Package Description:



TTP275-AO8N
SOP8-A



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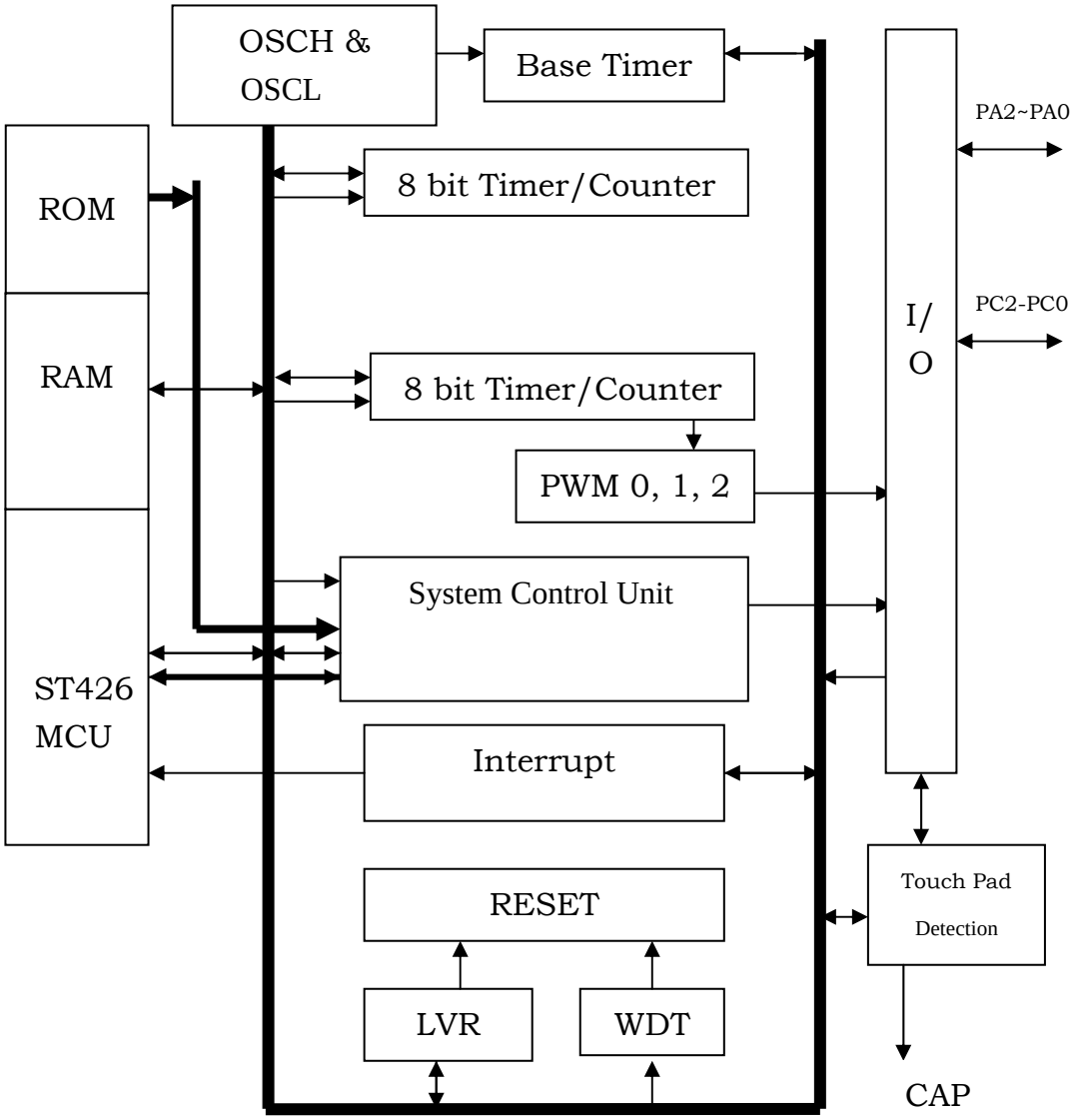
§ Block Diagram:



§ Pin Description:

Pin Name	Share Pin	I/O	Pin no.	Mask Option	Pin Description
V_{DD}	-	Power	+1	-	Positive power supply
V_{SS}	-	Power	+1	-	Negative power supply, ground
PA0 PA1 PA2	INT0/PWM0/VPP INT1/PWM1 PWM2	IO IO IO	+3	-	I/O port with external interrupt input and PWM output (PA0,PA1). PA2 is shared with internal PWM2 output.
PC0 PC1 PC2	TP0 TP1 TP2	IO/I IO/I IO/I	+3	-	IO port or touch pad input.
CAP	-	O	+1	-	Touch signal output
			9	-	

§ IO Cell type Description:

Pin Name	I/O Type	Description
PA0~PA1	Figure IO-C	STD IO with internal output & external input
PA2	Figure IO-B	STD IO with internal output
PC0~PC2	Figure IO-A	STD IO with external input

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-40 ~ +85	℃
Storage Temperature	Tst	-40 ~ +125	℃
OTP Supply Voltage	VPP	VSS-0.3 ~ VSS+12.5	V
Input Voltage	Vin	VSS -0.3 ~ VDD+0.3	V
Human Body Mode	ESD	>5	KV
Note: VSS symbolizes for system ground			

DC & AC Characteristics

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		2.7	-	5.5	V
Operating Current (Normal Mode, CPU working, I/O no load)	I_{nd1}	VDD=5.0V, no load, F_{OSCH}=4MHz,	-	2.5	3.0	mA
	I_{nd2}	VDD=5.0V, no load, F_{OSCL} on, F_{OSCH} off,	-	30	50	uA
Operating Current (Sleep Mode, CPU stop, I/O no load)	I_{sd1}	VDD=5.0V, no load, F_{OSCH}=4MHz,	-	0.7	1.0	mA
	I_{sd2}	VDD=3.0V, no load, F_{OSCL} on, F_{OSCH} off,	-	5	10	uA
LVR Current	I_{LVR}	VDD=5.0V	-	2	2.5	uA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
PA0 Sink Current	I_{OL}	VDD=5.0V, VOL=0.6V	-	2	-	mA
PA0 Source Current	I_{OH}	VDD=5V, VOH=VDD-0.7V	-	-1	-	mA
Output port Sink Current (exclude PA0)	I_{OL}	VDD=5.0V, VOL=0.6V	-	8	-	mA
Output Port Source Current (exclude PA0)	I_{OH}	VDD=5V, VOH=VDD-0.7V	-	-4	-	mA
I/O Port Pull-up Resistor	R_{PH}	VDD=5.0V	100	150	200	KΩ

§ AC Characteristics: (Test condition at room temperature=25°C)

Parameter	Test Condition		Min.	Typ.	Max.	Unit
External Reset	Low active pulse width tRES		2	-	-	CPU clock
Interrupt input	Low active pulse width tINT		2	-	-	
Wake up input	Low active pulse width t_{wkup}, Application de-bounce should be manipulated by user' software		2	-	-	OSCL
System Oscillator Frequency	F_{OSCH} (Built-in RC)	VDD=5.0V	-	4M	-	Hz
Peripheral Oscillator Frequency	Built-in F_{OSCL}(RC)	VDD=5.0V	12K	16K	21K	Hz
Startup Period of Oscillators	T_{OSCH} (Built-in RC)	wake-up from off mode	8	-	-	F_{OSCH}
	T_{OSCL} (Built-in RC)	Wake-up from off mode	8	-	-	F_{OSCL}
Stable Time Of System Clock Switching	T_{OSCH} (Built-in RC)	OSCL→OSCH & OSCH off	8	-	-	F_{OSCH}
	(If H/L=0 then OSCH stop)					
	T_{OSCL} (Built-in RC)	OSCH→OSCL & OSCL on	8	-	-	F_{OSCL}
Timer/Counter input clock frequency	Input frequency rating, no de-bounce circuit built-in ,at VDD=5V		DC	-	4M	Hz
System Stable Time after Power up	After power up, the system needs to initialize the configured state and OST.		-	-	40	ms

§ Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~$7BF_H$	-	Program ROM [1984*16]
-	000_H ~007_H	File Registers
-	008_H~$01F_H$	Peripheral registers (I)
-	020_H~$0AF_H$	Working RAM [144*4]
-	200_H~303_H	Peripheral registers (II)

§ Interrupt Vectors:

Interrupt Vectors	Function Description
$000	hardware RESET
$001	Hardware IRQ

§ File registers:

Address	Symbol	R/W	Default	Description
000_H	(DP1)	R/W	-	Indirect addressing register
001_H	ACC	R/W	-	Accumulator & Read Table 1st data
002_H	TB1	R/W	-	Read Table 2nd data
003_H	TB2	R/W	-	Read Table 3rd data
004_H	TB3	R/W	-	Read Table 4th data
005_H	DPL	R/W	-	Data Pointer low nibble
006_H	DPM	R/W	-	Data Pointer middle nibble
007_H	DPH	R/W	-	Data Pointer high nibble

§ Peripheral registers: Interrupt request flag register

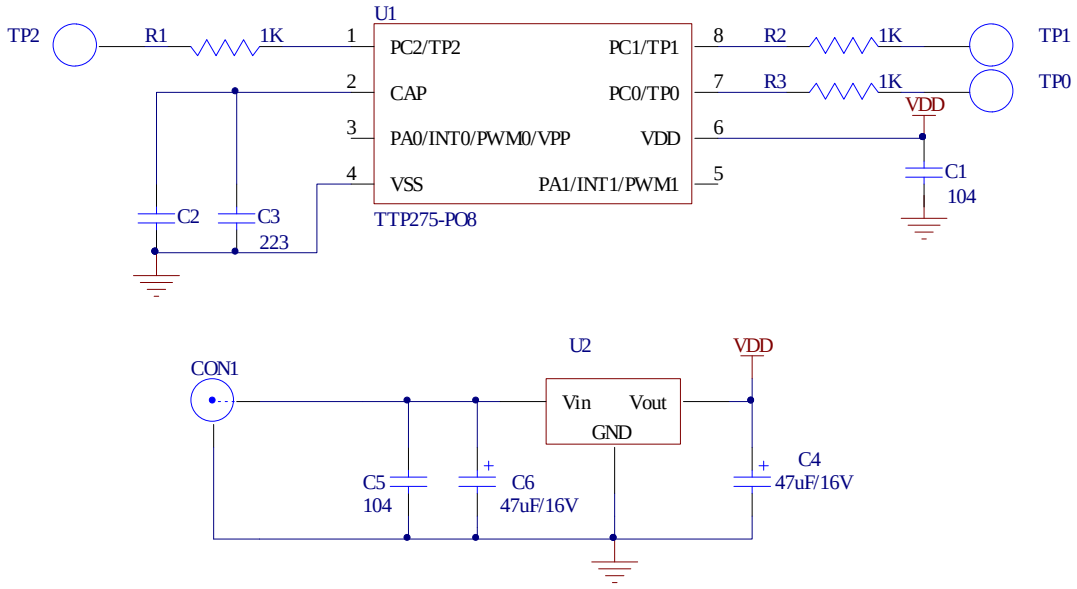
Address	Symbol	R/W	Default	Description
008_H	PS	R/W	-10-	CPU power saving control register
009_H	-	-	-	
$00A_H$	INTC	R/W	0000	Interrupt enable control register
$00B_H$	INTF	R/W	0000	Interrupt request flag register
$00C_H$	INTC1	R/W	--00	Extended interrupt enable register
$00D_H$	INTF1	R/W	--00	Extended interrupt request flag register
$00E_H$	PWMC	R/W	-000	PWM control register
$00F_H$	PWM0L	R/W	xxxx	PWM0 duty low nibble data register
010_H	PWM0H	R/W	xxxx	PWM0 duty high nibble data register
011_H	-	-	-	
012_H	PAC	R/W	-111	I/O port A control register

013_H	PA	R/W	-111	I/O port A data register
014_H	-	-	-	
015_H	-	-	-	
016_H	PCC	R/W	-111	I/O port C control register
017_H	PC	R/W	-111	I/O port C data register
018_H	-	-	-	
019_H	-	-	-	
$01A_H$	PWM1L	R/W	xxxx	PWM1 duty low nibble data register
$01B_H$	PWM1H	R/W	xxxx	PWM1 duty high nibble data register
$01C_H$	PWM2L	R/W	xxxx	PWM2 duty low nibble data register
$01D_H$	PWM2H	R/W	xxxx	PWM2 duty high nibble data register
$01E_H$	TPINTC	R/W	00--	Touchpad interrupt enable control register
$01F_H$	TPINTF	R/W	00--	Touchpad interrupt request flag register
200_H	TCP1C	R/W	0000	TCP1 Timer/counter control register
201_H	TCP1L	R/W	xxxx	TCP1 Timer/counter data low register
202_H	TCP1H	R/W	xxxx	TCP1 Timer/counter data high register
203_H	TCP2C	R/W	0000	TCP2 Timer/counter control register
204_H	TCP2L	R/W	xxxx	TCP2 Timer/counter data low register
205_H	TCP2H	R/W	xxxx	TCP2 Timer/counter data high register
206_H	PAI	R	----	Port A pad data reading address
207_H	-	-	-	
208_H	PCI	R	----	Port C pad data reading address
209_H	-	-	-	
$20A_H$	-	-	-	-
$20B_H$	-	-	-	-
$20C_H$	TCPFS	R/W	-000	TCP clock source FS pre-scale register
$20D_H$	TBC	R/W	1111	Time base control register
$20E_H$	MCKS	R/W	-111	Modulation clock selector register
$20F_H$	TPCHS0	R/W	-000	Touch pad channel selector register
210_H	-	-	-	
211_H	-	-	-	
212_H	TPCTL	R/W	-000	Touch pad control register
213_H	TPCT0	R/W	xxxx	Touch pad Duty counter 1st nibble
214_H	TPCT1	R/W	xxxx	Touch pad Duty counter 2nd nibble
215_H	TPCT2	R/W	xxxx	Touch pad Duty counter 3rd nibble
216_H	-	-	-	
217_H	-	-	-	
218_H	-	-	-	
219_H	SPCON1	R/W	-000	Special control register 1
$21A_H$	-	-	-	
$21B_H$	ADJSTAT	R	--1-	Frequency Adjustment Status flag register
$21C_H$	OSCHADJ	R/W	-001	OSCH frequency adjustment register
300_H	RESETF	R/W	0000	Reset flag
301_H	TBRB	W	xxxx	Time base counter clear address
302_H	MRO	W	xxxx	Mask option register write enable address
303_H	CLRWDT	W	xxxx	Clear WDT 2nd instruction

Note:
a. Default means initial value after power on or reset.
b. R is "read" only, W is "write" only, R/W is both of "read" & "write".

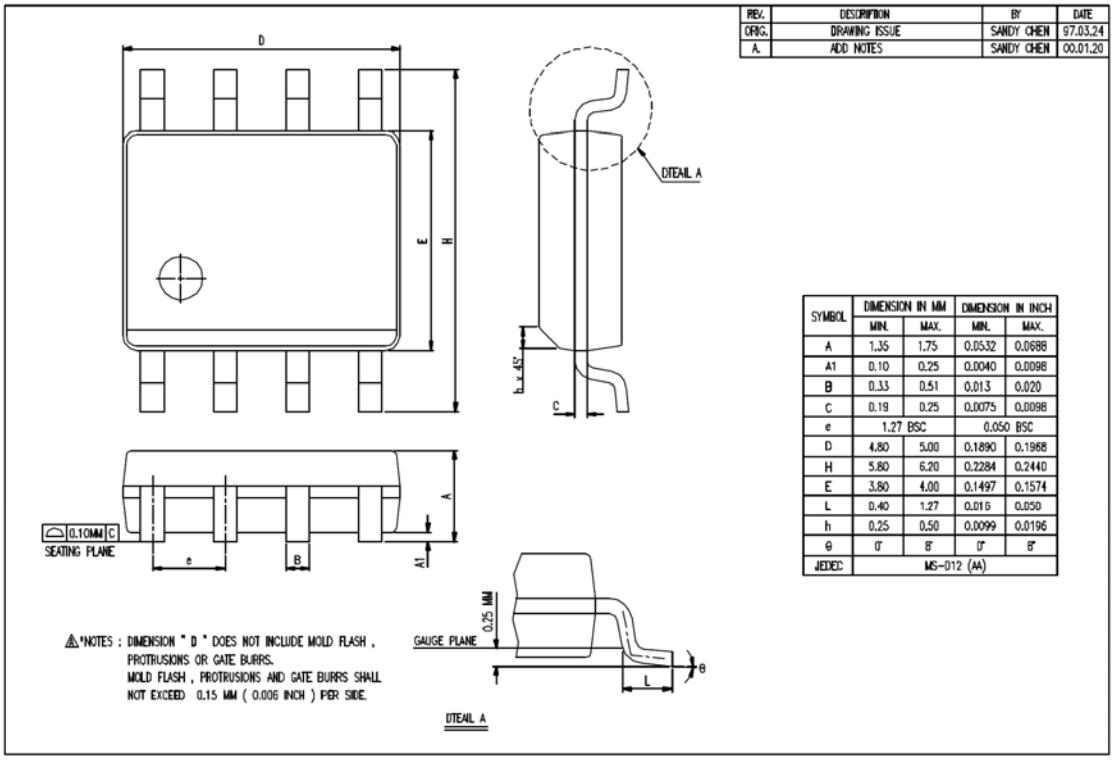
Reference only

§ Application Circuit



§ Package Information:

- **SOP 8**



§ Ordering Information：

	Package type
TTP275-AO8N	**SOP8**
TTP275-PO8N	**SOP8**

§ REVISION HISTORY：

2018/03/09：(Ver. 1.0) New build

2018/10/01：(Ver. 1.1) Modify Page5 Top=-40~+85