# 1 key Touch Pad Detector IC

## Outline

- The TTP233D-KB8 TonTouch$^{TM}$ is a touch pad detector IC which offers 1 touch key. The device built-in regulator for touch sensor. Stable sensing method can cover diversity conditions. The touching detection IC is designed for replacing traditional direct button key with diverse pad size. Low power consumption and wide operating voltage are the contact key features for DC or AC application.

## Characteristic

- Operating voltage 2.4V ~ 5.5V

- Built-in regulator for touch sensor

- Built-in low voltage reset (LVR) function

- Operating current, @VDD=3V no load
  At low power mode typical 1.5uA, maximum 3uA
  At fast mode typical 4uA, maximum 8uA

- The response time about 46mS at fast mode, 160mS at low power mode @VDD=3V

- Sensitivity can adjust by the capacitance（1~50pF）outside

- Stable touching detection of human body for replacing traditional direct switch key

- Provides Fast mode and Low Power mode selection by pad option (LPMB pin)

- Provides direct output or toggle output selection by pin option (TOG pin)

- Have the maximum on time about 16 sec($\pm 35\%$ @ VDD=3.0V)

- Q pin is CMOS output can be selected active high or active low by pad option (AHLB pin)
  OPDO that has no diode protection, active low

- After power-on have about 0.5sec stable-time, during the time do not touch the key pad, and the function is disabled

- Auto calibration for life
  The re-calibration period is about 1 sec within 8 sec after power-on. When key has been touched within 8 sec or key has not been touched more than 8 sec after power-on, then the re-calibration period change to 4 sec

## Applications

- Wide consumer products
- Button key replacement

## Block diagram
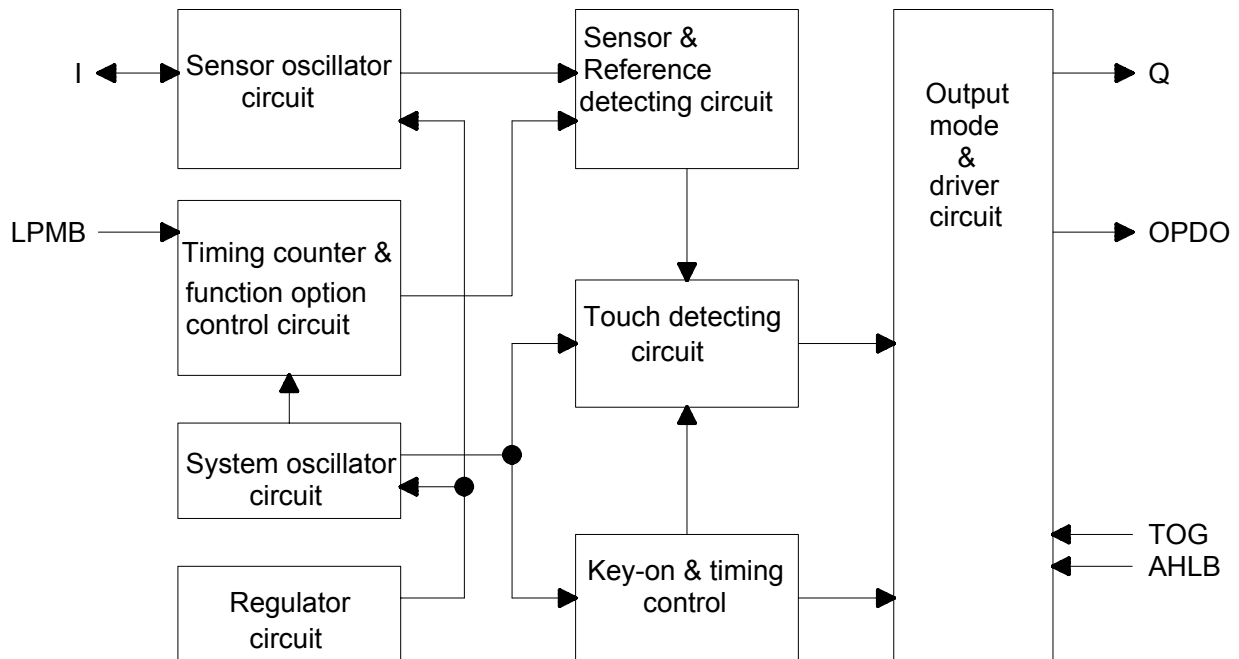


## Pin Description

| Pin NO | Pin Name | Type | Pad Description |
|--------|----------|------|-----------------|
| 1 | I | I/O | Input sensor port |
| 2 | VSS | P | Negative power supply, ground |
| 3 | OPDO | OD | Open drain output pin active low(have no Diode protective circuit) |
| 4 | Q | O | CMOS output pin |
| 5 | LPMB | I-PH | Low power mode selection, 1(Default)=>Fast mode; 0=>Low power mode |
| 6 | TOG | I-PL | Output type option pin, 0(Default)=>Direct output; 1=>Toggle output |
| 7 | AHLB | I-PL | Output Q active high or low selection, 0(Default)=>Active high; 1=>Active low |
| 8 | VDD | P | Positive power supply |

## Pin Type

- I     CMOS input only
- O     CMOS push-pull output
- I／O   CMOS I／O
- P     Power／Ground

- I-PH   CMOS input and pull-high resister
- I-PL   CMOS input and pull-low resister
- OD     Open drain output, have no Diode protective circuit

## Electrical Characteristics

- ### Absolute maximum ratings

| Parameter | Symbol | Conditions | Rating | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_{OP}$ | — | -40～+85 | ℃ |
| Storage Temperature | $T_{STG}$ | — | -50～+125 | ℃ |
| Supply Voltage | VDD | Ta=25°C | VSS-0.3～VSS+5.5 | V |
| Input Voltage | $V_{IN}$ | Ta=25°C | VSS-0.3～VDD+0.3 | V |
| Human Body Mode | ESD | — | 5 | KV |
| Note：VSS symbolizes for system ground | | | | |

- ### DC / AC characteristics：（Test condition at room temperature = 25 ℃）

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 2.4 | 3 | 5.5 | V |
| Internal Regulator Output | VREG | | 2.2 | 2.3 | 2.4 | V |
| Operating Current | $I_{OPL}$ | VDD=3V, At low power mode | | 1.5 | 3 | uA |
| | $I_{OPF}$ | VDD=3V, At fast mode | | 4.0 | 8 | uA |
| Input Ports | $V_{IL}$ | Input Low Voltage | 0 | | 0.2 | VDD |
| Input Ports | $V_{IH}$ | Input High Voltage | 0.8 | | 1.0 | VDD |
| Output Port Sink Current | $I_{OL}$ | VDD=3V, $V_{OL}$=0.6V | | 8 | | mA |
| Output Port Source Current | $I_{OH}$ | VDD=3V, $V_{OH}$=2.4V | | -4 | | mA |
| Input Pin Pull-high Resistor | $R_{PH}$ | VDD=3V (LPMB) | | 30K | | ohm |
| Input Pin Pull-low Resistor | $R_{PL}$ | VDD=3V (TOG, AHLB) | | 25K | | ohm |
| Output Response Time | $T_R$ | VDD=3V、At fast mode | | 46 | | mS |
| | | VDD=3V、At low power mode | | 160 | | |

## Function Description

### Ⅰ. Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP233D-KB8 offers some methods for adjusting the sensitivity outside.

1.  by the electrode size
    Under other conditions are fixed. Using a larger electrode size can increase sensitivity. Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope.

2.  by the panel thickness
    Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value.

3.  by the value of Cs please see the down figure
    Under other conditions are fixed. When do not use the Cs to VSS, the sensitivity is most sensitive. When adding the value of Cs will reduce sensitivity in the useful range （$1 \leq Cs \leq 50pF$）.
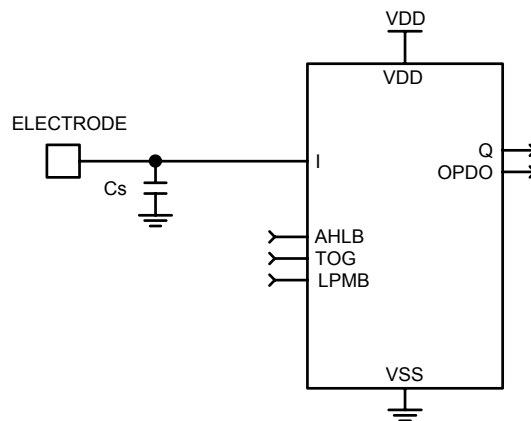


### Ⅱ. Output mode By TOG AHLB pin option

TOG pin： Direct output or toggle output selection.

AHLB pad： Output Q active high or active low selection.

### Pin Q（CMOS output）option features：

| TOG | AHLB | Pin Q option features |
|-----|------|-----------------------|
| 0 | 0 | Direct output, CMOS active high |
| 0 | 1 | Direct output, CMOS active low |
| 1 | 0 | Toggle output, power on state = 0 |
| 1 | 1 | Toggle output, power on state = 1 |

**Pad OPDO（Open drain active low output, has no diode protective circuit）**
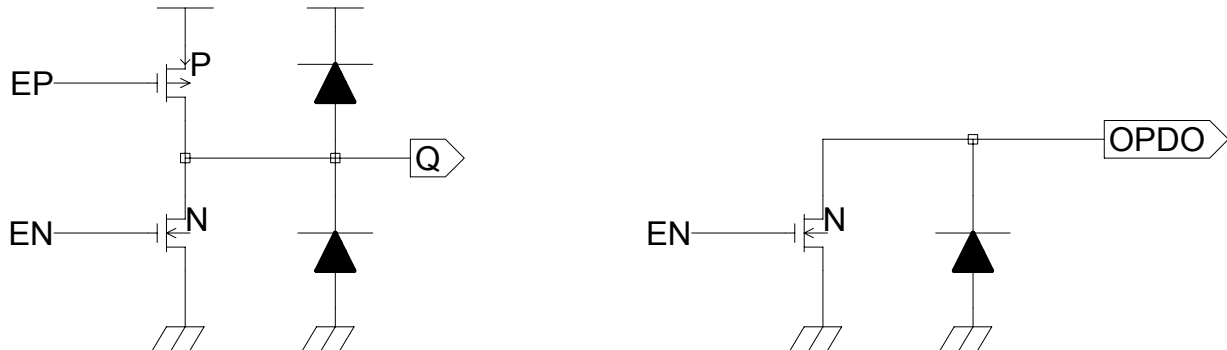


## Ⅲ. Maximum key on duration time

If some objects cover in the sense pad, and causing the change quantity enough to be detected. To prevent this, the TTP233D-KB8 sets a timer to monitor the detection. The timer is the maximum on duration time. It is set about 16 sec(±35%) at 3V. When the detection is over the timer, the system will return to the power-on initial state, and the output becomes inactive until the next detection.

## Ⅳ. Fast and Low power mode selection　By LPMB pad option

The TTP233D-KB8 has Fast mode and Low Power mode to be selected. It depends on the state of LPMB pad. When the LPMB pin is opened or connected to VDD, the TTP233D-KB8 runs in Fast mode. When the LPMB pin is connected to VSS, the TTP233D-KB8 runs in Low Power mode.

In the Fast mode response time is faster, but the current consumption will be increased. In the Low Power mode it will be saving power, but will be slowing response time for first touch. When it awaked in fast mode, the response time is the same the fast mode. In this mode when detecting key touch, it will switch to Fast mode. Until the key touch is released and will keep a time about 10 sec. Then it returns to Low Power mode.

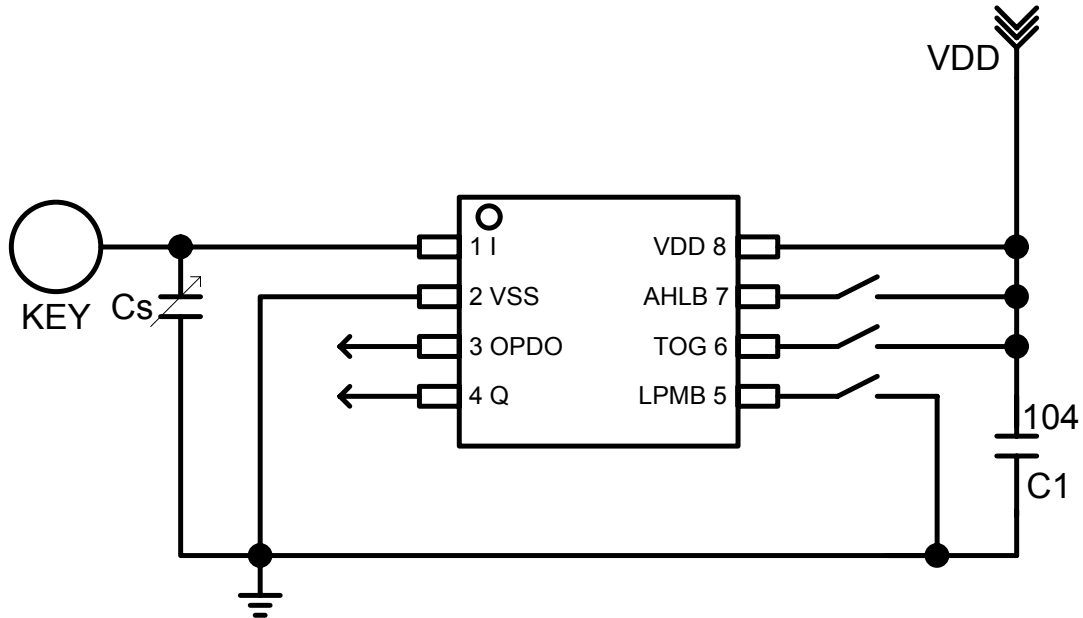**The states and timing of two modes please see below figure.**



Fast Mode
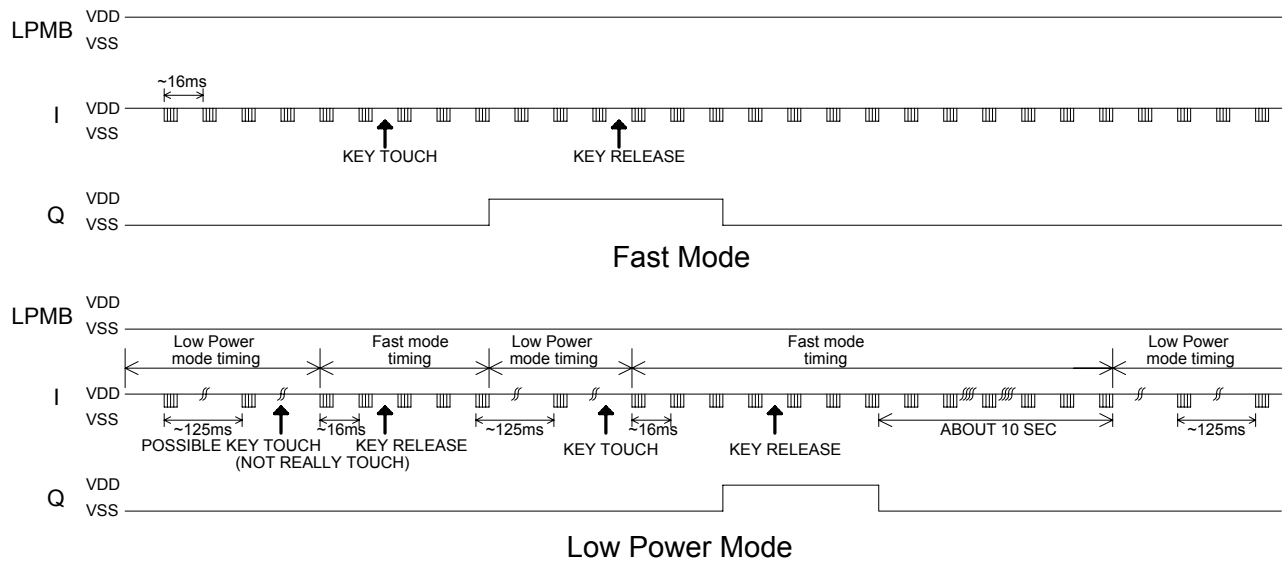


Low Power Mode

| LPMB | Option features |
|------|-----------------|
| 1 | Fast mode |
| 0 | Low Power mode |

## Ⅴ. Option pin

For power saving concern and package bonding option consideration, all the feature option pins with latch type design and initial states are 0 or 1 as power on. If those pins are forced to VDD or VSS, the states will be changed to 1 or 0 without any current leakage to conflict the power saving issue.

| Feature option pins | Initial state by Power on |
|---------------------|---------------------------|
| AHLB | 0 |
| TOG | 0 |
| LPMB | 1 |

**Application circuit**                                   **Reference only**



P.S. :

1. On PCB, the length of lines from touch pad to IC pin shorter is better.
   And the lines do not parallel and cross with other lines.

2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.

3. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.

4. The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP233D-KB8).

5. The capacitance Cs can be used to adjust the sensitivity. The value of Cs use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range of Cs value are 1~50pF.

6. The sensitivity adjustment capacitors（Cs）must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.

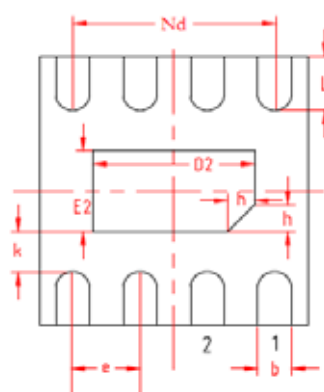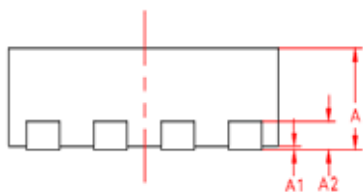## Package outline

Package Type: DFN8L
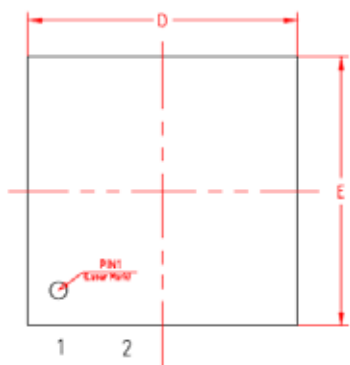
TOP VIEW     SIDE VIEW     BOTTOM VIEW

| DIMENSION IN MM | | | |
|--------|------|---------|------|
| SYMBOL | MIN | NOMINAL | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | – | 0.02 | 0.05 |
| A2 | | 0.203 REF | |
| b | 0.20 | 0.25 | 0.30 |
| D | 1.90 | 2.00 | 2.10 |
| D2 | 1.10 | 1.20 | 1.30 |
| E | 1.90 | 2.00 | 2.10 |
| E2 | 0.60 | 0.70 | 0.80 |
| e | | 0.50 BSC | |
| K | 0.25 | 0.30 | 0.35 |
| L | 0.30 | 0.35 | 0.40 |
| h | 0.15 | 0.20 | 0.25 |
| Nd | | 1.50 BSC | |

SIDE VIEW

## Package configuration

TTP233D-KB8

Package Type DFN8L
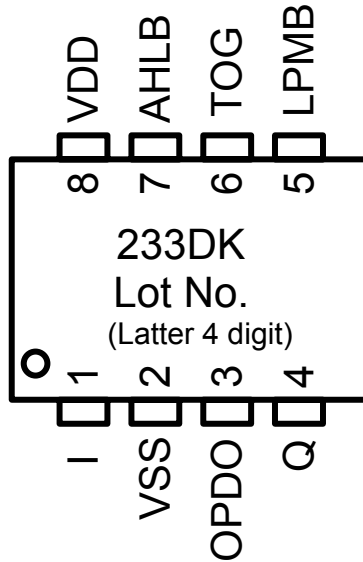


## Ordering Information

| TTP233D-KB8 | | |
|---|---|---|
| **Package Type** | **Chip Type** | **Wafer Type** |
| TTP233D-KB8 | No support | No support |

## REVISION HISTORY

1. 2019/08/15
 - Initial version：V1.0