Version: 1.0



# PIR sensor control chip

### **Content**

Outline	2
Characteristic	2
Applications	2
Pin Description	4
Electrical Characteristics	5
Function Description	6
I . Function description	6
${\rm I\hspace{1em}I}$ . Description of repetitive and non-repeatable trigger functions	6
Ⅲ. Application Description	9
Application Circuit	10
I . Application Circuit(1): PIR infrared sensor schematic diagram	10
∏ . Application Circuit(2) : VCC = 5.5V ~28V DC DEMO	11
Ⅲ. Application Circuit(3): Reset by external RC	11
Package outline	12
Package Type: SOP-16	12
Package configuration	13
Ordering Information	13
Revision History:	13



#### Outline

TTP136G is a CMOS chip designed to human infrared sensor control integrated circuits; it is a kind of high-performance sensor signal processing integrated circuit (IC) which together with PIR sensor and outward elements to constituent PIR switch. It can automatically and quickly open such devices as incandescent lamps, fluorescent lamps, buzzers, automatic valves, electric fans, dryers and automatic hand-washing facilities. IC is especially suitable for enterprises, hotels, shopping malls, warehouses, passages or corridors of houses, automatic lights, lighting systems and alarm systems.

#### Characteristic

- Operating voltage 1.8~6.0V.
- Lower Power mode operating Current (no load)
  - @VDD=3.0V, typical 20uA
  - @VDD=5.0V, typical 33uA
- Also compatible with BISS0001.
- Built-in two-way discriminator can effectively suppress interference.
- Built-in reference power supply for internal comparator and operational amplifier.
- Built-in delay time timer (Tx) and blocking time timer (Ti), novel structure, stable and reliable, and wide adjustment range.
- 16-pin SOP package.

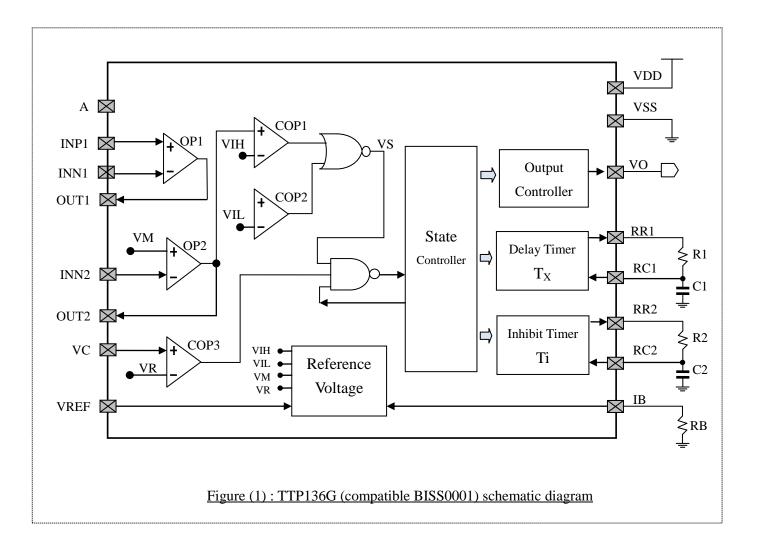
## **Applications**

- Human infrared sensor lights.
- Automatic energy-efficient lighting occasions like garden, garage, hallway, stairs.
- Monitoring, alarm, doorbell system like home, shops, offices, factories.
- Automatic switching system like exhaust fans, ceiling fans

2021/11/11 Page 2 of 13 Version: 1.0



## Block diagram





## Pin Description

Pin	Pin	I/O	Din Description
NO.	Name	Type	Pin Description
1	A	I	Retriggerable & non-retriggerable mode select
			(A=0: on- retriggerable, A=1: retriggerable)
2	VO	O	Detector output pin (active high)
3	RR1	O	Tx adjustment terminal output
4	RC1	I	Tx adjustment terminal input
			$TX \approx 49152R1C1$
5	RC2	I	Ti adjustment terminal input
3	RC2	1	$Ti \approx 48R2C2 \circ$
6	RR2	O	Ti adjustment terminal output
7	VSS	P	Negative power supply, ground
8	VREF	I	Reset & voltage reference input
0	V/C	т	Trigger input control
9	VC	I	VC<0.2*VDD =disable; VC>0.2*VDD=enable
10	ID.	1/0	Op-amp input bias current setting (RB connect to VSS,
10	IB	I/O	RB about = $1.5M\Omega$ )
11	VDD	P	Positive power supply, VDD
12	OUT2	О	2 <sup>nd</sup> stage Op-amp output
13	INN2	I	2 <sup>nd</sup> stage Op-amp inverting input
14	INP1	I	1 <sup>st</sup> stage Op-amp non-inverting input
15	INN1	I	1 <sup>st</sup> stage Op-amp inverting input
16	OUT1	O	1 <sup>st</sup> stage Op-amp output

## Pin Type

• I CMOS input only

• O CMOS output

• I/O CMOS input/output

• P Power/Grand



## **Electrical Characteristics**

### • Absolute maximum ratings

Parameter	Symbol	Conditions	Rating	unit				
Operating Temperature	TOP	_	-40 <b>∼</b> +85	$^{\circ}\! \mathbb{C}$				
Storage Temperature	TSTG	_	-50∼+125	$^{\circ}\! \mathbb{C}$				
Supply Voltage	VDD	Ta=25°C	VSS-0.3~VSS+5.5	V				
Input Voltage	VIN	Ta=25°C	VSS-0.3~VDD+0.3	V				
Human Body MODE	ESD	_	≥4	KV				
Note: VSS symbolizes for system ground								

### • DC / AC characteristics : (Test condition at room temperature = $25 \, ^{\circ}\text{C}$ )

Parameter	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Operating Voltage	VDD		1.8	5.0	6.0	V
		RB=1.5MΩ,VDD=3V, no load	-	20	30	uA
Lower Power mode	т	RB=2.0MΩ,VDD=3V, no load	1	15	25	uA
Operating current	$I_{OP}$	RB=1.5MΩ,VDD=5V, no load	1	33	45	uA
		RB=2.0MΩ,VDD=5V, no load	-	24	40	uA
OP Offset voltage	Vos	VDD=5.0V	-	-	50	mV
OP input leakage	I <sub>LEAK</sub>	VDD=5.0V	-	-	50	nA
Open loop-Gain	A <sub>VN</sub>	VDD=5V, RL=1.5MΩ	60	-	-	dB
Common-mode	CMRR	VDD=5V, RL=1.5MΩ	60	-	-	dB
rejection ratio						
OP Output High	VYH	VDD=5V	4.25	-	-	V
OP Output Low	VYL	RL=500KΩ 接 1/2VDD	-	-	0.75	V
VC Input High	VCH	VREF=VDD=5V	1.1	-	-	V
VC Input Low	VCL		-	-	0.9	V
VO Output High	VOH	VDD=5V IOH=0.5mA	4	4.8	-	V
VO Output Low	VOL	VDD=5V IOL=0.1mA		0.1	0.4	V
A Input High	VAH	VDD=5V	3.5	-	-	V
A Input Low	VAL	VDD=5V	-	-	1.5	V



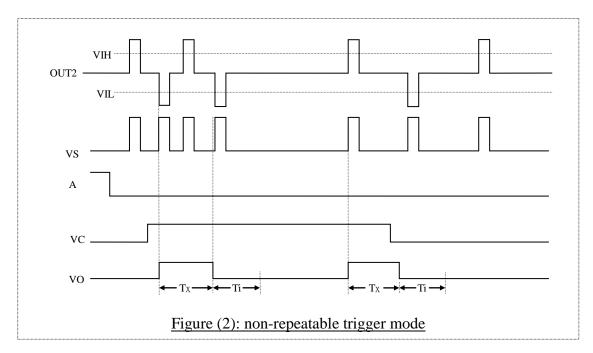
## **Function Description**

#### I . Function description

<u>Figure (1)</u> is the principle block diagram of TTP136G (compatible with BISS0001) infrared sensor signal processor. The external components are selected by the user according to their needs. It can be seen from the figure that TTP136G is a dedicated digital-analog hybrid integrated circuit composed of operational amplifiers, voltage comparators and state controllers, delay time timers, block time timers, and reference voltage sources. It can be widely used in a variety of sensors and delay controller.

#### II. Description of repetitive and non-repeatable trigger functions

Let us first illustrate the working process of TTP136G (compatible with BISS0001)
with the waveforms of each point in the non-repeatable trigger mode shown in
Figure (2)



- 1-1. First, the user uses the operational amplifier OP1 to form a sensor signal pre-processing circuit to amplify the signal according to actual needs.
- 1-2. Then it is integrated to the operational amplifier OP2, and the second stage of amplification is carried out. At the same time, the DC potential is raised to VM ( $\approx 0.5 \text{VDD}$ ), and then sent to the bidirectional amplitude discriminator composed of comparators COP1 and COP2 to detect the effective trigger signal VS.
- 1-3. Because VIH  $\approx$  0.7VDD, VIL  $\approx$  0.3VDD, when VDD = 5V, the noise interference of  $\pm 1V$  can be effectively suppressed, and the reliability of the system is improved.
- 1-4. When the input voltage VC  $\leq$  VR ( $\approx$  0.2VDD), the output of COP1 is low level to seal the gate U2, and the trigger signal VS is forbidden to pass to the lower level.

2021/11/11 Page 6 of 13 Version: 1.0



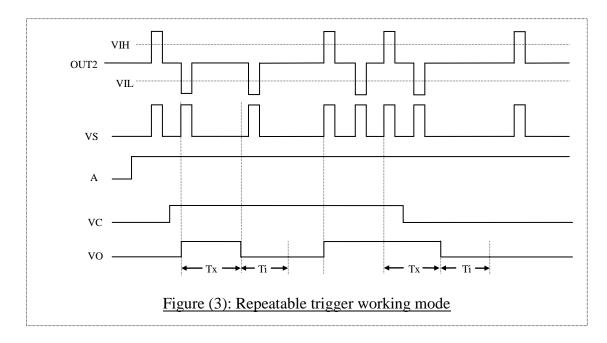
- 1-5. When VC> VR, the output of COP1 is high, and U2 is turned on and U2. At this time, if the rising edge of the trigger signal VS comes, the delay time timer can be started, and the VS terminal output is high. Enter the delay cycle.
- 1-6. When the A terminal is connected to the "0" level, any change in VS during the TX time will be ignored until the end of the TX time, which is the so-called non-repeatable trigger mode.
- 1-7. When the TX time is over, VS jumps back to low level, and at the same time starts the lockout timer and enters the lockout period Ti.
- 1-8. During the Ti cycle, any change in VS cannot make VO a valid state. The setting of this function can effectively suppress various interferences generated during load switching.

#### Note:

- (1) The higher the VDD and the larger the sensing distance window (VIH-VIL), the better the noise suppression characteristics.
- (2) On the contrary, the lower the VDD, the longer the sensing distance, that is, the smaller the window (VIH-VIL), but the worse the noise suppression characteristics.



2. Let us first illustrate the working process of TTP136G (compatible with BISS0001) in this state with the waveform of each point in the repeatable trigger mode shown in Figure (3).



- 2-1. During the period of VC = "0" and A = "0", VS cannot trigger VO to be in a valid state. When VC = "1" and A = "1", VS can repeatedly trigger VO to be in a valid state, and it will remain valid during the TX cycle.
- 2-2. During TX time, as long as there is an upward transition of VS, VO will continue to extend for one TX cycle from the moment of VS upward transition. 1 If VS remains "1", VO will always remain active.
- 2-3. If VS remains in the "0" state, VO will return to the invalid state after the TX cycle ends, and within the blocking time Ti, any change in VS cannot trigger VO to be in the valid state.

Through the above analysis, we have a comprehensive understanding of the circuit structure and working process of TTP136G (compatible with BISS0001). It can be seen that the device has a novel structural design and strong functions, and can be applied in a wide range of fields.

2021/11/11 Page 8 of 13 Version: 1.0



#### Ⅲ. Application Description

The PIR infrared switch is a passive infrared switch composed of TTP136G (compatible with BISS0001) and a PIR infrared sensor and a small number of external components. It can automatically and quickly turn on all kinds of incandescent lamps, fluorescent lamps, buzzers, automatic doors, electric fans, dryers, and automatic hand-washing sinks. It is a high-tech product. It is especially suitable for sensitive areas such as aisles and corridors of enterprises, hotels, shopping malls, warehouses and families, or for automatic lighting, lighting and alarm systems in safe areas.

PIR infrared sensor is a new type of sensitive element, which is composed of high PIR coefficient material, matched with filter lens and field effect tube for impedance matching. It can detect the infrared radiation emitted from the human body in a non-contact manner, convert it into electrical signal output, and effectively suppress interference radiation outside the human body radiation wavelength. Such as sunlight, lights and their reflectors.

In this example, the operational amplifier OP1 of TTP136G (compatible with BISS0001) is used as the preamplifier of the PIR infrared sensor, and C3 is coupled to the operational amplifier OP2 for the second stage of amplification. After processing by the two-way amplitude discriminator formed by the voltage comparators COP1 and COP2, a valid trigger signal is detected to start the delay time timer. The output signal passes through the transistor Q1 and drives the relay to connect the load. R3 is a photoresistor, which is used to detect the ambient illuminance. When used as lighting control, if the environment is brighter, the resistance value of R3 will be reduced, making the 9-pin input low and blocking the trigger signal, saving lighting power. If it is applied to other areas, it can be covered with shades without being affected by the environment. SW1 is a working mode selection switch. When SW1 is connected to terminal 1, the infrared switch is in a repeatable trigger mode; when SW1 is connected to terminal 2, the infrared switch is in a non-repeatable mode of triggering.

#### Note:

- (1). Accord to <u>Application Circuit(1)</u>. The operational amplifier OP1 is used as the pre-amplifier of the PIR infrared sensor. After power-on, to make the operational amplifier work normally, the potential of the C5 capacitor must be charged to the same potential at the S terminal of the infrared sensor, that is, INN1 potential ≈ INP1 potential.
  - The charging time is affected by C5 capacitance value/R7, R8 resistance value/S terminal potential.
- (2). Operational amplifier OP2 is used as the second-stage amplification, and the C3 capacitor must be charged to VM ( $\approx 0.5 \text{VDD}$ ) potential, the operational amplifier can work normally, and the charging time is affected by the value of C3 capacitor/R5, R10 resistance.
- (3). The above two charging actions will be carried out at the same time. Both capacitors must be charged until both operational amplifiers can work. The

2021/11/11 Page 9 of 13 Version: 1.0



time required is called the sensor warm-up time.

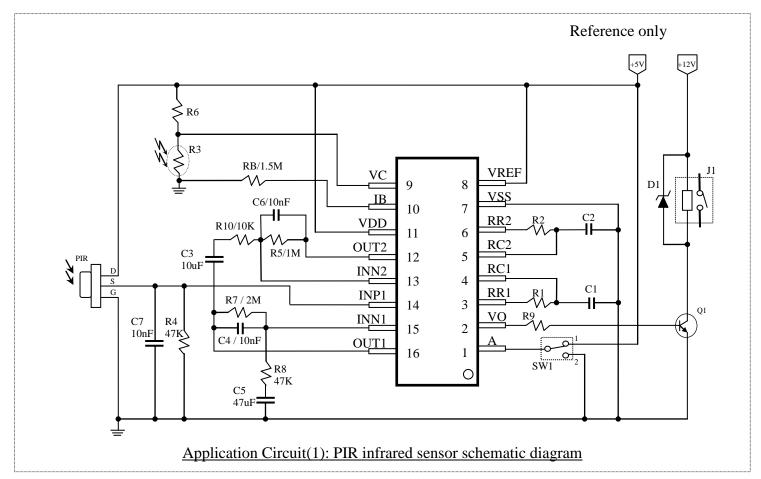
(4). Take the provided application circuit as an example. When the pyroelectric infrared sensor S terminal voltage=0.7V, R8=47K  $\Omega$ , R7=2M  $\Omega$ , R5=1M  $\Omega$ , R10=10K  $\Omega$ , C3=10uF, C5=47uF, C4=C6=10nF.

The warm-up time is about 35 seconds under the condition of VDD=5V, and about 48 seconds under the condition of VDD=3.3V, both of which are the warm-up time required at room temperature.

(5). The system cannot be triggered normally during the warm-up time.

### **Application Circuit**

I . Application Circuit(1): PIR infrared sensor schematic diagram

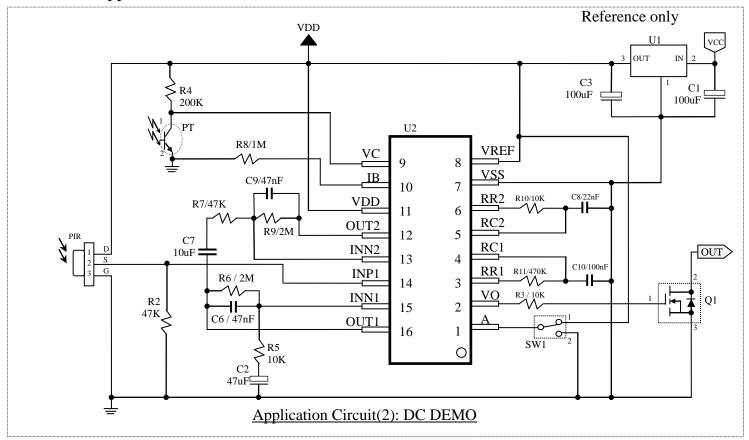


$RR_1RC_1 - TX \approx 491$	•	nent terminal		$\begin{array}{c} \textbf{RR}_2\textbf{RC}_2 - \text{Tr adjustment terminal} \\ \textbf{Ti} \approx 48R2C2 \end{array}$					
C1	R1	VDD=5V	VDD=3.3V	C2	R2	VDD=5V	VDD=3.3V		
CI	KI	Tx time	Tx time	CZ	K2	T <sub>I</sub> time	T <sub>I</sub> time		
0.01uF	$22K\Omega$	7.1 sec	5.7 sec	0.1uF	300KΩ	1.1 sec	1.0 sec		
0.01uF	47ΚΩ	15 sec	12 sec	0.1uF	430ΚΩ	1.6 sec	1.3 sec		
0.01uF	100ΚΩ	31 sec	25 sec	0.1uF	620KΩ	2.3 sec	2.0 sec		
0.01uF	200ΚΩ	62 sec	49 sec	0.1uF	$1M\Omega$	3.7 sec	3.1 sec		
0.01uF	330ΚΩ	102 sec	80 sec						
0.01uF	680ΚΩ	209 sec	164 sec						
0.01uF	1ΜΩ	308 sec	242 sec						

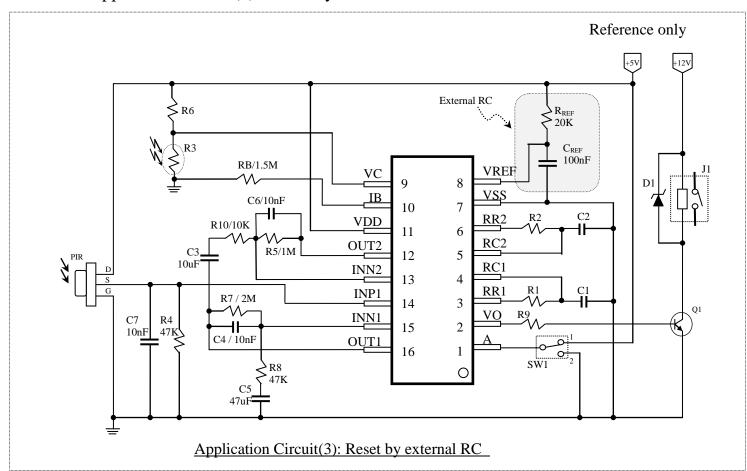
2021/11/11 Page 10 of 13 Version: 1.0



### II . Application Circuit(2) : VCC = 5.5V ~28V DC DEMO



### Ⅲ. Application Circuit(3): Reset by external RC



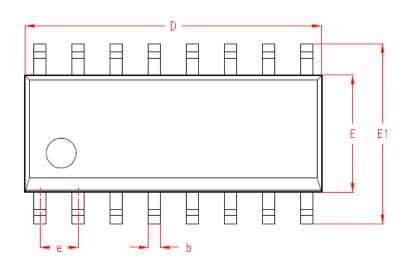


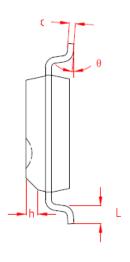
## Package outline

Package Type: SOP-16

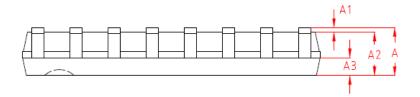
TOP VIEW







SIDE VIEW



	Symbol Parameter (Unit : mm)													
	A			Al		A2			A3			b		
Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
		1.75	0.10		0.25	1.35	1.45	1.55	0.60	0.65	0.70	0.35		0.50

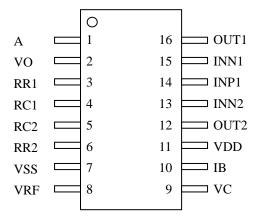
Symbol Parameter (Unit : mm)													
	c			D		E			E1			e	
Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Тур	
0.19		0.25	9.80	10.00	10.20	3.80	3.90	4.00	5.80	6.00	6.20	1.27 BSC	

	Symbol Parameter (Unit : mm)										
	h			L		θ					
Min	Nom	Max	Min	Nom	Max	Min	Nom	Max			
0.30		0.50	0.40		0.80	0		<b>8</b> °			



## Package configuration

Package type: SOP-16



## Ordering Information

Package Item	Package Type	Chip Type	Wafer Type
TTP136G-AOBN	SOP-16	No support	No support
TTP136G-BOB	SOP-16	No support	No support

## **Revision History:**

1. 2021/11/11: Version: 1.0

Original version.