20-Key Touch MTP MCU

Patent

PATENT :『電流源控制及補償觸控電容感測方法及其裝置』
PAT NO. I339356 (Taiwan)
PAT NO. ZL 2007 1 0202087. 0 (CHINA)
PATENT :『具環境變化校正的電容式觸控感測裝置』
PAT NO. M383780 (Taiwan)
PAT NO. ZL 2010 2 0141537. 7 (CHINA)
PATENT :『省電型多鍵觸摸開關感測裝置』
PAT NO. M375250 (Taiwan)
PAT NO. ZL 2010 2 0302392. 4 (CHINA)

General Description:

TTR051 MCU is an easy-used 4-bit CPU base microcontroller. It contains 4032-word ROM, 384-nibble RAM, timer/Counter, interrupt service, IO control hardware, PWM output, IIC function, LVR, ADC and touch pad feature for specified applications. The device is also suitable for diverse simple applications in control appliance and consumer product.

Features:

1. Tontek RISC 4-bit CPU core
2. Total 26 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
4. Advance CMOS process
5. Working memory with 4032*16 program ROM and 384*4 SRAM
6. 4-level stacks
7. The MCU will go into low speed operation mode (RC32K on and RC8M off) automatically after power on or reset release
8. The CPU operation frequency comes from system clock divided by register.
9. LDO voltage can select 2.3V or 2.5V or 2.7V output by register
10. LVR voltage 2.0V
11. Provides a two-wire serial interface (IIC-BUS) with read/write buffers, eliminating the need to pull down the SCL BUS to ensure full speed execution (8 bytes buffers for write command, 2 bytes buffers for read command)
12. Provide 20 pins with touch pad detection
13. Touch reference voltage can select 5/14, 6/14, 7/14, 8/14, 9/14 V_{TP} by register
14. Provides hardware Touch Pad scanning and provides up to 6 blocking buffers to record scan results
15. Provides hardware sleep function with two sets of 12-bit count value settings, divided into two modes, high speed and low speed, when the high speed mode trigger is provided

by the low frequency clock counter (TB1)

16. Correct the reference time of the low frequency clock counter (TB1, TB2) via an accurate high frequency
17. Charge and discharge sequence control (CDSC) for touch sensor function
18. Provide high frequency hardware frequency shifting function (OSCHADJ), synchronized with touch function, no shifting when touch stops and Cs initial
19. Provide MCKS duty cycle random sequence mode to reduce EMI interference
20. Operating voltage: 2.2V~5.5V(LVR=2.0V)
21. System operating frequency: (at VDD=5V)
    - High-speed RC oscillator (RC8M):
      - Built-in RC oscillator:8MHz (typical) ± 5%
      - High-speed system clock (OSCH): 4MHz (typical)
    - Low speed RC oscillator (RC32K):
      - Built-in RC oscillator: 32KHz (typical) ± 30%
      - Low-speed peripheral clock(OSCL): 32KHz (typical)
22. Provide 4 IO+20 touch pad or 24 general programmable IO
    - IO port built-in key wake-up feature enable by software setting
    - Provide external interrupt inputs
    - Provide internal signal outputs, like PWM
23. Two time base
    - Time base offers 2 various period interrupt request
24. Two 8-bit TCP1/TCP2 auto-reload timer/counter
    - 4 timer clock sources selected by software
25. One 12-bit TCP3 auto-reload timer/counter, can improve PWM function
    - 4 timer clock sources selected by software
26. Built-in 5 set 12-bit PWM with period-adjustment / positive-negative-output function
27. 8-channel 12-bit ADC
    - Built-in reference 2V reference voltage
    - AIN7 can be select built-in reference 2V
    - AIN0~AIN6 can be input externally
28. MCU system protection and power saving controlled mode
    - Built-in watch dog timer (WDT) circuit
    - Built-in low voltage reset (LVR) function
    - ROM code error detection
    - Provide high/low system operating speed, sleep and stop mode for power saving control
29. Provide 15 interrupt sources
    - External: INT0, INT1 shared with IO pad
    - Internal: two time base, three timer/counter
    - Three touch pad’s interrupt

- Four IIC interrupt
- One ADC interrupt

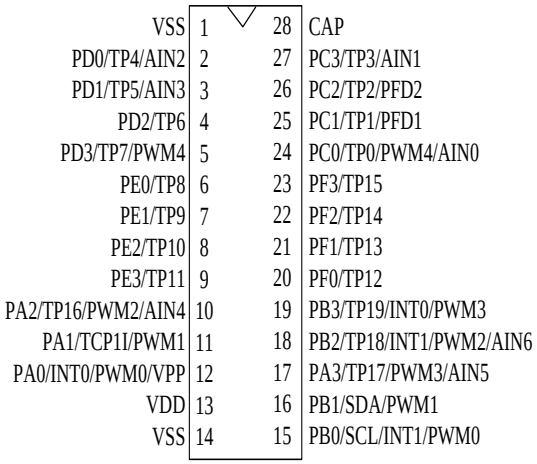
30. Provide package types
    SSOP28、SSOP24、TSSOP20

Applications:

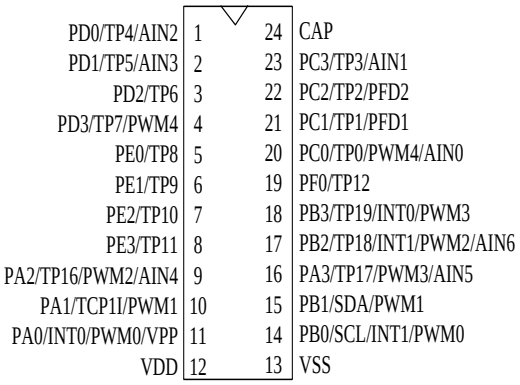
1. Household electric appliances
2. Consumer products
3. Measurement controller

Package Description:

For reference, the actual design will be official in the future



SSOP28-A



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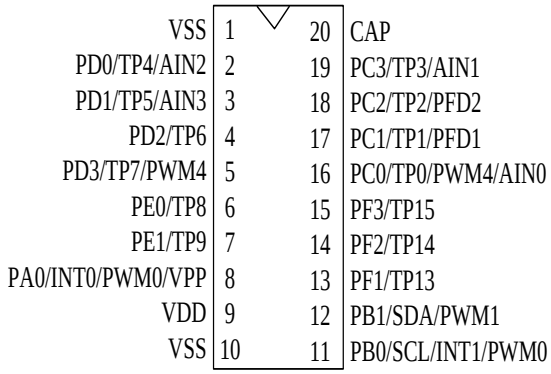
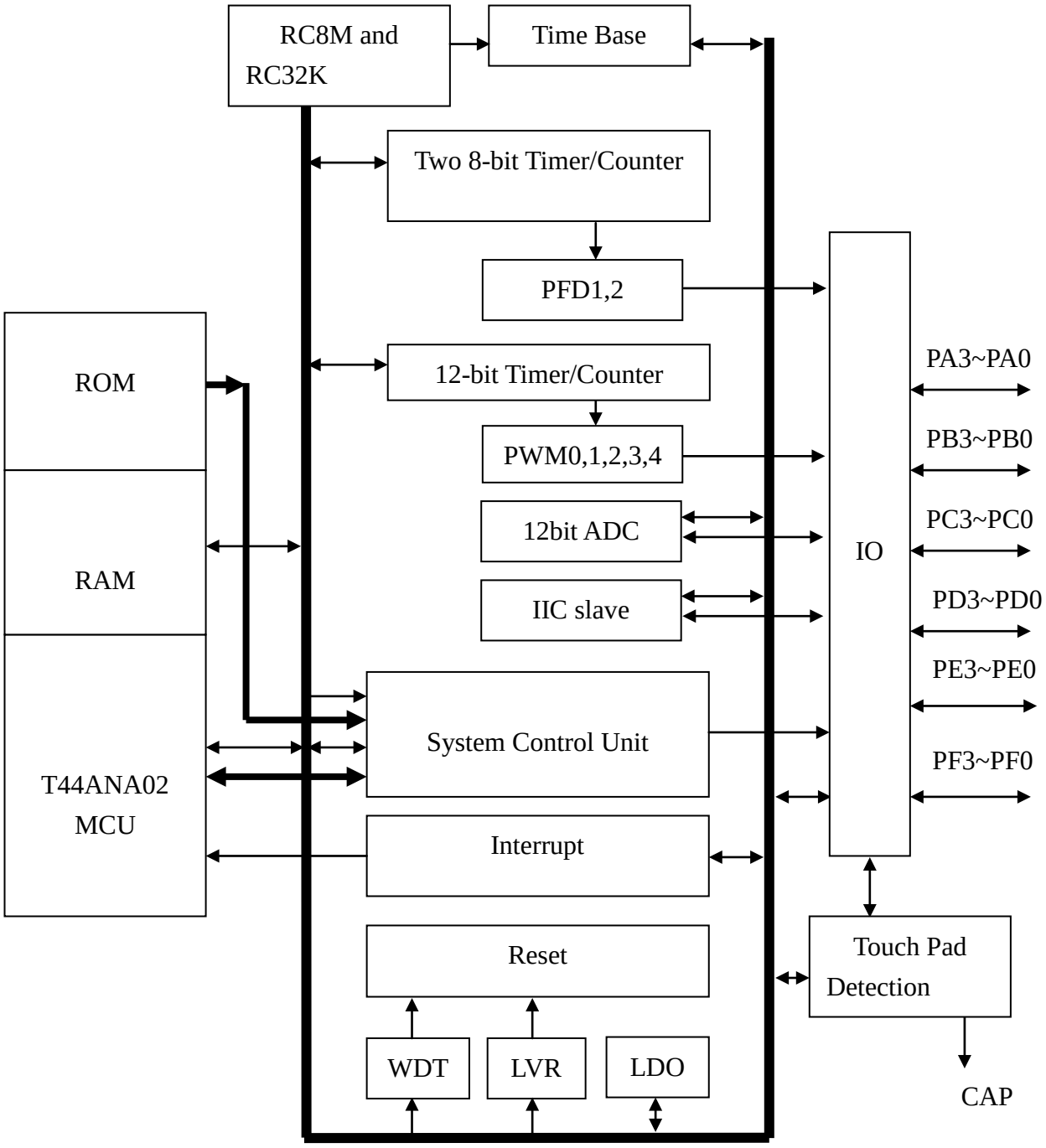


TSSOP20-A

Block Diagram:



Pin Description:

Pin Name	Share Pin	IO	Pin No.	Pin Description
VDD	-	Power	+2	Positive power supply.
VSS	-	Power	+3	Negative power supply, ground.
PA0 PA1 PA2 PA3	INT0/PWM0/VPP TCP1I/PWM1 TP16/PWM2/AIN4 TP17/PWM3/AIN5	IO/I/O IO/I/O IO/I/O IO/I/O	+4	IO port with external interrupt input, external clock input and PWM output. PA0 is shared with external interrupt input, PA1 is shared with external clock input, PA2,PA3 are shared with touch pad input. PA2,PA3 are shared with ADC input.
PB0 PB1 PB2 PB3	SCL/INT1/PWM0 SDA/PWM1 TP18/INT1/PWM2/AIN6 TP19/INT0/PWM3	IO/I/O IO/O IO/I/O IO/I/O	+4	IO port with internal IICBUS, external interrupt input and PWM output. PB0,PB1 are shared with internal IICBUS, PB0,PB2,PB3 are shared with external interrupt input. PB2,PB3 are shared with touch pad input. PB2 is shared with ADC input.
PC0 PC1 PC2 PC3	TP0/PWM4/AIN0 TP1/PFD1 TP2/PFD2 TP3/AIN1	IO/I/O IO/I/O IO/I/O IO/I	+4	IO port or touch pad input. PC0 is shared with PWM output. PC1, PC2 are shared with PFD output. PC0,PC3 are shared with ADC input.
PD0 PD1 PD2 PD3	TP4/AIN2 TP5/AIN3 TP6 TP7/PWM4	IO/I IO/I IO/I IO/I/O	+4	IO port or touch pad input. PD3 is shared with PWM output. PD0,PD1are shared with ADC input.
PE0 PE1 PE2 PE3	TP8 TP9 TP10 TP11	IO/I IO/I IO/I IO/I	+4	IO port or touch pad input.
PF0 PF1 PF2 PF3	TP12 TP13 TP14 TP15	IO/I IO/I IO/I IO/I	+4	IO port or touch pad input.
CAP	-	O	+1	Touch signal output.
Total Pad	-	-	30	

IO Cell Type Description:

Pin Name	IO Type	Description
PA0	Figure IO-C	STD IO share with external interrupt trigger input and PWM output.
PA1	Figure IO-G	STD IO share with TCP1 clcok input and PWM output.
PA2~PA3	Figure IO-B	STD IO share with touch pad input and ADC input and PWM output.
PB0	Figure IO-F	STD IO share with external interrupt trigger input and PWM output and IIC-BUS.
PB1	Figure IO-E	STD IO share with PWM output and IIC-BUS.
PB2	Figure IO-J	STD IO share with touch pad input and external interrupt trigger input and ADC input and PWM output.
PB3	Figure IO-D	STD IO share with touch pad input and external interrupt trigger input with bandgap and PWM output.
PC0	Figure IO-B	STD IO share with touch pad input and ADC input and PWM output.
PC1~PC2	Figure IO-H	STD IO share with touch pad input and internal PFD output.
PC3	Figure IO-I	STD IO share with touch pad input and ADC input.
PD0~ PD1	Figure IO-I	STD IO share with touch pad input and ADC input.
PD2	Figure IO-A	STD IO share with touch pad input.
PD3	Figure IO-K	STD IO share with touch pad input and PWM output.
PE0~PE3	Figure IO-A	STD IO share with touch pad input.
PF0~PF3	Figure IO-A	STD IO share with touch pad input.

Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-40~+85	℃
Storage Temperature	Tst	-50~+125	℃
Supply Voltage	VDD	VSS-0.3~VSS+6.0	V
MTP Supply Voltage	VPP	VSS-0.3~VSS+9	V
Input Voltage	Vin	VSS-0.3~VDD+0.3	V
Human Body Mode	ESD	MIL-STD Class 3A (4KV~8KV)	
Note: VSS symbolizes for system ground.			

DC and AC Characteristics

DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	F_{CPU}=4MHz, LVR on 2.0V	2.2	-	5.5	V
Low Voltage Reset (LVR)	V_{LVR}	LVR 2.0V	-	2.0	2.1	V
Operating Current (Normal Mode, CPU working, IO no load)	I_{nd1}	VDD=5.0V, no load, RC32K on, RC8M on, F_{CPU}=4MHz LVR on, LDO off, bandgap off, ADC off	-	2.5	3	mA
	I_{nd2}	VDD=5.0V, no load, RC32K on, RC8M off, F_{CPU}=32KHz, , LVR on, LDO off, bandgap off, ADC off	-	30	50	uA
Operating Current (Sleep Mode, CPU stop, IO no load)	I_{sd1}	VDD=5.0V, no load, RC32K on, RC8M on, LVR on, LDO off, bandgap off, ADC off	-	0.9	1.3	mA
	I_{sd2}	VDD=3.0V, no load, RC32K on, RC8M off, LVR on, LDO off, bandgap off, ADC off	-	7	12	uA
Standby Current (Stop Mode, CPU stop, IO no load)	I_{sd3}	VDD=5.0V, no load, RC32K off, RC8M off, LVR on, LDO off, bandgap off, ADC off	-	-	3	uA
LVR Current	I_{LVR}	VDD=5.0V	-	1	2	uA
Input Ports	V_{IL1}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH1}	Input High Voltage	0.8	-	1.0	VDD

PA0 Sink Current	I_{OL1}	VDD=5.0V, VOL=0.6V	-	2	-	mA
PA0 Source Current	I_{OH1}	VDD=5V, VOH=4.3V	-	-1	-	mA
Output port Sink Current (PA,PB,PC,PD,PE,PF except PA0)	I_{OL3}	VDD=5.0V, VOL=0.6V	-	8	-	mA
Output Port Source Current (PA,PB,PC,PD,PE,PF except PA0)	I_{OH3}	VDD=5V, VOH=4.3V	-	-4	-	mA
IO Port Pull-up Resistor	R_{PH1}	VDD=5.0V	100	150	200	KΩ
Bandgap Current	I_{BGAP}	VDD=5.0V	-	150	-	uA
Bandgap Voltage	V_{BGAP}		0.97	1.0	1.03	V
Bandgap Settling Time	T_{STBG}		-	100	-	us
TP Comparator current	I_{CP}	VDD=5.0V	-	60	-	uA
LDO CHARACTERISTICS						
LDO Voltage (LDO)	V_{LDO1}	LDO select 2.7V	2.4	2.7	3.0	V
	V_{LDO2}	LDO select 2.5V	2.2	2.5	2.8	V
	V_{LDO3}	LDO select 2.3V	2.0	2.3	2.6	V
LDO Current	I_{LDO}	VDD=5V,		30		uA
LDO OFF -> ON Stable Time	T_{STB}			100		uS
ADC CONVERTER CHARACTERISTICS						
Resolution	N_R				12	bit
Integral Non-Linearity error	ADC_{INL}			±3		LSB
Differential Non-Linearity error	ADC_{DNL}			±3		LSB
A/D clock period	TAD				2	MHZ
Conversion time (not Including acquisition time)	TCNV			80TAD		TAD
Acquisition Time	TACQ			32TAD		TAD

AC Characteristics: (Test condition at room temperature=25°C)

Parameter	Test Condition		Min.	Typ.	Max.	Unit
Interrupt input	Low active pulse width t_{INT}		2	-	-	CPU clock
Wake up input	Low active pulse width t_{WKUP}, Application de-bounce should be manipulated by user' software		2	-	-	OSCL
System Oscillator Frequency	RC8M (Built-in RC)	VDD=5.0V	7.6M	8M	8.4M	Hz
Peripheral Oscillator Frequency	RC32K (Built-in RC)(OSCL)	VDD=5.0V	22K	32K	42K	Hz
Startup Period of system clock	T_{OSCH} (Built-in RC)	wake-up from off mode	8	-	-	T_{OSCH}
	T_{OSCL} (Built-in RC)	Wake-up from off mode	8	-	-	T_{OSCL}
Stable Time of System Clock Switching	T_{OSCH} (Built-in RC)	OSCL→OSCH and OSCH off	8	-	-	T_{OSCL}
	(If H/L=0 then OSCH stop)					
	T_{OSCL} (Built-in RC)	OSCH→OSCL and OSCL on	8	-	-	T_{OSCL}
Timer/Counter input clock frequency	Input frequency rating, no de-bounce circuit built-in, VDD=5V		DC	-	4M	Hz
System Stable Time after Power up	After power up, the system needs to initialize the configured state and OST.		-	-	40	ms
Bandgap Stable Time			-		100	us

Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~FBF_H	-	Program ROM [4032*16]
-	000_H~007_H	File Registers
-	008_H~$01F_H$	Peripheral registers (I)
-	020_H~$19F_H$	Working RAM [384*4]
-	200_H~303_H	Peripheral registers (II)

Interrupt Vectors:

Interrupt Vectors	Function Description
$000	Hardware reset
$001	Hardware interrupt

Peripheral registers I:

Address	Symbol	R/W	Default	Description
000_H	(DP1)	R/W	----	Indirect addressing register
001_H	ACC	R/W	xxxx	Accumulator and Read Table 1st data
002_H	TB1	R/W	xxxx	Read Table 2nd data
003_H	TB2	R/W	xxxx	Read Table 3rd data
004_H	TB3	R/W	xxxx	Read Table 4th data
005_H	DPL	R/W	xxxx	Data Pointer low nibble data
006_H	DPM	R/W	xxxx	Data Pointer middle nibble data
007_H	DPH	R/W	xxxx	Data Pointer high nibble data

Peripheral Registers II:

Address	Symbol	R/W	Default	Description
008_H	PS	R/W	-000	CPU power saving control register
009_H	PSP	R/W	0000	Peripheral function control register
$00A_H$	INTC	R/W	0000	Interrupt enable control register
$00B_H$	INTF	R/W	0000	Interrupt request flag register
$00C_H$	INTC1	R/W	0000	Extended interrupt enable control register
$00D_H$	INTF1	R/W	0000	Extended interrupt request flag register
$00E_H$	TPINTC	R/W	000-	Touch pad interrupt control register
$00F_H$	TPINTF	R/W	000-	Touch pad interrupt request flag register
010_H	PAC	R/W	1111	Port A IO control register
011_H	PA	R/W	1111	Port A output data register
012_H	PBC	R/W	1111	Port B IO control register
013_H	PB	R/W	1111	Port B output data register
014_H	PCC	R/W	1111	Port C IO control register
015_H	PC	R/W	1111	Port C output data register
016_H	PDC	R/W	1111	Port D IO control register
017_H	PD	R/W	1111	Port D output data register
018_H	PEC	R/W	1111	Port E IO control register
019_H	PE	R/W	1111	Port E output data register
$01A_H$	PFC	R/W	1111	Port F IO control register
$01B_H$	PF	R/W	1111	Port F output data register
$01E_H$	IICINTC	R/W	0000	IIC interrupt enable control register
$01F_H$	IICINTF	R/W	0000	IIC interrupt request flag register
200_H	PAI	R	----	Port A pad data reading address register
201_H	PBI	R	----	Port B pad data reading address register
202_H	PCI	R	----	Port C pad data reading address register
203_H	PDI	R	----	Port D pad data reading address register
204_H	PEI	R	----	Port E pad data reading address register
205_H	PFI	R	----	Port F pad data reading address register
209_H	LDOCON	R/W	--00	LDO control register
$20A_H$	TBC	R/W	1111	Time base control register
$20B_H$	CPUFS	R/W	--00	CPU frequency division’s register
$20C_H$	INTTS	R/W	0000	INT trigger type selector register
$20D_H$	CDSC	R/W	-000	Touch scan frequency phase swap setting
$20E_H$	SPCON	R/W	0-00	Special control register
$20F_H$	TCPFS2	R/W	-000	TCP3 clock source FS pre-scale register
210_H	TCPFS1	R/W	-000	TCP1 and TCP2 clock source FS pre-scale register

211_H	TCP1L	R/W	Xxxx	TCP1 Timer/counter low nibble data register
212_H	TCP1H	R/W	Xxxx	TCP1 Timer/counter high nibble data register
213_H	TCP1C	R/W	0000	TCP1 Timer/counter control register
214_H	TCP2L	R/W	Xxxx	TCP2 Timer/counter low nibble data register
215_H	TCP2H	R/W	Xxxx	TCP2 Timer/counter high nibble data register
216_H	TCP2C	R/W	0000	TCP2 Timer/counter control register
218_H	OSCHADJ	R/W	0000	OSCH frequency adjustment register
219_H	ADJSTAT	R	--11	Frequency adjustment status flag register
$21A_H$	TBLDRL	R	0000	Time base preload low nibble data register
$21B_H$	TBLDRH	R	1000	Time base preload high nibble data register
$21F_H$	ODATA	R/W	0000	Touch pad output register for special function
220_H	PWMSTS0	R/W	0000	PWM start level selector register 0
221_H	PWMSTS1	R/W	---0	PWM start level selector register 1
222_H	PWMPS0	R/W	0000	PWM IO Port selector register 0
223_H	PWMPS1	R/W	---0	PWM IO Port selector register 1
224_H	PWMC0	R/W	0000	PWM control register 0
225_H	PWMC1	R/W	---0	PWM control register 1
226_H	PWM0L	R/W	Xxxx	PWM0 duty low nibble data register
227_H	PWM0M	R/W	Xxxx	PWM0 duty middle nibble data register
228_H	PWM0H	R/W	Xxxx	PWM0 duty high nibble data register
229_H	PWM1L	R/W	Xxxx	PWM1 duty low nibble data register
$22A_H$	PWM1M	R/W	Xxxx	PWM1 duty middle nibble data register
$22B_H$	PWM1H	R/W	Xxxx	PWM1 duty high nibble data register
$22C_H$	PWM2L	R/W	Xxxx	PWM2 duty low nibble data register
$22D_H$	PWM2M	R/W	Xxxx	PWM2 duty middle nibble data register
$22E_H$	PWM2H	R/W	Xxxx	PWM2 duty high nibble data register
$22F_H$	PWM3L	R/W	Xxxx	PWM3 duty low nibble data register
230_H	PWM3M	R/W	Xxxx	PWM3 duty middle nibble data register
231_H	PWM3H	R/W	Xxxx	PWM3 duty high nibble data register
232_H	PWM4L	R/W	Xxxx	PWM4 duty low nibble data register
233_H	PWM4M	R/W	Xxxx	PWM4 duty middle nibble data register
234_H	PWM4H	R/W	Xxxx	PWM4 duty high nibble data register
235_H	TCP3L	R/W	Xxxx	TCP3 Timer/counter low nibble data register
236_H	TCP3M	R/W	Xxxx	TCP3 Timer/counter middle nibble data register
237_H	TCP3H	R/W	Xxxx	TCP3 Timer/counter high nibble data register
238_H	TCP3C	R/W	0000	TCP3 Timer/counter control register
$23E_H$	CSAL	R/W	0000	Touch pad C load low nibble
$23F_H$	CSAH	R/W	-000	Touch pad C load high nibble
240_H	MCKS	R/W	0111	Modulation clock selector register

241_H	TPCON0	R/W	-00-	Touch pad control 0 register
242_H	TPCON1	R/W	-010	Touch pad control 1 register
243_H	TPCHS0	R/W	0000	Touch pad channel selector 0 register
244_H	TPCHS1	R/W	0000	Touch pad channel selector 1 register
245_H	TPCHS2	R/W	0000	Touch pad channel selector 2 register
246_H	TPCHS3	R/W	0000	Touch pad channel selector 3 register
247_H	TPCHS4	R/W	0000	Touch pad channel selector 4 register
248_H	TPCTL	R/W	-000	Touch pad control register
249_H	TPCT0	R/W	1111	Touch pad duty counter 0 register
$24A_H$	TPCT1	R/W	1111	Touch pad duty counter 1 register
$24B_H$	TPCT2	R/W	1111	Touch pad duty counter 2 register
$24C_H$	TPSLPS	R	--00	Touch pad sleep status register
$24E_H$	TPACT00	R	0000	TP Auto measurement counter 0_0 register
$24F_H$	TPACT01	R	0000	TP Auto measurement counter 0_1 register
250_H	TPACT02	R	0000	TP Auto measurement counter 0_2 register
251_H	TPACT10	R	0000	TP Auto measurement counter 1_0 register
252_H	TPACT11	R	0000	TP Auto measurement counter 1_1 register
253_H	TPACT12	R	0000	TP Auto measurement counter 1_2 register
254_H	TPACT20	R	0000	TP Auto measurement counter 2_0 register
255_H	TPACT21	R	0000	TP Auto measurement counter 2_1 register
256_H	TPACT22	R	0000	TP Auto measurement counter 2_2 register
257_H	TPACT30	R	0000	TP Auto measurement counter 3_0 register
258_H	TPACT31	R	0000	TP Auto measurement counter 3_1 register
259_H	TPACT32	R	0000	TP Auto measurement counter 3_2 register
$25A_H$	TPACT40	R	0000	TP Auto measurement counter 4_0 register
$25B_H$	TPACT41	R	0000	TP Auto measurement counter 4_1 register
$25C_H$	TPACT42	R	0000	TP Auto measurement counter 4_2 register
$25D_H$	TPACT50	R	0000	TP Auto measurement counter 5_0 register
$25E_H$	TPACT51	R	0000	TP Auto measurement counter 5_1 register
$25F_H$	TPACT52	R	0000	TP Auto measurement counter 5_2 register
261_H	IICCON	R/W	0000	IIC control register
262_H	IICSTS	R/W	0001	IIC status register
263_H	IICDATL	R	Xxxx	IIC data low nibble register
264_H	IICDATH	R	Xxxx	IIC data high nibble register
265_H	IICRDATL0	R/W	0000	IIC read data low nibble register 0
266_H	IICRDATH0	R/W	0000	IIC read data high nibble register 0
267_H	IICRDATL1	R/W	0000	IIC read data low nibble register 1
268_H	IICRDATH1	R/W	0000	IIC read data high nibble register 1
269_H	IICDACNT	R	0000	IIC data RX count register

$26A_H$	IICWDATL0	R/W	0000	IIC write data low nibble register 0
$26B_H$	IICWDATH0	R/W	0000	IIC write data high nibble register 0
$26C_H$	IICWDATL1	R/W	0000	IIC write data low nibble register 1
$26D_H$	IICWDATH1	R/W	0000	IIC write data high nibble register 1
$26E_H$	IICWDATL2	R/W	0000	IIC write data low nibble register 2
$26F_H$	IICWDATH2	R/W	0000	IIC write data high nibble register 2
270_H	IICWDATL3	R/W	0000	IIC write data low nibble register 3
271_H	IICWDATH3	R/W	0000	IIC write data high nibble register 3
272_H	IICWDATL4	R/W	0000	IIC write data low nibble register 4
273_H	IICWDATH4	R/W	0000	IIC write data high nibble register 4
274_H	IICWDATL5	R/W	0000	IIC write data low nibble register 5
275_H	IICWDATH5	R/W	0000	IIC write data high nibble register 5
276_H	IICWDATL6	R/W	0000	IIC write data low nibble register 6
277_H	IICWDATH6	R/W	0000	IIC write data high nibble register 6
278_H	IICWDATL7	R/W	0000	IIC write data low nibble register 7
279_H	IICWDATH7	R/W	0000	IIC write data high nibble register 7
280_H	CSINIT	R/W	0000	Cs capacitor initialization timer register
282_H	RPTTM	R/W	-000	Repeat counter
283_H	TPSLPLL0	R/W	0000	TP sleep limit low value 0 register
284_H	TPSLPLL1	R/W	0000	TP sleep limit low value 1 register
285_H	TPSLPLL2	R/W	0000	TP sleep limit low value 2 register
286_H	TPSLPLH0	R/W	0000	TP sleep limit high value 0 register
287_H	TPSLPLH1	R/W	0000	TP sleep limit high value 1 register
288_H	TPSLPLH2	R/W	0000	TP sleep limit high value 2 register
290H	ADL	R	0000	A/D result data low nibble register
291H	ADM	R	0000	A/D result data middle nibble register
292H	ADH	R	0000	A/D result data high nibble register
293H	ADCHS	R/W	-000	A/D channel selector register
294H	ADCTL	R/W	0000	A/D control register
296H	ADCSTAT	R	---1	A/D conversion status register
297H	ADSEL0	R/W	0000	A/D /IO selector register 0
298H	ADSEL1	R/W	-000	A/D /IO selector register 1
300_H	RESETF	R/W	-000	Reset source flag register
301_H	TBRB	W	----	Time base clear address register
302_H	MRO	W	----	Mask option register enable address register
303_H	CLRWDT	W	----	Clear WDT 2^{nd} instruction address register
Note: a. Default means initial value after power on or reset. b. R is “read” only, W is “write” only, R/W is both of “read” and “write”.				

Definition of register bits

ADR	NAME	BIT3	BIT2	BIT1	BIT0	initial
008_H	PS	-	HL	SLEEP	STOP	-000
009_H	PSP	LDOEN	PFD2EN	PFD1EN	SPECIO	0000
$00A_H$	INTC	TB2IE	TCP2IE	TCP1IE	TB1IE	0000
$00B_H$	INTF	TB2F	TCP2F	TCP1F	TB1F	0000
$00C_H$	INTC1	TCP3IE	ADCIE	INT1IE	INT0IE	0000
$00D_H$	INTF1	TCP3F	ADCF	INT1F	INT0F	0000
$00E_H$	TPINTC	TPCTIE	TPCMPIE	TPATIE	-	000-
$00F_H$	TPINTF	TPCTF	TPCMPF	TPATF	-	000-
010_H	PAC	PAC3	PAC2	PAC1	PAC0	1111
011_H	PA	PA3	PA2	PA1	PA0	1111
012_H	PBC	PBC3	PBC2	PBC1	PBC0	1111
013_H	PB	PB3	PB2	PB1	PB0	1111
014_H	PCC	PCC3	PCC2	PCC1	PCC0	1111
015_H	PC	PC3	PC2	PC1	PC0	1111
016_H	PDC	PDC3	PDC2	PDC1	PDC0	1111
017_H	PD	PD3	PD2	PD1	PD0	1111
018_H	PEC	PEC3	PEC2	PEC1	PEC0	1111
019_H	PE	PE3	PE2	PE1	PE0	1111
$01A_H$	PFC	PFC3	PFC2	PFC1	PFC0	1111
$01B_H$	PF	PF3	PF2	PF1	PF0	1111
$01E_H$	IICINTC	TXIE	SPIE	STIE	IICIE	0000
$01F_H$	IICINTF	TXF	SPF	STF	IICF	0000
200_H	PAI	PAI3	PAI2	PAI1	PAI0	----
201_H	PBI	PBI3	PBI2	PBI1	PBI0	----
202_H	PCI	PCI3	PCI2	PCI1	PCI0	----
203_H	PDI	PDI3	PDI2	PDI1	PDI0	----
204_H	PEI	PEI3	PEI2	PEI1	PEI0	----
205_H	PFI	PFI3	PFI2	PFI1	PFI0	----
209_H	LDOCON	-	-	LDOVS1	LDOVS0	--00
$20A_H$	TBC	TB2S	TB1S2	TB1S1	TB1S0	1111
$20B_H$	CPUFS	-	-	CS1	CS0	--00
$20C_H$	INTTS	INT1TS1	INT1TS0	INT0TS1	INT0TS0	0000
$20D_H$	CDSC	-	CDSC2	CDSC1	CDSC0	-000
$20E_H$	SPCON	INTDTS	-	INT1PS	INT0PS	0-00
$20F_H$	TCPFS2	-	FS22	FS21	FS20	-000
210_H	TCPFS1	-	FS12	FS11	FS10	-000

211_H	TCP1L	TCP13	TCP12	TCP11	TCP10	xxxx
212_H	TCP1H	TCP17	TCP16	TCP15	TCP14	xxxx
213_H	TCP1C	TCP1LD	TCP1S1	TCP1S0	TCP1EN	0000
214_H	TCP2L	TCP23	TCP22	TCP21	TCP20	xxxx
215_H	TCP2H	TCP27	TCP26	TCP25	TCP24	xxxx
216_H	TCP2C	TCP2LD	TCP2S1	TCP2S0	TCP2EN	0000
218_H	OSCHADJ	FADJ1	FADJ0	FST1	FST0	0000
219_H	ADJSTAT	-	-	OSCHADJF	TBADJF	--11
$21A_H$	TBLDRL	TBLDR3	TBLDR2	TBLDR1	TBLDR0	0000
$21B_H$	TBLDRH	TBLDR7	TBLDR6	TBLDR5	TBLDR4	1000
$21F_H$	ODATA	ODATA3	ODATA2	ODATA1	ODATA0	0000
220_H	PWMSTS0	PWM3STS	PWM2STS	PWM1STS	PWM0STS	0000
221_H	PWMSTS1	-	-	-	PWM4STS	---0
222_H	PWMPS0	PWM3PS	PWM2PS	PWM1PS	PWM0PS	0000
223_H	PWMPS1	-	-	-	PWM4PS	---0
224_H	PWMC0	PWM3EN	PWM2EN	PWM1EN	PWM0EN	0000
225_H	PWMC1	-	-	-	PWM4EN	---0
226_H	PWM0L	PWM0D3	PWM0D2	PWM0D1	PWM0D0	xxxx
227_H	PWM0M	PWM0D7	PWM0D6	PWM0D5	PWM0D4	xxxx
228_H	PWM0H	PWM0D11	PWM0D10	PWM0D9	PWM0D8	xxxx
229_H	PWM1L	PWM1D3	PWM1D2	PWM1D1	PWM1D0	xxxx
$22A_H$	PWM1M	PWM1D7	PWM1D6	PWM1D5	PWM1D4	xxxx
$22B_H$	PWM1H	PWM1D11	PWM1D10	PWM1D9	PWM1D8	xxxx
$22C_H$	PWM2L	PWM2D3	PWM2D2	PWM2D1	PWM2D0	xxxx
$22D_H$	PWM2M	PWM2D7	PWM2D6	PWM2D5	PWM2D4	xxxx
$22E_H$	PWM2H	PWM2D11	PWM2D10	PWM2D9	PWM2D8	xxxx
$22F_H$	PWM3L	PWM3D3	PWM3D2	PWM3D1	PWM3D0	xxxx
230_H	PWM3M	PWM3D7	PWM3D6	PWM3D5	PWM3D4	xxxx
231_H	PWM3H	PWM3D11	PWM3D10	PWM3D9	PWM3D8	xxxx
232_H	PWM4L	PWM4D3	PWM4D2	PWM4D1	PWM4D0	xxxx
233_H	PWM4M	PWM4D7	PWM4D6	PWM4D5	PWM4D4	xxxx
234_H	PWM4H	PWM4D11	PWM4D10	PWM4D9	PWM4D8	xxxx
235_H	TCP3L	TCP3_3	TCP3_2	TCP3_1	TCP3_0	xxxx
236_H	TCP3M	TCP3_7	TCP3_6	TCP3_5	TCP3_4	xxxx
237_H	TCP3H	TCP3_11	TCP3_10	TCP3_9	TCP3_8	xxxx
238_H	TCP3C	TCP3LD	TCP3S1	TCP3S0	TCP3EN	0000
$23E_H$	CSAL	CSA3	CSA2	CSA1	CSA0	0000
$23F_H$	CSAH	-	CSA6	CSA5	CSA4	-000

240_H	MCKS	MCKS3	MCKS2	MCKS1	MCKS0	0111
241_H	TPCON0	-	-	TPNIS	CSAMODE	--00
242_H	TPCON1	-	VREFS2	VREFS1	VREFS0	-010
243_H	TPCHS0	TPEN3	TPEN2	TPEN1	TPEN0	0000
244_H	TPCHS1	TPEN7	TPEN6	TPEN5	TPEN4	0000
245_H	TPCHS2	TPEN11	TPEN10	TPEN9	TPEN8	0000
246_H	TPCHS3	TPEN15	TPEN14	TPEN13	TPEN12	0000
247_H	TPCHS4	TPEN19	TPEN18	TPEN17	TPEN16	0000
248_H	TPCTL	-	TPCTL2	TPCTL1	TPCTL0	-000
249_H	TPCT0	TPCT3	TPCT2	TPCT1	TPCT0	1111
$24A_H$	TPCT1	TPCT7	TPCT6	TPCT5	TPCT4	1111
$24B_H$	TPCT2	TPCT11	TPCT10	TPCT9	TPCT8	1111
$24C_H$	TPSLPS	-	-	TPSLPLLS	TPSLPLHB	--00
$24E_H$	TPACT00	TPACT03	TPACT02	TPACT01	TPACT00	0000
$24F_H$	TPACT01	TPACT07	TPACT06	TPACT05	TPACT04	0000
250_H	TPACT02	TPACT011	TPACT010	TPACT09	TPACT08	0000
251_H	TPACT10	TPACT13	TPACT12	TPACT11	TPACT10	0000
252_H	TPACT11	TPACT17	TPACT16	TPACT15	TPACT14	0000
253_H	TPACT12	TPACT111	TPACT110	TPACT19	TPACT18	0000
254_H	TPACT20	TPACT23	TPACT22	TPACT21	TPACT20	0000
255_H	TPACT21	TPACT27	TPACT26	TPACT25	TPACT24	0000
256_H	TPACT22	TPACT211	TPACT210	TPACT29	TPACT28	0000
257_H	TPACT30	TPACT33	TPACT32	TPACT31	TPACT30	0000
258_H	TPACT31	TPACT37	TPACT36	TPACT35	TPACT34	0000
259_H	TPACT32	TPACT311	TPACT310	TPACT39	TPACT38	0000
$25A_H$	TPACT40	TPACT43	TPACT42	TPACT41	TPACT40	0000
$25B_H$	TPACT41	TPACT47	TPACT46	TPACT45	TPACT44	0000
$25C_H$	TPACT42	TPACT411	TPACT410	TPACT49	TPACT48	0000
$25D_H$	TPACT50	TPACT53	TPACT52	TPACT51	TPACT50	0000
$25E_H$	TPACT51	TPACT57	TPACT56	TPACT55	TPACT54	0000
$25F_H$	TPACT52	TPACT511	TPACT510	TPACT59	TPACT58	0000
261_H	IICCON	ADR2	ADR1	ADR0	IICEN	0000
262_H	IICSTS	MAASF	MBB	SRWB	TXACK	0001
263_H	IICDATL	DAT3	DAT2	DAT1	DAT0	xxxx
264_H	IICDATH	DAT7	DAT6	DAT5	DAT4	xxxx
265_H	IICRDATL0	RDAT03	RDAT02	RDAT01	RDAT00	0000
266_H	IICRDATH0	RDAT07	RDAT06	RDAT05	RDAT04	0000
267_H	IICRDATL1	RDAT13	RDAT12	RDAT11	RDAT10	0000

268_H	IICRDATH1	RDAT17	RDAT16	RDAT15	RDAT14	0000
269_H	IICDACNT	IICDACT3	IICDACT2	IICDACT1	IICDACT0	0000
$26A_H$	IICWDATL0	WDAT03	WDAT02	WDAT01	WDAT00	0000
$26B_H$	IICWDATH0	WDAT07	WDAT06	WDAT05	WDAT04	0000
$26C_H$	IICWDATL1	WDAT13	WDAT12	WDAT11	WDAT10	0000
$26D_H$	IICWDATH1	WDAT17	WDAT16	WDAT15	WDAT14	0000
$26E_H$	IICWDATL2	WDAT23	WDAT22	WDAT21	WDAT20	0000
$26F_H$	IICWDATH2	WDAT27	WDAT26	WDAT25	WDAT24	0000
270_H	IICWDATL3	WDAT33	WDAT32	WDAT31	WDAT30	0000
271_H	IICWDATH3	WDAT37	WDAT36	WDAT35	WDAT34	0000
272_H	IICWDATL4	WDAT43	WDAT42	WDAT41	WDAT40	0000
273_H	IICWDATH4	WDAT47	WDAT46	WDAT45	WDAT44	0000
274_H	IICWDATL5	WDAT53	WDAT52	WDAT51	WDAT50	0000
275_H	IICWDATH5	WDAT57	WDAT56	WDAT55	WDAT54	0000
276_H	IICWDATL6	WDAT63	WDAT62	WDAT61	WDAT60	0000
277_H	IICWDATH6	WDAT67	WDAT66	WDAT65	WDAT64	0000
278_H	IICWDATL7	WDAT73	WDAT72	WDAT71	WDAT70	0000
279_H	IICWDATH7	WDAT77	WDAT76	WDAT75	WDAT74	0000
280_H	CSINIT	CSIT3	CSIT2	CSIT1	CSIT0	0000
282_H	RPTTM	-	REPT2	REPT1	REPT0	-000
283_H	TPSLPLL0	TPLL3	TPLL2	TPLL1	TPLL0	0000
284_H	TPSLPLL1	TPLL7	TPLL6	TPLL5	TPLL4	0000
285_H	TPSLPLL2	TPLL11	TPLL10	TPLL9	TPLL8	0000
286_H	TPSLPLH0	TPLH3	TPLH2	TPLH1	TPLH0	0000
287_H	TPSLPLH1	TPLH7	TPLH6	TPLH5	TPLH4	0000
288_H	TPSLPLH2	TPLH11	TPLH10	TPLH9	TPLH8	0000
290H	ADL	AD3	AD2	AD1	AD0	0000
291H	ADM	AD7	AD6	AD5	AD4	0000
292H	ADH	AD11	AD10	AD9	AD8	0000
293H	ADCHS	-	CH2	CH1	CH0	-000
294H	ADCTL	ADEN	ADCK2	ADCK1	ADCK0	0000
296H	ADCSTAT	-	-	-	ADF	---1
297H	ADSEL0	PD1/AIN3	PD0/AIN2	PC3/AIN1	PC0/AIN0	0000
298H	ADSEL1	-	PB2/AIN6	PA3/AIN5	PA2/AIN4	-000
300_H	RESETF	-	BOF	LVRF	WDTF	-000
301_H	TBRB	-	-	-	-	----
302_H	MRO	-	-	-	-	----
303_H	CLRWDT	-	-	-	-	----

System Function Description:

S-1: System oscillator

The high speed oscillator is operated in built-in RC mode. The frequency range between 7.6MHz~8.4MHz (typical at VDD=5V). The system clock (OSCH) is system oscillator frequency divided by 2.

S-2: Peripheral oscillator

The low speed oscillator is built-in an internal RC oscillator that is for low power consumption consideration and fixed peripheral device timing control. The frequency range between 22KHz~42KHz (typical at VDD=5V). The peripheral clock (OSCL) is peripheral oscillator frequency.

S-3: CPU clock

The CPU clock comes from system/peripheral clock which is controlled by H/L bit in PS register. The high speed operation frequency comes from system clock divided by CPUFS register. The low speed operation frequency comes from peripheral clock.

CPUFS[20BH]: CPU frequency division's register [R/W], power on value [--00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	CS1	CS0
Read/Write	-	-	R/W	R/W

CS2~CS0: The selector value of CPU division's register.

CS1~CS0	CPU frequency	OSCH=4MHz
00	OSCH/1	4MHz
01	OSCH/2	2MHz
10	OSCH/4	1MHz
11	OSCH/8	500KHz

OSCH=RC8MHz/2

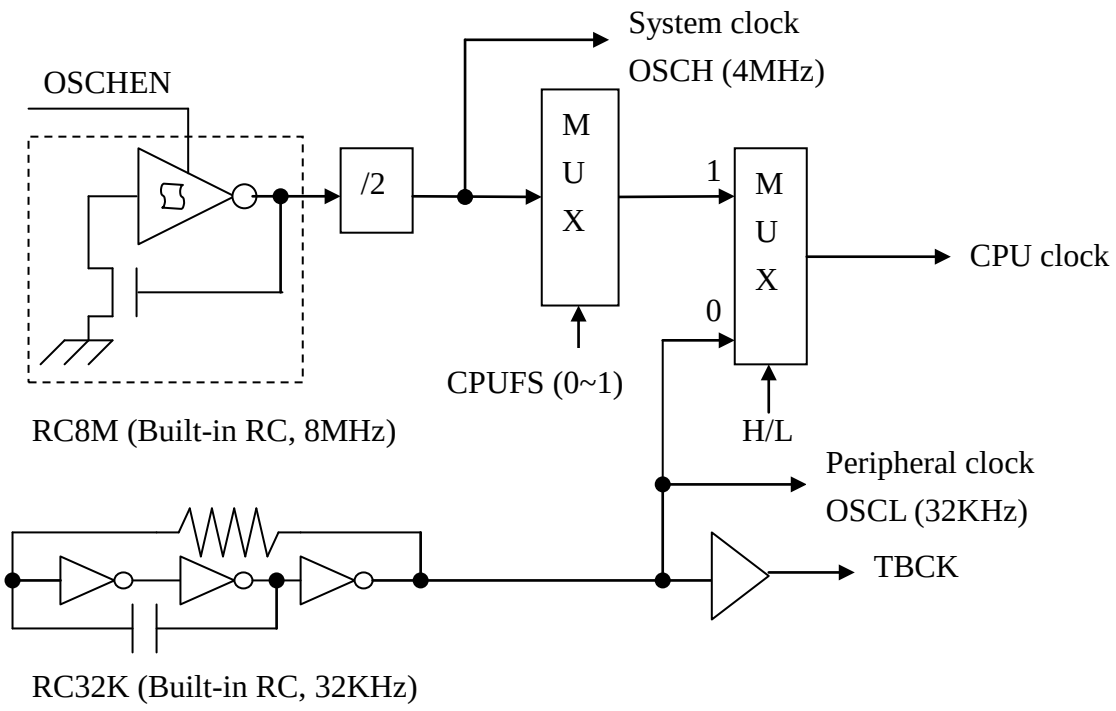


Figure: System/Peripheral Oscillator and CPU Clock Sources

S-4: Power Saving Mode (Stop mode and Sleep mode)

The CPU enters stop or sleep mode is operated by writing CPU power saving control register (PS). During the power saving mode, CPU holds the internal status of the system. In stop mode, the oscillator clocks will be stopped and system need a warm-up time for the stability of system clock running after wake up.

When the power saving mode is switched, do not perform it at the same time as the high and low speed switching. Switch to low speed before setting the power saving mode. The instruction that follow the STOP or SLEEP mode (set by PS register) must be NOP, and two NOP instructions must be followed, it make sure to wake up success.

Example: set low speed sleep from high speed.

```
STX     #$2,PS          or          ORI     #$2,PS,M
NOP                                 NOP
NOP                                 NOP
```

S-5: MCU System Operation Mode

The MCU has 4 operating modes, including high-speed operation, low speed operation, sleep and stop modes. The MCU will go into low speed operation mode (RC32K on and RC8M off) automatically after power on or reset release. After wake up from sleep mode, the MCU will resume the last operation mode.

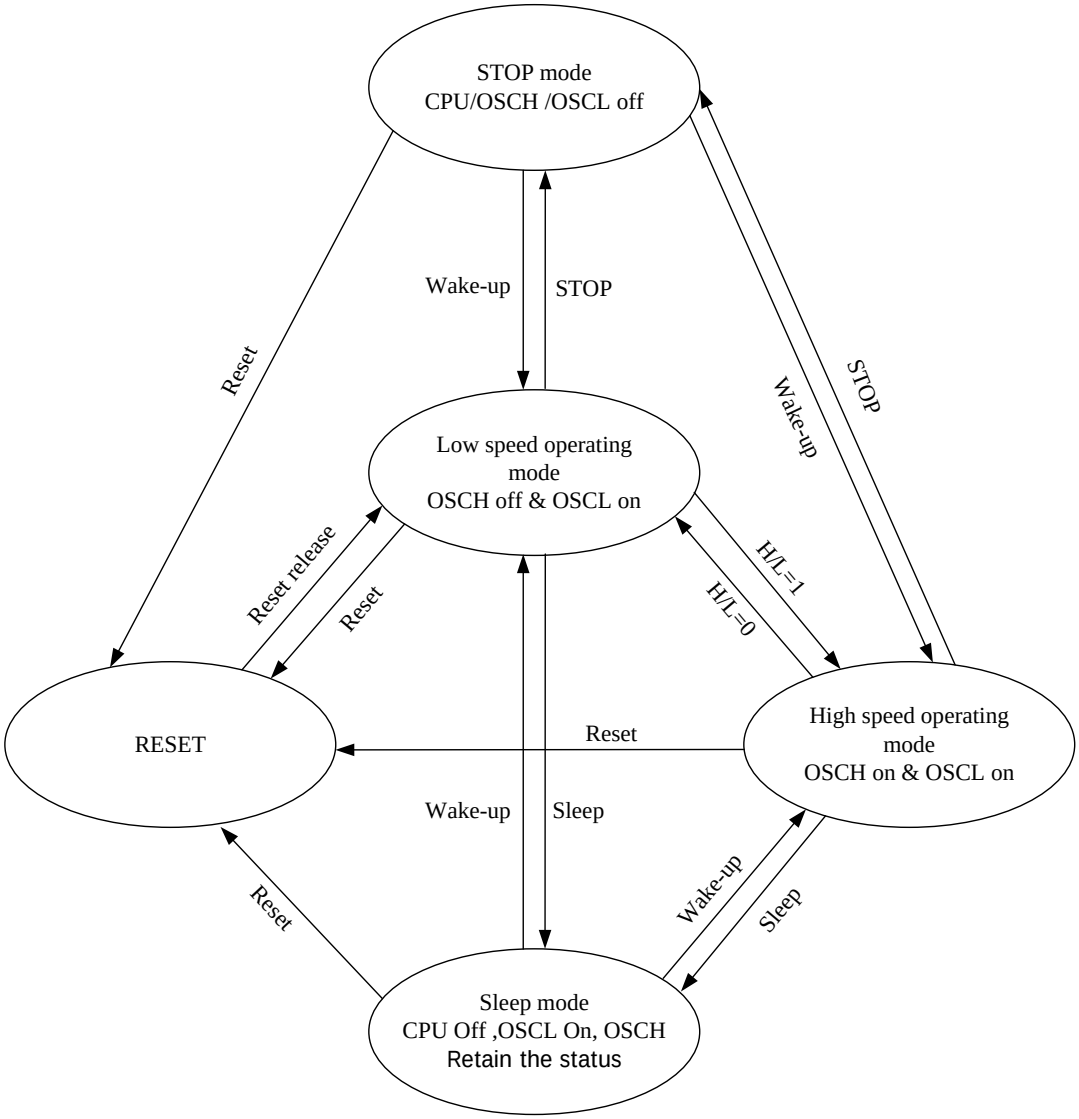


Figure: System Operation State Diagram

* Power saving mode condition and release

Modes	Stop Mode	Sleep Mode
High speed oscillator	Stopped	Stopped as H/L=0
		Keep operating as H/L=1
Low speed oscillator	Stopped	Keep operating
CPU clock	Stopped	Stopped
CPU internal status	Stop and retain the status	
Memory, Flag, Register, IO	Retain the status	
Program counter	Hold the next executed address	
Peripherals: Time bases, Timers, Interrupts	Stopped and retain	Keep operating
Watch dog timer	Disable and cleared	
Release condition	Reset, External INT sources, Input wake-up	Reset, Internal and External INT sources, Input wake-up

S-6: Watch Dog Timer (WDT)

The clock of watch dog timer comes from time base 1st overflow output (TB1OV).User can use the time up signal to prevent a software malfunction or abnormal sequence from jumping to an unknown memory location causing a system fatal failure. Normally, if the watch dog timer time up signal active that will reset the chip. At the same time, program and hardware can be initialized and resume system under normal operation. The chip also provides 2 steps clear watch dog command as the programmer writes INTF with F_H data first that will enable the WDT clear, and then writes CLRWDT register after. Completely finishes the two write steps will clear the watch dog timer. User should well arrange the two command steps for avoiding the dead lock loop.

Watch dog timer will be clear when reset, CPU enter sleep mode or stop mode.

User should keep in minds that always clear the WDT at main program and never clear the WDT in the interrupt routine.

The maximum period of WDT =(TB1OV cycle time) * 8

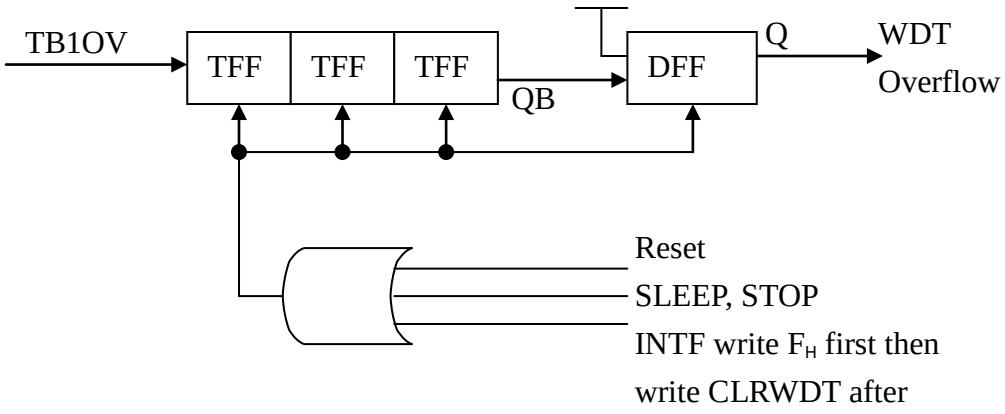


Figure: Watch Dog Timer control circuit

S-7: Low Voltage Reset (LVR)

The low voltage reset (LVR) forces the MCU in reset state during power failure, especially as MCU working in AC power application, preventing from abnormal state is the key issue. This function can not be turn off. The detected voltage is 2.0V. The voltage would have a little tolerance in different lot of chip and environment.

S-8: Reset

The chip has four kinds of reset sources: POR (power on reset), Watch dog timer overflow reset, LVR (low voltage reset) and Burn out reset. The system reset will initialize the CPU and peripheral device with default state.

- POR (power on reset)

The chip provides automatically system reset function when the power is turned on. The VDD should be below 0.5V and its rising slope (from 0.1VDD up to 0.9VDD) needs less than 10ms.

- Watch dog timer overflow reset

The system reset signal will generate automatically when the watch dog timer runs overflow. If watch dog timer is cleared regularly by users' program, no watch dog timer reset will occur. Unless the MCU is forced into abnormal state, the software controlled procedure is disrupted and causing watch dog timer overflow, and then it will generate a system reset signal to initializes the chip returning to normal operation.

- Low voltage reset (LVR)

The LVR function is used to monitor the supply voltage of MCU, it will generate a system reset signal (with 8 OSCL de-bounce time) to reset the microcontroller as the VDD power falls below the default setting level V_{LVR}.

- Burn out reset (Program sequence abnormal)

As CPU out of program area, the CPU can detect the abnormal condition and generate a system reset signal.

RESETF[300H]: Reset source flag register [R/W], power on value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	BOF	LVRF	WDTF
Read/Write	-	R/W	R/W	R/W

WDTF: Watch dog timer overflow reset flag. (0: no active; 1: active)

LVRF: Low voltage reset flag. (0: no active; 1: active)

BOF: Burn out reset flag. (0: no active; 1: active)

Note: The RESETF is only cleared by power on reset.

S-9: Power Saving Control Register

PS[008H]: Power saving control register [R/W] , default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	H/L	SLEEP	STOP
Read/write	-	R/W	R/W	R/W

STOP: Into stop mode. (0: disable; 1: enable)

SLEEP: Into sleep mode. (0: disable; 1: enable)

H/L: CPU clock selector. (1: System clock; 0: Peripheral clock)

When H/L=0, system clock oscillator is stopped.

When STOP bit is set to 1, system and peripheral clock oscillator are stopped. In STOP mode, although the H / L bit is set to 1, the system frequency is still turned off. The SLEEP bit and STOP bit will be cleared to 0 automatically when the release conditions occur from reset, interrupt or input wake up.

When the power saving mode is switched, do not perform it at the same time as the high and low speed switching. Switch to low speed before setting the power saving mode. The instruction that follow the STOP or SLEEP mode (set by PS register) must be NOP, and two NOP instructions must be followed, it make sure to wake up success.

Example: set low speed sleep from high speed.

```
STX    #$2,PS          or          ORI    #$2,PS,M
NOP                                NOP
NOP                                NOP
```

PSP[009H]: Peripheral function control register[R/W] , default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	LDOEN	PFD2EN	PFD1EN	SPECIO
Read/write	R/W	R/W	R/W	R/W

SPECIO: Special IO function selector. (0:disable; 1:enable)

PFD1EN: PFD1 output enable. (0: disable; 1: enable)

PFD2EN: PFD2 output enable. (0: disable; 1: enable)

LDOEN: LDO enable. (0: disable; 1: enable)

LDOCON[209H]: LDO control register [R/W] , default value [--00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	LDOVS1	LDOVS0
Read/write	-	-	R/W	R/W

LDOVS1~0: LDO voltage selector.

00: 2.7V.

01: 2.5V.

10: 2.3V.

11: reserved.

S-10: Special control register

SPCON [20EH]: Special control register [R/W] , default value [0-00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	INTDTS	-	INT1PS	INT0PS
Read/write	R/W	-	R/W	R/W

INT0PS: INT0 output port selector. (0: PA0; 1: PB3)

INT1PS: INT1 output port selector. (0: PB0; 1: PB2)

INTDTS: INT0 Interrupt input detector selection. (0: Schmitt; 1: comparator)

Compare reference voltage use bandgap voltage.(Only PB3 can select Schmitt or comparator, PA0 is always Schmitt.)

S-10-1 Use INT0 for LVD

INT0 input type can select Schmitt or comparator by SPCON register, if comparator select then the comparator reference voltage is the bandgap voltage(1.0+-3%), it will consumption more current than Schmitt because band gap turn on. It can be used to detect VDD voltage for battery low and so on.

S-11: OST time

The system/peripheral oscillator generates the system control timing for CPU core or peripheral devices with fixed control phase, so the waveform of oscillator becomes sensitive to noise, abnormal duty especially fatal for CPU. Any switching of clock source needs oscillation stable time (OST) to make sure the oscillation is stable and synchronized with CPU timing phase. The relative OST for different oscillator with reference value as below table:

OST	System clock(OSCH)	Peripheral clock(OSCL)
High speed STOP wakeup	-	8
Low speed STOP wakeup	-	8
High speed SLEEP wakeup	8	-
Low speed SLEEP wakeup	-	8
Low speed to High speed	-	8
High speed to Low speed	-	8

S-12: Interrupts

The CPU provides only 1 interrupt vector (001_H) and no priority, but can expand to multi-sources. Interrupt source includes external interrupts (INTxINT), timer/counter interrupts (TCPxINT), time base interrupt (TBxINT) or other peripheral device interrupt request (TPINT and IICINT). The interrupt control registers (INTC or INTC1) contain the interrupt control bits to enable and disable corresponding interrupt request and the corresponding interrupt request flags in the (INTF or INTF1) registers. Before finishing the interrupt service routine, another interrupt request will keep waiting until program return from interrupt routine.

If the interrupt request needs service, the programmer may set the corresponding interrupt enable bit to allow interrupt active. External interrupts can select trigger type by setting INTTS register, and set the related interrupt request flag (INTxF). The internal timer/counter interrupt is setting the TCPxF to 1, resulting from the timer/counter overflow. The time base interrupt was provided 2 periodic interrupt request cycles for user operating a periodic routine.

When the corresponding interrupt enable and flag bit is set to 1, the CPU will active the interrupt service routine. Then CPU reads the service flag and check the request priority then proceeds with the relative interrupt service. After CPU writes the corresponding bit to 0 in the INTFx register, the service flag will be cleared to 0(using STX #n,$m instruction). The INTF and INTF1 registers' bit can only write "0" to clear the flag. User writes "1" to flag bit with no effect.

INT0 input type can select Schmitt or comparator by INTDTS in SPCON register, if comparator select then the comparator reference voltage is the band gap voltage(1.0+-3%), it will consumption more current than Schmitt because band gap turn on. It can be used to detect VDD voltage for battery low and so on.

INTTS[20CH]: Interrupt trigger type selector register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	INT1S1	INT1S0	INT0S1	INT0S0
Read/Write	R/W	R/W	R/W	R/W

INT0S1~INT0S0: Interrupt 0 (INT0) trigger type selector.

00: Low level trigger.

01: Falling edge trigger.

10: Rising edge trigger.

11: Dual edge trigger.

INT1S1~INT1S0: Interrupt 1 (INT1) trigger type selector.

00: Low level trigger.

01: Falling edge trigger.

10: Rising edge trigger.

11: Dual edge trigger.

INTC[00AH]: Interrupt control register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TB2IE	TCP2IE	TCP1IE	TB1IE
Read/Write	R/W	R/W	R/W	R/W

TB1IE: Enable time base 1st interrupt. (0: disable; 1: enable)

TCP1IE: Enable interrupt of TCP1 timer/counter. (0: disable; 1: enable)

TCP2IE: Enable interrupt of TCP2 timer/counter. (0: disable; 1: enable)

TB2IE: Enable time base 2nd interrupt. (0: disable; 1: enable)

INTF[00BH]: Interrupt request flag register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TB2F	TCP2F	TCP1F	TB1F
Read/Write	R/W	R/W	R/W	R/W

TB1F: Time base 1st interrupt request flag. (0: inactive; 1: active)

TCP1F: TCP1 Timer/counter interrupt request flag. (0: inactive; 1: active)

TCP2F: TCP2 Timer/counter interrupt request flag. (0: inactive; 1: active)

TB2F: Time base 2nd interrupt request flag. (0: inactive; 1: active)

INTC1[00CH]: Extended interrupt control register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP3IE	ADCIE	INT1IE	INT0IE
Read/Write	R/W	R/W	R/W	R/W

INT0IE: Enable INT0 external interrupt. (0: disable; 1: enable)

INT1IE: Enable INT1 external interrupt. (0: disable; 1: enable)

ADCIE: Enable ADC interrupt. (0: disable; 1: enable)

TCP3IE: Enable TCP3 Timer/counter interrupt. (0: disable; 1: enable)

INTF1[00DH]: Extended interrupt request flag register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP3F	ADCF	INT1F	INT0F
Read/Write	R/W	R/W	R/W	R/W

INT0F: INT0 external interrupt request flag. (0: inactive; 1: active)

INT1F: INT1 external interrupt request flag. (0: inactive; 1: active)

ADCF: ADC interrupt request flag. (0: inactive; 1: active)

TCP3F : TCP3 Timer/counter interrupt request flag. (0 : inactive ; 1 : active)

TPINTC[00EH]: Touch pad interrupt control register [R/W], default value [000-]

TPINTC	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTIE	TPCMPIE	TPATIE	-
Read/Write	R/W	R/W	R/W	-

TPATIE: TP auto mode measure interrupt enable. (0: disable; 1: enable)

TPCMPIE: Capacitor overcharge interrupt enable. (0: disable; 1: enable)

TPCTIE: Duty counter overflow interrupt enable. (0: disable; 1: enable)

TPINTF[00FH]: Touch pad interrupt request flag register [R/W], default value [000-]

TPINTF	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTF	TPCMF	TPATF	-
Read/Write	R/W	R/W	R/W	-

TPATF: TP auto mode measure flag. (0: inactive; 1: active)

TPCMPF: Capacitor overcharge’s flag. (0: inactive; 1: active)

TPCTF: Duty counter’s overflow flag. (0: inactive; 1: active)

IICINTC[01EH]: IIC interrupt control register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TXIE	SPIE	STIE	IICIE
Read/Write	R/W	R/W	R/W	R/W

IICIE: Enable IIC interrupt. (0: disable; 1: enable)

STIE: Enable IIC start signal interrupt. (0: disable; 1: enable)

SPIE: Enable IIC stop signal interrupt. (0: disable; 1: enable)

TXIE: Enable IIC first byte is transmitted interrupt. (0: disable; 1: enable)

IICINTF[01FH]: IIC interrupt request flag register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TXF	SPF	STF	IICF
Read/Write	R/W	R/W	R/W	R/W

IICF: IIC interrupt request flag. (0: inactive; 1: active)

STF : IIC start signal interrupt request flag. (0 : inactive ; 1 : active)

SPF: IIC stop signal interrupt request flag. (0: inactive; 1: active)

TXF: IIC first byte is transmitted interrupt request flag. (0: inactive; 1: active)

SPCON [20EH]: Special control register [R/W] , default value [0-00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	INTDTS	-	INT1PS	INT0PS
Read/write	R/W	-	R/W	R/W

INT0PS: INT0 output port selector. (0: PA0; 1: PB3)

INT1PS: INT1 output port selector. (0: PB0; 1: PB2)

INTDTS: INT0 Interrupt input detector selection. (0: Schmitt; 1: comparator)

Compare reference voltage use bandgap voltage. (Only PB3 can select Schmitt or comparator, PA0 is always Schmitt.)

Peripheral function description:

P-1: Timer/Counter clock pre-scale

The System clock is the most high frequency divided by 2 of MCU. For various peripherals, application needs different clock source divided from system clock. TCPFSx register is a selector for choosing suitable frequency (FSx).

TCPFS1[210H]: TCP1 and TCP2 clock pre-scale register [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	FS12	FS11	FS10
Read/Write	-	R/W	R/W	R/W

FS12~FS10: The selector of TCPFS1.

FS12~FS10	FS1	FS12~FS10	FS1
000	OSCH/1	100	OSCH/16
001	OSCH/2	101	OSCH/32
010	OSCH/4	110	OSCH/64
011	OSCH/8	111	OSCH/128

OSCH: RC8M/2=4MHz.

TCPFS2[20FH]: TCP3 clock pre-scale register [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	FS22	FS21	FS20
Read/Write	-	R/W	R/W	R/W

FS22~FS20: The selector of TCPFS2.

FS22~FS20	FS2	FS22~FS20	FS2
000	OSCH/1	100	OSCH/16
001	OSCH/2	101	OSCH/32
010	OSCH/4	110	OSCH/64
011	OSCH/8	111	OSCH/128

OSCH: RC8M/2=4MHz.

P-1-1 OSC Frequency Adjustment

ADJSTAT [219H]: Frequency Adjustment Status flag register [R], default value [--11]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	OSCHADJF	TBADJF
Read/write	-	-	R	R

TBADJF: Time base adjustment status flag. (0: busy; 1: idle)

OSCHADJF: OSCH frequency adjustment status flag. (0: busy, 1: idle)

OSCHADJ [218H]: OSCH frequency adjustment register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	FADJ1	FADJ0	FST1	FST0
Read/write	R/W	R/W	R/W	R/W

FST1~FST0: Frequency Shift Time selector.

FST1~FST0	Frequency Shift Time (us)
00	6
01	10
10	16
11	20

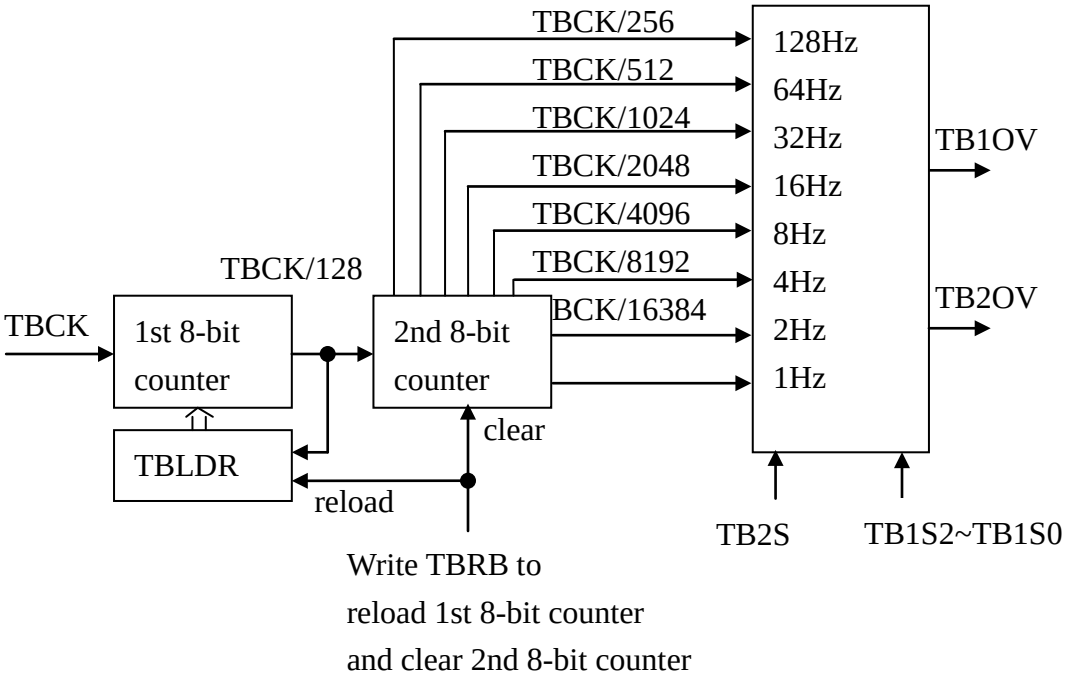
FADJ1~FADJ0: OSCH Frequency adjustment range selector.

FADJ1~FADJ0	Frequency adjustment range	Value
00	Disable	0
01	-1,0,+1	±1
10	-2,-1,0,+1,+2	±2
11	-3,-2,-1,0,+1,+2,+3	±3

First set the change time of the register FST, select FADJ to set the frequency swing range, and activate the frequency shift function. When the TP scans, the frequency shift starts to move. When the TP scan ends, the frequency will return to the frequency before the frequency shift. When the frequency shift occurs, the swing moves back and forth from the center frequency. Set FADJ = 0 to turn off the frequency shift function. When performing the frequency shift function, OSCHADJF will be set to 0. Then the user cannot change FADJ and FST, but only 0 can be set to the off function. OSCHADJF will be set to 1. The frequency shift function will stop immediately but must wait until the frequency stabilizes to return to the original frequency.

P-2: Time base

The time base has 2 interrupt sources and both of them come from the peripheral internal RC oscillator. The time base 1st overflow output (TB1OV) can cause interrupt and the period is selected by TB1S2~TB1S0 in TBC register. The time base 2nd overflow output (TB2OV) also offers two sample frequency options by TB2S bit in the TBC register.



TBC[20AH]: Time base control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TB2S	TB1S2	TB1S1	TB1S0
Read/Write	R/W	R/W	R/W	R/W

TB1S2~TB1S0: Time base 1st overflow frequency selector.

TB2S: Time base 2nd overflow frequency selector.

Note: Every time writing the TBRB will clear the time base.

TB1S2~TB1S0	TB1OV	TBCK=32KHz
000	TBCK/256	128HZ
001	TBCK/512	64HZ
010	TBCK/1024	32HZ
011	TBCK/2048	16HZ
100	TBCK/4096	8HZ
101	TBCK/8192	4HZ
110	TBCK/16384	2HZ
111	TBCK/32768	1HZ

TB2S	TB2OV	TBCK=32KHz
0	TBCK/1024	32Hz
1	TBCK/2048	16Hz

P-2-1 Adjustment time base

ADJSTAT [219H]: Frequency Adjustment Status flag register [R], default value [--11]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	OSCHADJF	TBADJF
Read/write	-	-	R	R

TBADJF: Time base adjustment status flag. (0: busy; 1: idle)

OSCHADJF: OSCH frequency adjustment status flag. (0: busy; 1: idle)

TBLDRL[21AH]: Time base preload low nibble data register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TBLDR3	TBLDR2	TBLDR1	TBLDR0
Read/Write	R	R	R	R

TBLDR3~TBLDR0: Time base preload low nibble data.

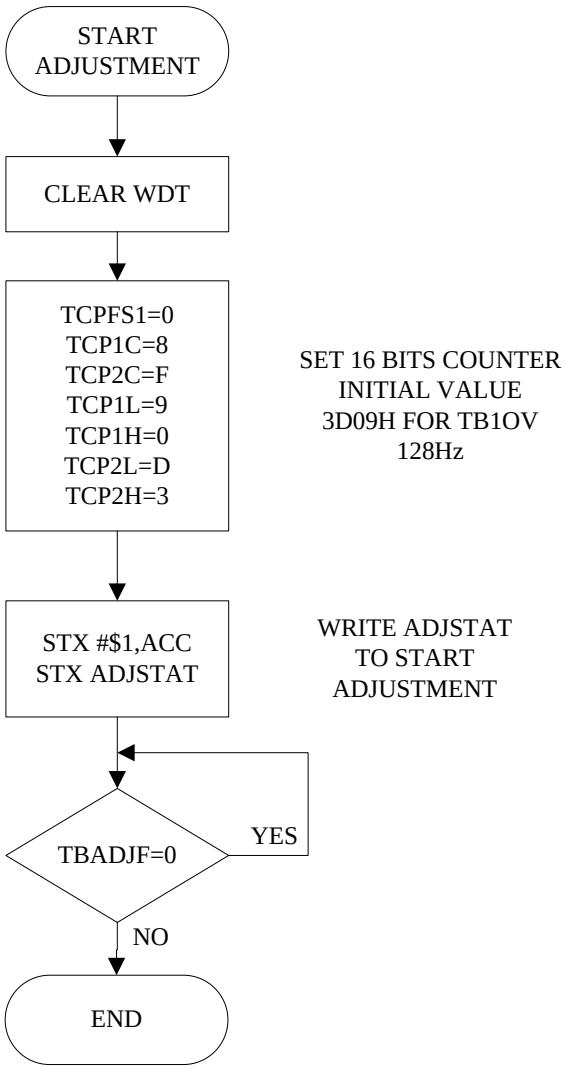
TBLDRH[21BH]: Time base preload high nibble data register [R], default value [1000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TBLDR7	TBLDR6	TBLDR5	TBLDR4
Read/Write	R	R	R	R

TBLDR7~TBLDR4: Time base preload high nibble data.

Since 32K / 128 is about 256Hz, users can adjust the time base to the exact 256Hz by modifying the first 8-bit counter preload value, the time base preload counter initial value is 80H in power on, the adjustment procedure will modify the preload counter value to approach 256Hz, there is using TCP1 and TCP2 cascaded to form a 16-bit timer/counter, chooses clock source FS and set TCPFS1=0_H for TCP1, then load $3D09_H$(4MHz/15625=256Hz) to the 16-bit counter and write 1_H to ADJSTAT register to start adjustment, then check TBADJF flag. The adjustment procedure is finished when TBADJF=1.

The adjustment procedure flow chart as follow:



P-3: 8-bit Timer/Counter for TCP1

One 8-bit timer/counters (TCP1) with 4 kind clock sources and preload data buffer can implement as a timer or counter feature. The clock source of TCP1 is selected by TCP1S1~TCP1S0 of the TCP1 control register (TCP1C). TCP1OV is the timer or counter overflow signal and the rising edge will set the relative interrupt flag.

TCP1C[213H]: TCP1 Timer/counter control register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP1LD	TCP1S1	TCP1S0	TCP1EN
Read/Write	R/W	R/W	R/W	R/W

TCP1EN: TCP1 counting enabled. (0: disable; 1: enable)

TCP1LD: TCP1 auto-reload enabled. (0: disable; 1: enable)

TCP1S1~TCP1S0: TCP1 clock source selector.

TCP1S1~TCP1S0	TCP1 clock source
00	FS1
01	TCP1I
10	TBCK
11	TB1OV

TCP1L[211H]: TCP1 low nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP13/TCP1D3	TCP12/TCP1D2	TCP11/TCP1D1	TCP10/TCP1D0
Read/Write	R/W	R/W	R/W	R/W

TCP13~TCP10: Reading TCP1 counter low nibble data.

TCP1D3~TCP1D0: Writing TCP1D low nibble of data buffer.

TCP1H[212H]: TCP1 high nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP17/TCP1D7	TCP16/TCP1D6	TCP15/TCP1D5	TCP14/TCP1D4
Read/Write	R/W	R/W	R/W	R/W

TCP17~TCP14: Reading TCP1 counter high nibble data.

TCP1D7~TCP1D4: Writing TCP1D high nibble of data buffer.

* TCP1D: Like an 8-bit TCP1 data register [R/W], default value [xxH]

TCP1D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP1D7	TCP1D6	TCP1D5	TCP1D4	TCP1D3	TCP1D2	TCP1D1	TCP1D0

The special R/W function for TCP1 has different target, AS writing TCP1H/L registers that are updating preload data of the TCP1D. As read TCP1H/L registers that are the brand new TCP1 counter value.

P-4: 8-bit Timer/Counter for TCP2

One 8-bit timer/counters (TCP2) with 4 kind clock sources and preload data buffer can implement as a timer or counter feature. The clock source of TCP2 is selected by TCP2S1~TCP2S0 of TCP2 control register (TCP2C). TCP2OV is the timer or counter overflow signal and the rising edge will set the relative interrupt flag.

TCP2C[216H]: TCP2 Timer/counter control register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP2LD	TCP2S1	TCP2S0	TCP2EN
Read/Write	R/W	R/W	R/W	R/W

TCP2EN: TCP2 counting enabled. (0: disable; 1: enable)

TCP2LD: TCP2 auto-reload enabled. (0: disable; 1: enable)

TCP2S1~TCP2S0: TCP2 clock source selector.

TCP2S1~TCP2S0	TCP2 clock source
00	FS1
01	OSCH
10	TBCK
11	TCP1OV

TCP2L[214H]: TCP2 low nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP23/TCP2D3	TCP22/TCP2D2	TCP21/TCP2D1	TCP20/TCP2D0
Read/Write	R/W	R/W	R/W	R/W

TCP23~TCP20: Reading TCP2 counter low nibble data.

TCP2D3~TCP2D0: Writing TCP2D low nibble of data buffer.

TCP2H[215H]: TCP2 low high data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP27/TCP2D7	TCP26/TCP2D6	TCP25/TCP2D5	TCP24/TCP2D4
Read/Write	R/W	R/W	R/W	R/W

TCP27~TCP24: Reading TCP2 counter high nibble data.

TCP2D7~TCP2D4: Writing TCP2D high nibble of data buffer.

* TCP2D: Like an 8-bit TCP2 data register [R/W], default value [xxH]

TCP2D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP2D7	TCP2D6	TCP2D5	TCP2D4	TCP2D3	TCP2D2	TCP2D1	TCP2D0

The special R/W function for TCP2 has different Target, AS writing TCP2H/L registers that are updating preload data of the TCP2D. As read TCP2H/L registers that are the brand new TCP2 counter value.

P-5: 12-bit Timer/Counter/PWM for TCP3

One 12-bit timer/counters (TCP3) with 4 kind clock sources and preload data buffer can implement as a timer or counter feature. The clock source of TCP3 is selected by TCP3S1~TCP3S0 of TCP3 control register (TCP3C). TCP3OV is the timer or counter overflow signal and the rising edge will set the relative interrupt flag.

TCP3C[238H]: TCP3 Timer/counter/PWM control register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP3LD	TCP3S1	TCP3S0	TCP3EN
Read/Write	R/W	R/W	R/W	R/W

TCP3EN: TCP3 counting enabled. (0: disable; 1: enable)

TCP3LD: TCP3 auto-reload enabled. (0: disable; 1: enable)

TCP3S1~TCP3S0: TCP3 clock source selector.

TCP3S1~TCP3S0	TCP3 clock source
00	FS2
01	RC8M
10	TBCK
11	TB1OV

TCP3L[235H]: TCP3 low nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP33/TCP3D3	TCP32/TCP3D2	TCP31/TCP3D1	TCP30/TCP3D0
Read/Write	R/W	R/W	R/W	R/W

TCP33~TCP30: Reading TCP3 counter low nibble data.

TCP3D3~TCP3D0: Writing TCP3D low nibble of data buffer.

TCP3M[236H]: TCP3 low middle data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP37/TCP3D7	TCP36/TCP3D6	TCP35/TCP3D5	TCP34/TCP3D4
Read/Write	R/W	R/W	R/W	R/W

TCP37~TCP34: Reading TCP3 counter high nibble data.

TCP3D7~TCP3D4: Writing TCP3D high nibble of data buffer.

TCP3H[237H]: TCP3 low high data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP311/TCP3D11	TCP310/TCP3D10	TCP39/TCP3D9	TCP38/TCP3D8
Read/Write	R/W	R/W	R/W	R/W

TCP311~TCP38: Reading TCP3 counter high nibble data.

TCP3D11~TCP3D8: Writing TCP3D high nibble of data buffer.

* TCP3D: Like an 12-bit TCP3 data register [R/W], default value [xxH]

TCP3D	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP3D11	TCP3D10	TCP3D9	TCP3D8	TCP3D7	TCP3D6	TCP3D5	TCP3D4	TCP3D3	TCP3D2	TCP3D1	TCP3D0

The special R/W function for TCP3 has different Target, AS writing TCP3H/M/L registers that are updating preload data of the TCP3D. As read TCP3H/M/L registers that are the brand new TCP3 counter value.

.Timer

When TCPx works as a timer, user needs give the preload data TCPxD for periodic interrupt. After initial setting, user starts the TCPx counting by setting.

When 8-bit timer/counter:

Tc = (selected clock cycle) * (256) if TCPxD=00H

Tc = (selected clock cycle) * (TCPxD) otherwise

When 16-bit timer/counter:

Tc = (selected clock cycle) * (65536) if TCP1D=00H and TCP2D=00H

Tc = (selected clock cycle) * (TCP2D*256+TCP1D) otherwise

When 12-bit timer/counter:

Tc = (selected clock cycle) * (4096) if TCP3D=000H

Tc = (selected clock cycle) * (TCP3D) otherwise

When user writes data to the TCPxH/L or TCP3H/M/L, the data just keep in TCPxH/L or TCP3H/M/L latch. During the TCPxEN=1 command executed, the TCPxH/L or TCP3H/M/L latch's complement value will load into counter TCPxH/L or TCP3H/M/L as initial value and start the timer function. Necessary TCPxLD=1, timer run with reload feature as TCPx up counts and reaches the value of FF_H or FFF_H for TCPx. At the same time, interrupt request flag TCPxF will set activated, if software enables the corresponding interrupt enable bit, interrupt hardware will cause MCU interrupt service routine.

.PFD

PSP[009H]: Peripheral function control register[R/W] , default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	LDOEN	PFD2EN	PFD1EN	SPECIO
Read/write	R/W	R/W	R/W	R/W

SPECIO: Special IO function selector. (0:disable; 1:enable)

PFD1EN: PFD1 output enable. (0: disable; 1: enable)

PFD2EN: PFD2 output enable. (0: disable; 1: enable)

LDOEN: LDO enable. (0: disable; 1: enable)

The PFD Mode includes in timer mode and the output frequency is:

PFD1 frequency = (selected clock frequency) / (TCP1D) / (2)

PFD2 frequency = (selected clock frequency) / (TCP2D) / (2)

When PFDxEN enable and PFDx (PC1, PC2) OUT pin change to output mode, PFDx signal will output to PFDx OUT pin

At this time, most users will disable the interrupt feature for tone or melody generation.

.Counter

Counter feature is implemented only by TCPxLD=0, the TCPxD can be zero or not that depends on software needs. User starts and stops the counter by changing the TCPxEN bit value. On the save side, reading the counter value after stopping the count by disable TCPxEN=0, if reading the counter value during value changing that means clock in happening at the same time. The reading of counter value may disrupt for transient state. If counter is not enough for counting, user can enable the interrupt and using the data RAM as software counter for extending the counter stage.

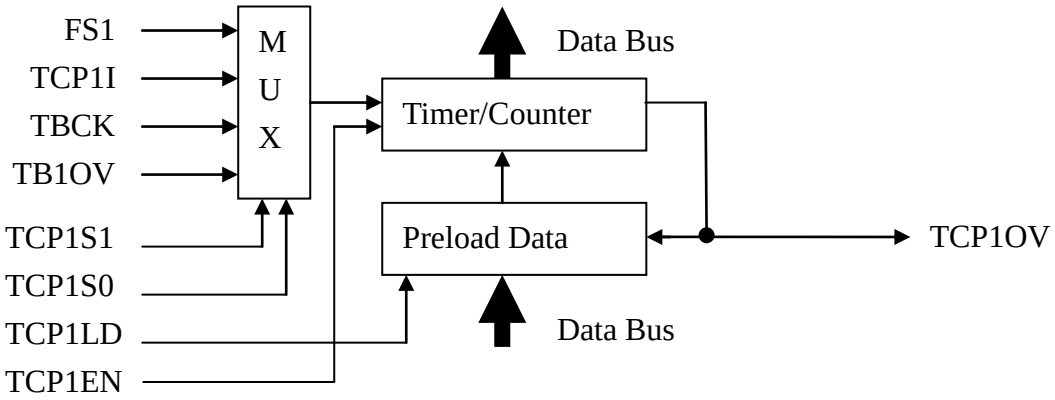


Figure: 8-bit Timer/Counter (TCP1)

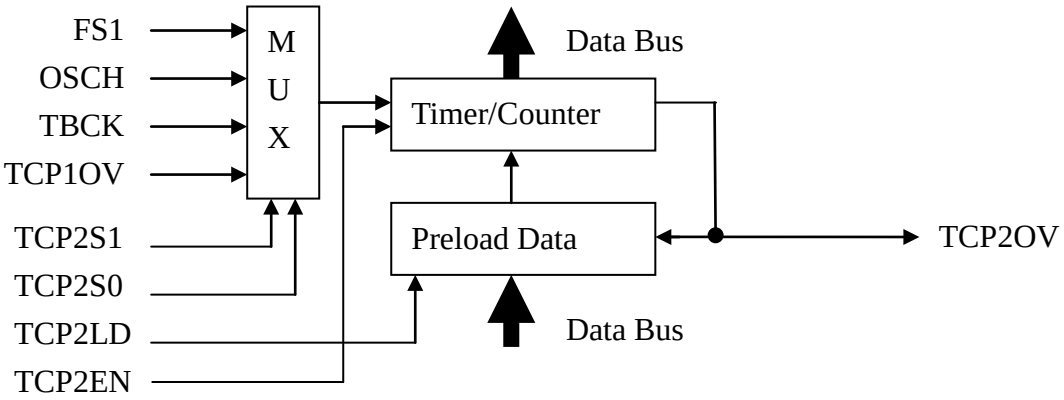


Figure: 8-bit Timer/Counter (TCP2)

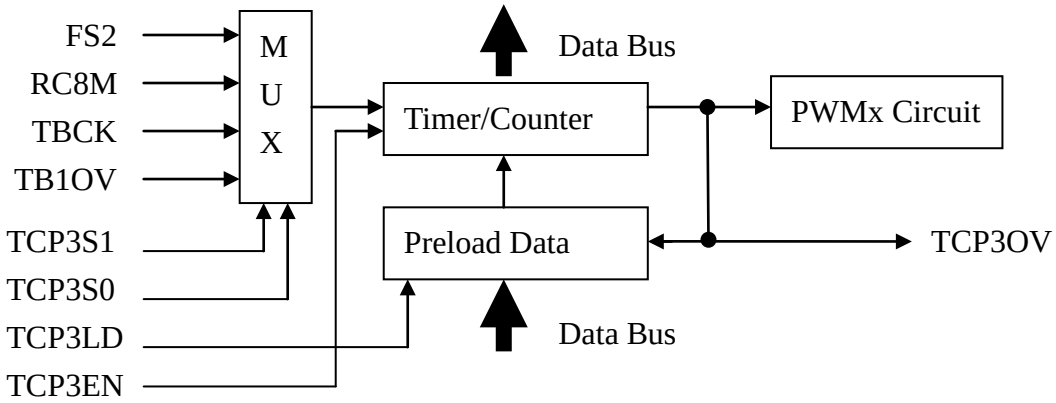


Figure: 12-bit Timer/Counter/PWM (TCP3)

TCP1S1~TCP1S0	TCP1 clock source
00	FS1
01	TCP1I
10	TBCK
11	TB1OV

	PFD Output
TCP1	PFD1

TCP2S1~TCP2S0	TCP2 clock source
00	FS1
01	OSCH
10	TBCK
11	TCP1OV

	PFD Output
TCP2	PFD2

TCP3S1~TCP3S0	TCP3 clock source
00	FS2
01	RC8M
10	TBCK
11	TB1OV

	PWM Output
TCP3	PWM0,1,2,3,4

FSx: Clock scaled frequency comes from OSCH.
TCP1I: External clock input (falling edge).
OSCH: Bulit-in high frequency RC oscillator/2.
RC8M: Bulit-in high frequency RC oscillator.
TBCK: Peripheral clock source, 32KHz in the RC mode.
TB1OV: Time base 1st overflow output.
TCP1OV: TCP1 overflow output.
PFD1: TCP1 cycle time/2 output signal.
PFD2: TCP2 cycle time/2 output signal.
PWM0~4: TCP3 cycle time with PWMxD duty output signal.

P-6: 16-bit Timer/Counter (TCP1 and TCP2 cascade)

Two sets TCP can be cascaded to form a 16-bit timer/counter when TCP2 chooses TCP1OV as clock source (TCP2S1=1 and TCP2S0=1). In the 16-bit timer application, user should use TCP1EN to control the starting or stopping counting of 16-bit timer/counter, data load is controlled by writing TCP1EN=1. The rising TCP2OV will reload the contents in the preload register into timer/counter if TCP2LD=1. The interrupt feature is different, in this case, the TCP1 interrupt will be inhibit when TCP1OV occur, the TCP2 interrupt is normally.

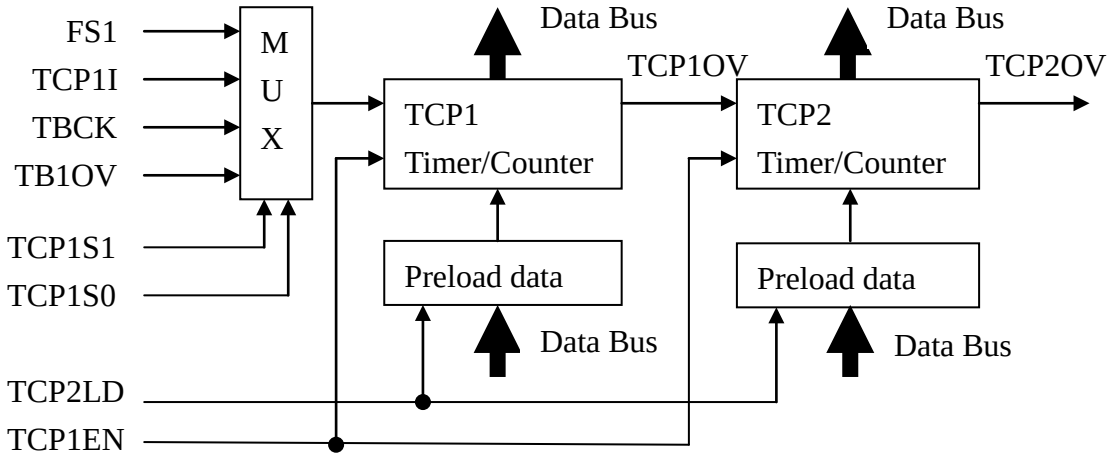


Figure: 16-bit Timer/Counter (TCP1 and TCP2 cascade)

P-7: PWM

The PWM period generated from TCP3. When PWMxEN enable, and PWMOUT pin change to output mode (PA0, PA1, PA2, PA3, PB0, PB1, PD1, PB2, PB3, PC0, PD3 must be output mode), PWMx signal will output to PWMOUT pin. If TCP3 is running, set PWMxEN=1 will not execute until TCP3OV occur.

The duty of PWMx value is store in PWMxL and PWMxM and PWMxH, user write PWMxL first, last write PWMxH. When write the PWMxH, the duty value will be load to PWMxD at the same time. PWM's duty value cannot bigger than TCP3 preload data. If not, PWMOUT is an unexpected signal.

User can select PWMOUT pin start with 1 or start with 0 by PWMSTS register. When TCP3 enable, timer/counter start counting. If timer/counter value equal to PWMx duty's complement value, PWMOUT will change state. The PWMOUT back to start state, When TCP3 is overflow.

User does not use TCP3D=000_H. If not, PWMOUT is an unexpected signal.

PWMSTS0[220H]: PWM start level selector register 0 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM3STS	PWM2STS	PWM1STS	PWM0STS
Read/Write	R/W	R/W	R/W	R/W

PWM0STS: PWM0 Start level selector. (0: Start 0; 1: Start 1)

PWM1STS: PWM1 Start level selector. (0: Start 0; 1: Start 1)

PWM2STS: PWM2 Start level selector. (0: Start 0; 1: Start 1)

PWM3STS: PWM3 Start level selector. (0: Start 0; 1: Start 1)

PWMSTS1[221H]: PWM start level selector register 1 [R/W], default value [---0]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	PWM4STS
Read/Write	-	-	-	R/W

PWM4STS: PWM4 Start level selector. (0: Start 0; 1: Start 1)

PWMPS0[222H]: PWM Port selector register 0 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM3PS	PWM2PS	PWM1PS	PWM0PS
Read/Write	R/W	R/W	R/W	R/W

PWM0PS: PWM0 Port selector. (0: PA0; 1: PB0)

PWM1PS: PWM1 Port selector. (0: PA1; 1: PB1)

PWM2PS: PWM2 Port selector. (0: PA2; 1: PB2)

PWM3PS: PWM3 Port selector. (0: PA3; 1: PB3)

PWMPS1[223H]: PWM Port selector register 1 [R/W], default value [---0]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	PWM4PS
Read/Write	-	-	-	R/W

PWM4PS: PWM4 port selector. (0: PC0; 1: PD3)

PWMC0[224H]: PWM control register 0 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM3EN	PWM2EN	PWM1EN	PWM0EN
Read/Write	R/W	R/W	R/W	R/W

PWM0EN: PWM0 output enabled. (0: disable; 1: enable)

PWM1EN: PWM1 output enabled. (0: disable; 1: enable)

PWM2EN: PWM2 output enabled. (0: disable; 1: enable)

PWM3EN: PWM3 output enabled. (0: disable; 1: enable)

PWMC1[225H]: PWM control register 1 [R/W], default value [---0]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	PWM4EN
Read/Write	-	-	-	R/W

PWM4EN: PWM4 output enabled. (0: disable; 1: enable)

PWM0L[226H]: PWM0 duty low nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM0D3	PWM0D2	PWM0D1	PWM0D0
Read/Write	R/W	R/W	R/W	R/W

PWM0D3~PWM0D0: PWM0 duty low nibble data.

PWM0M[227H]: PWM0 duty middle nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM0D7	PWM0D6	PWM0D5	PWM0D4
Read/Write	R/W	R/W	R/W	R/W

PWM0D7~PWM0D4: PWM0 duty middle nibble data.

PWM0H[228H]: PWM0 duty high nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM0D11	PWM0D10	PWM0D9	PWM0D8
Read/Write	R/W	R/W	R/W	R/W

PWM0D11~PWM0D8: PWM0 duty high nibble data.

PWM1L[229H]: PWM1 duty low nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM1D3	PWM1D2	PWM1D1	PWM1D0
Read/Write	R/W	R/W	R/W	R/W

PWM1D3~PWM1D0: PWM1 duty low nibble data.

PWM1M[22AH]: PWM1 duty middle nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM1D7	PWM1D6	PWM1D5	PWM1D4
Read/Write	R/W	R/W	R/W	R/W

PWM1D7~PWM1D4: PWM1 duty middle nibble data.

PWM1H[22BH]: PWM1 duty high nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM1D11	PWM1D10	PWM1D9	PWM1D8
Read/Write	R/W	R/W	R/W	R/W

PWM1D11~PWM1D8: PWM1 duty high nibble data.

PWM2L[22CH]: PWM2 duty low nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM2D3	PWM2D2	PWM2D1	PWM2D0
Read/Write	R/W	R/W	R/W	R/W

PWM2D3~PWM2D0: PWM2 duty low nibble data.

PWM2M[22DH]: PWM2 duty middle nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM2D7	PWM2D6	PWM2D5	PWM2D4
Read/Write	R/W	R/W	R/W	R/W

PWM2D7~PWM2D4: PWM2 duty middle nibble data.

PWM2H[22EH]: PWM2 duty high nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM2D11	PWM2D10	PWM2D9	PWM2D8
Read/Write	R/W	R/W	R/W	R/W

PWM2D11~PWM2D8: PWM2 duty high nibble data.

PWM3L[22FH]: PWM3 duty low nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM3D3	PWM3D2	PWM3D1	PWM3D0
Read/Write	R/W	R/W	R/W	R/W

PWM3D3~PWM3D0: PWM3 duty low nibble data.

PWM3M[230H]: PWM3 duty middle nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM3D7	PWM3D6	PWM3D5	PWM3D4
Read/Write	R/W	R/W	R/W	R/W

PWM3D7~PWM3D4: PWM3 duty middle nibble data.

PWM3H[231H]: PWM3 duty high nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM3D11	PWM3D10	PWM3D9	PWM3D8
Read/Write	R/W	R/W	R/W	R/W

PWM3D11~PWM3D8: PWM3 duty high nibble data.

PWM4L[232H]: PWM4 duty low nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM4D3	PWM4D2	PWM4D1	PWM4D0
Read/Write	R/W	R/W	R/W	R/W

PWM4D3~PWM4D0: PWM4 duty low nibble data.

PWM4M[233H]: PWM4 duty middle nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM4D7	PWM4D6	PWM4D5	PWM4D4
Read/Write	R/W	R/W	R/W	R/W

PWM4D7~PWM4D4: PWM4 duty middle nibble data.

PWM4H[234H]: PWM4 duty high nibble data register [R/W], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWM4D11	PWM4D10	PWM4D9	PWM4D8
Read/Write	R/W	R/W	R/W	R/W

PWM4D11~PWM4D8: PWM4 duty high nibble data.

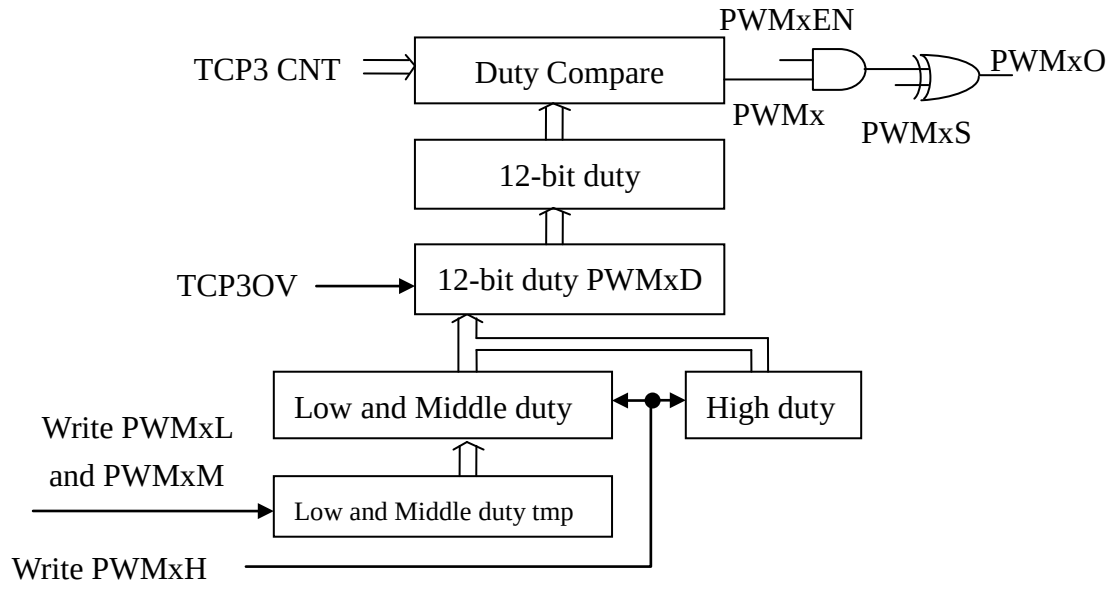


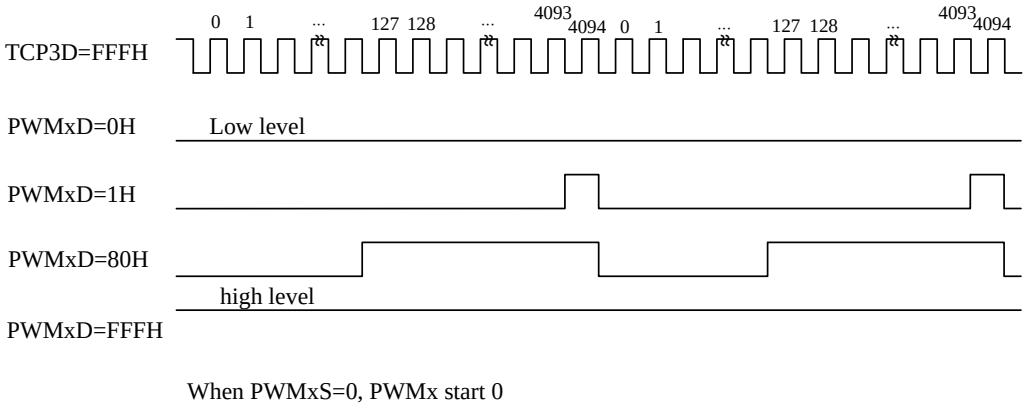
Figure: PWM (TCP3)

PWMxD	PWMx duty	Note
0	(0 * clock cycle) / TCP3 timer's period	All off
1	(1 * clock cycle) / TCP3 timer's period	-
2	(2 * clock cycle) / TCP3 timer's period	-
……	……	-
n	((n) * clock cycle) / TCP3 timer's period	-
……	……	-
TCP3D	((TCP3D) * clock cycle) / TCP3 timer's period	All on

Note:

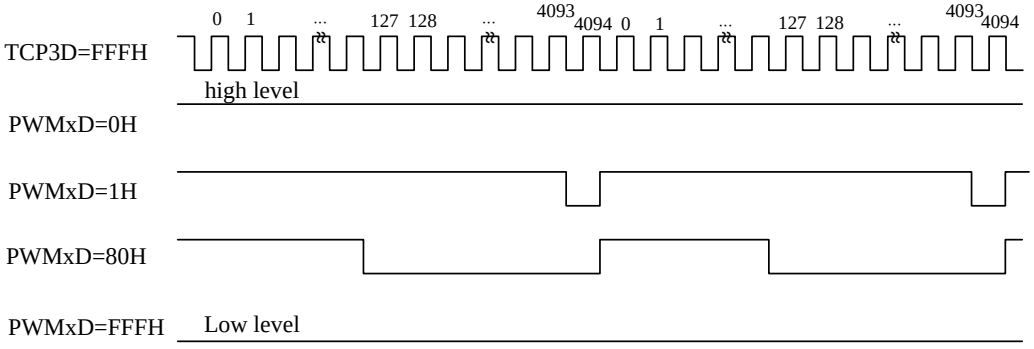
1. PWMxD cannot bigger than TCP3D.
2. TCP3 timer's period = (TCP3D) * clock cycle.
3. PWM0~3 can start 0 or start 1 by PWMSTS0 register.
4. PWM4 can start 0 or start 1 by PWMSTS1 register.

Table: PWMx duty



When PWMxS=0, PWMx start 0

Figure: PWMx output start 0 when PWMxSTS=0



When PWMxS=1, PWMx start 1

Figure: PWMx output start 1 when PWMxSTS=1

P-8: IIC Module

IIC is a 2-wire, bi-directional serial bus, which provides a simple, efficient way for data exchange between devices. This two-wire bus minimizes the interconnection between devices and eliminates the need for address decoders. IIC provides up to 8 sets of data receiving registers and 2 sets of data transfer registers to ensure that the IIC can perform data transfer at full speed.

P-8-1 IIC Control

Every IIC device must have independent slave address. User can use IICCON<3:1> (ADR<2:0>) to select one independent slave address, the map address reference follow table.

Slave Device Addressing

Device Identifier				Device Address			R/W bit
B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	ADR2	ADR1	ADR0	R/W

ADR2	ADR1	ADR0	IIC device address 7-bit	With R/W Bit and R/W=0
0	0	0	101 0000 (50H)	1010 0000 (A0H)
0	0	1	101 0001 (51H)	1010 0010 (A2H)
0	1	0	101 0010 (52H)	1010 0100 (A4H)
0	1	1	101 0011 (53H)	1010 0110 (A6H)
1	0	0	101 0100 (54H)	1010 1000 (A8H)
1	0	1	101 0101 (55H)	1010 1010 (AAH)
1	1	0	101 0110 (56H)	1010 1100 (ACH)
1	1	1	101 0111 (57H)	1010 1110 (AEH)

Table: IIC address mapping table

IICINTC[01EH]: Extended interrupt control register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TXIE	SPIE	STIE	IICIE
Read/Write	R/W	R/W	R/W	R/W

IICIE : enable IIC interrupt. (0 : disable ; 1 : enable)

STIE : enable IIC start signal interrupt. (0 : disable ; 1 : enable)

SPIE : enable IIC stop signal interrupt. (0 : disable ; 1 : enable)

TXIE : enable IIC data transmission interrupt. (0 : disable ; 1 : enable)

IICINTF[01FH]: Extended interrupt request flag register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TXF	SPF	STF	IICF
Read/Write	R/W	R/W	R/W	R/W

IICF: IIC interrupt request flag. (0: inactive; 1: active)

STF : IIC start signal interrupt request flag. (0 : inactive ; 1 : active)

SPF: IIC stop signal interrupt request flag. (0: inactive; 1: active)

(Signal generation requires address matching)

TXF : IIC data transmission interrupt request flag. (0 : inactive ; 1 : active)

IICCON[261H]: IIC control register 1 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	ADR2	ADR1	ADR0	IICEN
Read/Write	R/W	R/W	R/W	R/W

IICEN: IIC function enable. (0: disable; 1: enable)

ADR2~ADR0: IIC slave address.

IICSTS[262H]: IIC status register [R/W], default value [0001]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	MAASF	MBB	SRWB	TXACK
Read/Write	R/W	R	R	R

TXACK: receive master acknowledge. (0: master don’t send acknowledge; 1: master send acknowledge)

SRWB: IIC slave read or write select. (0: write data to slave; 1: read data from slave)

(Clear by start signal)

MBB: IIC bus busy flag. (0: IIC bus idle; 1: IIC bus busy)

(Clear by stop signal)

MAASF: IIC slave address match flag. (0: not match; 1: match)

(Clear by software or start signal)

IICDATL[263H]: IIC data transmission low nibble register [R], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	DAT3	DAT2	DAT1	DAT0
Read/Write	R	R	R	R

DAT3~DAT0: IIC data transmission low nibble data.

IICDATH[264H]: IIC data transmission high nibble register [R], default value [xxxx]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	DAT7	DAT6	DAT5	DAT4
Read/Write	R	R	R	R

DAT7~DAT4: IIC data transmission high nibble data.

IICRDATL0[265H]: IIC read data low nibble register 0 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	RDAT03	RDAT02	RDAT01	RDAT00
Read/Write	R/W	R/W	R/W	R/W

RDAT03~RDAT00: IIC read low nibble data 0.

IICRDATH0[266H]: IIC read data high nibble register 0 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	RDAT07	RDAT06	RDAT05	RDAT04
Read/Write	R/W	R/W	R/W	R/W

RDAT07~RDAT04: IIC read high nibble data 0.

IICRDATL1[267H]: IIC read data low nibble register 1 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	RDAT13	RDAT12	RDAT11	RDAT10
Read/Write	R/W	R/W	R/W	R/W

RDAT13~RDAT10: IIC read low nibble data 1.

IICRDATH1[268H]: IIC read data high nibble register 1 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	RDAT17	RDAT16	RDAT15	RDAT14
Read/Write	R/W	R/W	R/W	R/W

RDAT17~RDAT14: IIC read high nibble data 1.

IICDACNT[269H]: IIC data RX counter register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	IICDACT3	IICDACT2	IICDACT1	IICDACT0
Read/Write	R	R	R	R

IICDACT3~ IICDACT0 IIC data RX counter register.

IICWDATL0[26AH]: IIC write data low nibble register 0 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT03	WDAT02	WDAT01	WDAT00
Read/Write	R/W	R/W	R/W	R/W

WDAT03~WDAT00: IIC write low nibble data 0.

IICWDATH0[26BH]: IIC write data high nibble register 0 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT07	WDAT06	WDAT05	WDAT04
Read/Write	R/W	R/W	R/W	R/W

WDAT07~WDAT04: IIC write high nibble data 0.

IICWDATL1[26CH]: IIC write data low nibble register 1 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT13	WDAT12	WDAT11	WDAT10
Read/Write	R/W	R/W	R/W	R/W

WDAT13~WDAT10: IIC write low nibble data 1.

IICWDATH1[26DH]: IIC write data high nibble register 1 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT17	WDAT16	WDAT15	WDAT14
Read/Write	R/W	R/W	R/W	R/W

WDAT17~WDAT14: IIC write high nibble data 1.

IICWDATL2[26EH]: IIC write data low nibble register 2 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT23	WDAT22	WDAT21	WDAT20
Read/Write	R/W	R/W	R/W	R/W

WDAT23~WDAT20: IIC write low nibble data 2.

IICWDATH2[26FH]: IIC write data high nibble register 2 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT27	WDAT26	WDAT25	WDAT24
Read/Write	R/W	R/W	R/W	R/W

WDAT27~WDAT24: IIC write high nibble data 2.

IICWDATL3[270H]: IIC write data low nibble register 3 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT33	WDAT32	WDAT31	WDAT30
Read/Write	R/W	R/W	R/W	R/W

WDAT33~WDAT30: IIC write low nibble data 3.

IICWDATH3[271H]: IIC write data high nibble register 3 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT37	WDAT36	WDAT35	WDAT34
Read/Write	R/W	R/W	R/W	R/W

WDAT37~WDAT34: IIC write high nibble data 3.

IICWDATL4[272H]: IIC write data low nibble register 4 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT43	WDAT42	WDAT41	WDAT40
Read/Write	R/W	R/W	R/W	R/W

WDAT43~WDAT40: IIC write low nibble data 4.

IICWDATH4[273H]: IIC write data high nibble register 4 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT47	WDAT46	WDAT45	WDAT44
Read/Write	R/W	R/W	R/W	R/W

WDAT47~WDAT44: IIC write high nibble data 4.

IICWDATL5[274H]: IIC write data low nibble register5 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT53	WDAT52	WDAT51	WDAT50
Read/Write	R/W	R/W	R/W	R/W

WDAT53~WDAT50: IIC write low nibble data 5.

IICWDATH5[275H]: IIC write data high nibble register 5 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT57	WDAT56	WDAT55	WDAT54
Read/Write	R/W	R/W	R/W	R/W

WDAT57~WDAT54: IIC write high nibble data 5.

IICWDATL6[276H]: IIC write data low nibble register 6 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT63	WDAT62	WDAT61	WDAT60
Read/Write	R/W	R/W	R/W	R/W

WDAT63~WDAT60: IIC write low nibble data 6.

IICWDATH6[277H]: IIC write data high nibble register 6 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT67	WDAT66	WDAT65	WDAT64
Read/Write	R/W	R/W	R/W	R/W

WDAT67~WDAT64: IIC write high nibble data 6.

IICWDATL7[278H]: IIC write data low nibble register 7 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT73	WDAT72	WDAT71	WDAT70
Read/Write	R/W	R/W	R/W	R/W

WDAT73~WDAT70: IIC write low nibble data 7.

IICWDATH7[279H]: IIC write data high nibble register 7 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	WDAT77	WDAT76	WDAT75	WDAT74
Read/Write	R/W	R/W	R/W	R/W

WDAT77~WDAT74: IIC write high nibble data 7.

Set IICCON<0> (IICEN) can enable all IIC block. The first byte of data transfer immediately following the START signal is the slave address transmitted by the master. This is a seven bit long calling address followed by an R/W bit.

When START signal is detected, IICSTS<2> (MBB) is set and IICINTF<1> (STF) is also set and IICDACNT will be clear. An interrupt is generated if the IICINTC<1> (STIE) be set. Users can clear counters or update data for multiple Byte transmissions.

When STOP signal is detected, MBB is cleared and IICINTF<2> (SPF) is also set. An interrupt is generated if the IICINTC<2> (SPIE) be set.

IICSTS<3> (MAASF) is set when IIC device match the calling address. When MAASF is set, and IICINTF<0> (IICF) is also set.

An interrupt is generated if the IICINTC<0> (IICIE) be set. User can check IICSTS<1> (SRWB) to know IIC device operate in transmit or receive mode. When IICF is set, an interrupt is generated to the CPU.

IICF is set when one of the following events occurs:

- IIC device address match.
- Completion of one byte of data transfer. It is set at the falling edge of the 9th clock.

When IIC device operate in transmit mode, master's acknowledge store in IICSTS<0> (TXACK). If detect acknowledge, this bit set, if not, this bit clear.

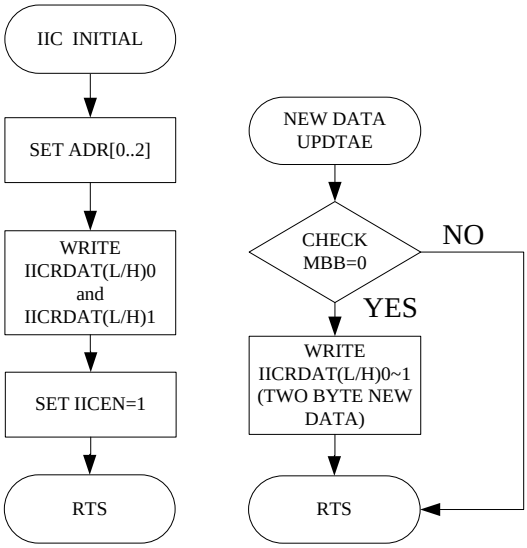
IICDAT(L/H) is read only register. In transmit mode, data written into the register to send to the bus automatically, with the most significant bit out first. In receive mode, the complete data will be automatically written into the receiving register according to the indicators of IICDACNT, and the IICDACNT index will be added to 1.

Whenever IICRDAT(L/H)0 transfer is complete, IICRDAT(L/H)1 will automatically load transfer buffer, and generates an interrupt flag (TXF) notify updatable, an interrupt is generated if the IICINTC<3> (TXIE) be set. If the data transfer will be more than two bytes, you can create a data counter, interrupt flag is generated every time, data will be placed in IICRDAT(L/H)0 and IICRDAT(L/H)1 by order by software, however, if the master halfway want to re-read the beginning of the data, when the data counter is not starting from scratch, data can not be read correctly, this situation can be set STIE be 1, when receiving the START signal from IIC BUS, an interrupt is generated, by receiving this start signal, the data counter is reset by the software, so you can re-read the data correctly.

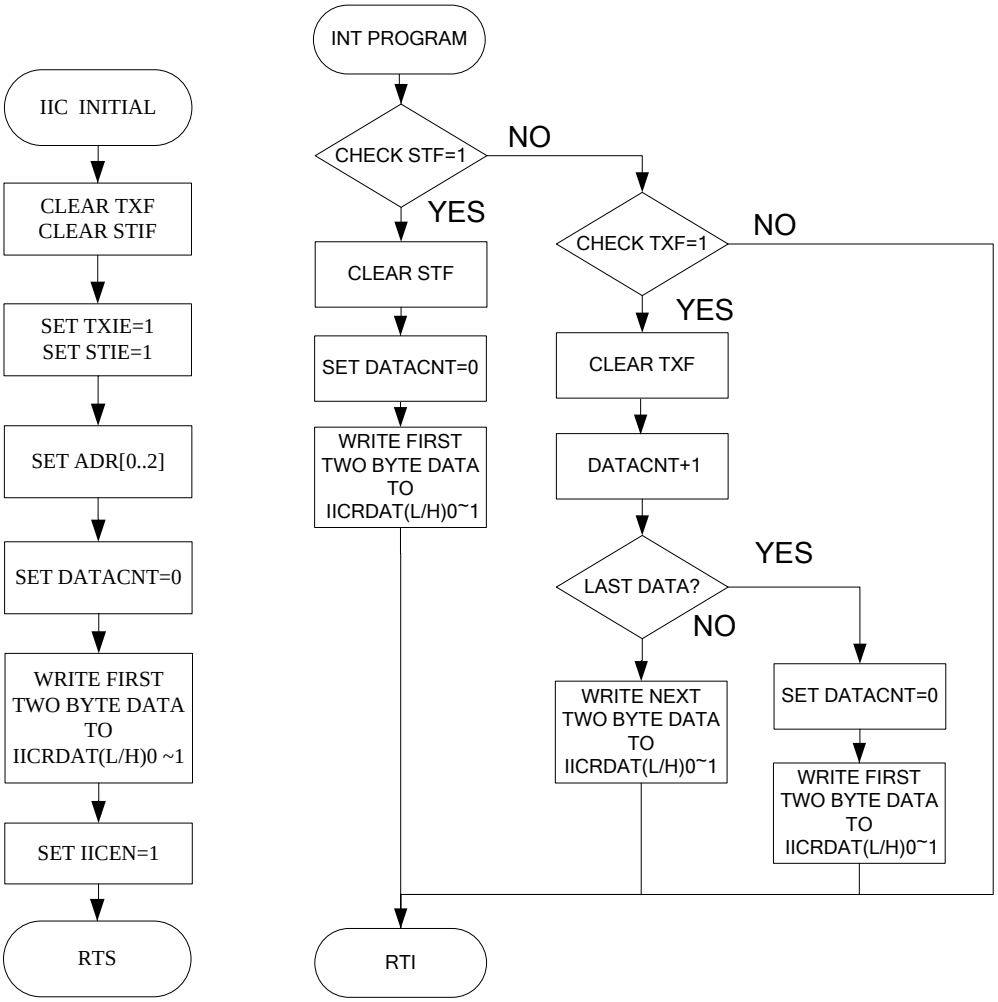
P-8-2 IIC Receive Buffer Register

Provides 8 sets of IICWDATL / H 0~7 data buffer registers. When IIC receives the write command, IICDACNT will return to 0. After receiving 1 byte of data, it will be automatically stored in the designated register according to the IICDACNT content, and the IICDACNT content will be Increase by 1. If you receive more than 8 consecutive data, it will overwrite the first data.

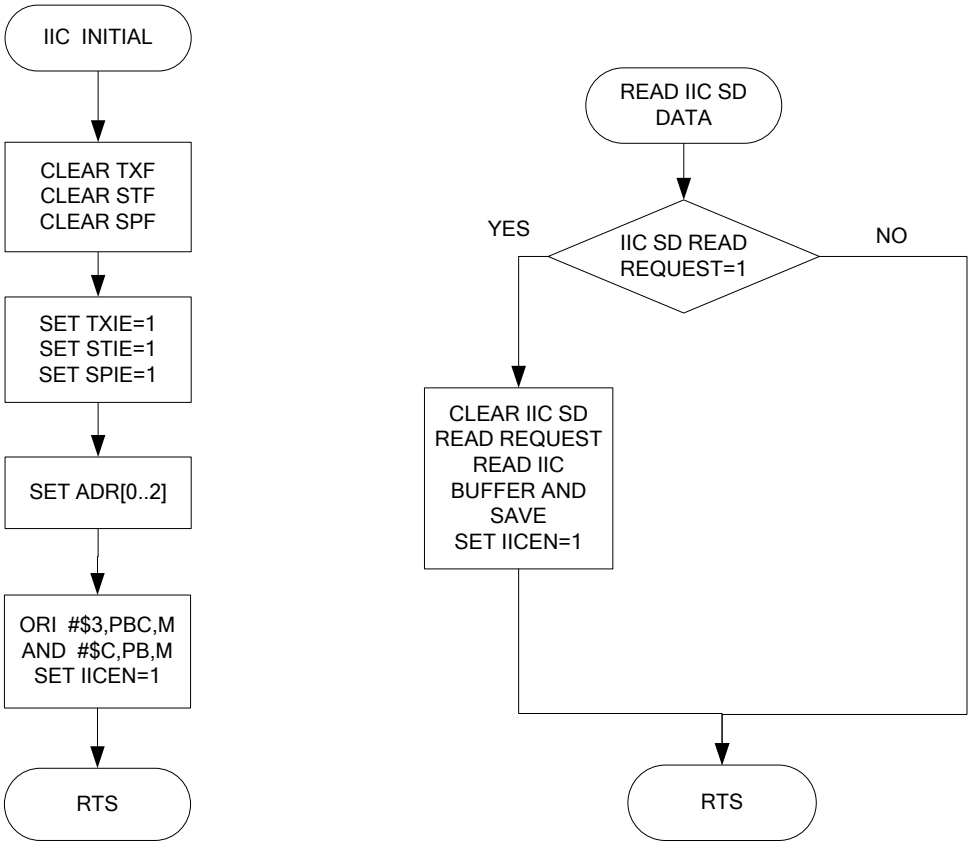
Send 1 or 2 Byte data



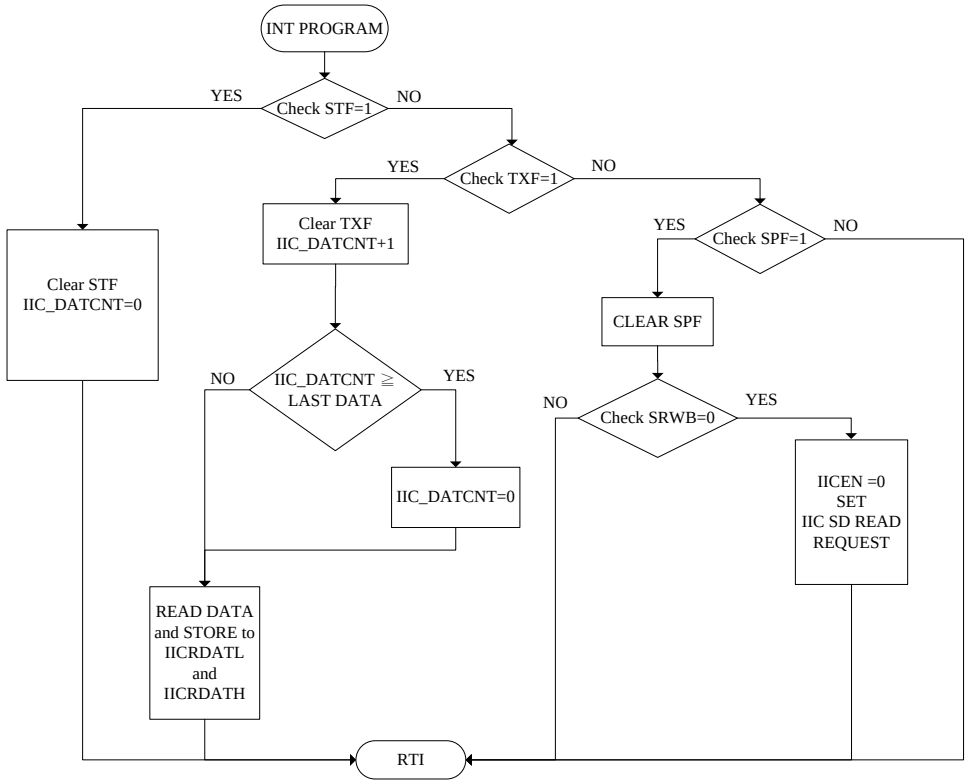
Send more than 2 Byte data



Read / Write



For IIC read and write command for new



P-9: Analog to Digital Converter (ADC)

The TTR051 has a 12-bit 8-channel high-precision successive approximation ADC built in. This ADC is multiplexed with other functions of the IO port.

The basic functions of this ADC are:

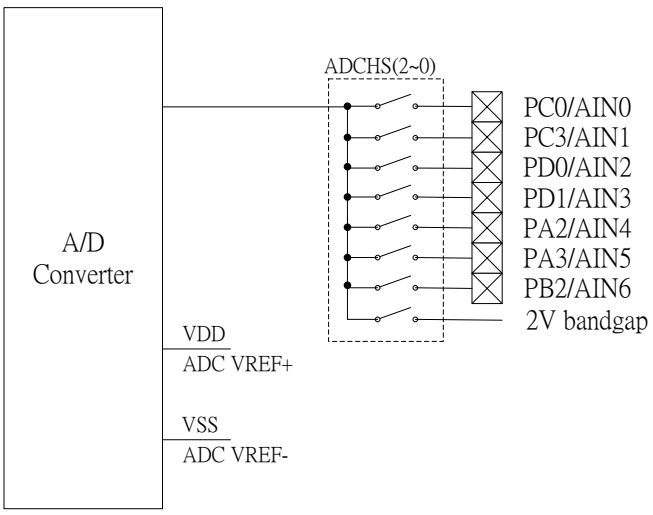
12-bit resolution; more than 10 digits accuracy; Internal one channel AIN7 can be connected to internal 2V voltage to measure VDD voltage; external 7 channels AIN0~6 are used for external signal measurement.

The A/D converter can be triggered by write to ADL or ADM or ADH register to start and ADF bit will be set ’0’. When conversion is complete, the ADF bit returns to ’1’, ADL/ADM/ADH will store the latest data and the ADCF bit in the INTF1 register is set, and an A/D interrupt will occur, if enabled.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode, if the A/D converter is triggered by write to ADH register, it means TTR051 will enter SLEEP until compelety of A/D module. By the way , please confirm that the AD CLK signal source is suitable for this unique function.

After conversion compelety of A/D module , ADL/ADM/ADH will store the latest data , and ADCF will be setting , if A/D interrupt is enabled , A/D interrupt will occur, but if A/D interrupt is disabled , A/D interrupt will not occur and A/D module is still be turn on , so A/D module will have extra dc consumption , it means that if we care about dc consumption , user must remember to turn off A/D module by set ‘0’ to ADEN bit in ADCTL register.

ADC Structure as follow:



ADL[290H]: A/D result data low nibble register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	AD3	AD2	AD1	AD0
Read/Write	R	R	R	R

AD3~AD0: A/D result low nibble data .

ADM[291H]: A/D result data middle nibble register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	AD7	AD6	AD5	AD4
Read/Write	R	R	R	R

AD7~AD4: A/D result middle nibble data .

ADH[292H]: A/D result data high nibble register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	AD11	AD10	AD9	AD8
Read/Write	R	R	R	R

AD7~AD4: A/D result high nibble data .

ADCHS[293H]: A/D channel selector register 0 [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	---	CH2	CH1	CH0
Read/Write	R/W	R/W	R/W	R/W

CH2~CH0: A/D channel selector .

000 : select analog input channel 0 (AIN0)
001 : select analog input channel 0 (AIN1)
010 : select analog input channel 0 (AIN2)
011 : select analog input channel 0 (AIN3)
100 : select analog input channel 0 (AIN4)
101 : select analog input channel 0 (AIN5)
110 : select analog input channel 0 (AIN6)
111 : select analog input channel 0 (AIN7), internal 2V voltage

Bit3: Reserved, please keep it as 0 and do not change

ADCTL[294H]: A/D control register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	ADEN	ADCK2	ADCK1	ADCK0
Read/Write	R/W	R/W	R/W	R/W

ADCK2~ADCK0 A/D Conversion clock selector

000 : 1MHz

001 : 250KHz

010 : 125KHz

011 : (32KHz)

100 : 2MHz

101 : 1MHz

110 : 500KHz

111 : (32KHz)

(32KHz) : When the MCU is executed at high speed, it is OSCH/128, and when the MCU is switched to low speed, it is OSCL

ADEN : A/D Enable control bit

0 : A/D converter is shutoff and consumes no operating current

1 : A/D converter module is operating

ADCSTAT[296H]: A/D conversion status register [R], default value [---1]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	ADF
Read/Write	-	-	-	R

ADF Conversion status flag.

0 : A/D conversion operation.

1 : Idle.

ADSEL0[297H]: A/D /IO selector register 0 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PD1/AIN3	PD0/AIN2	PC3/AIN1	PC0/AIN0
Read/Write	R/W	R/W	R/W	R/W

AIN3~0 : A/D / IO set bit .

0 : Set to IO port.

1 : Set to the A/D.

ADSEL1[298H]: A/D /IO selector register 1 [R/W], default value [-000]

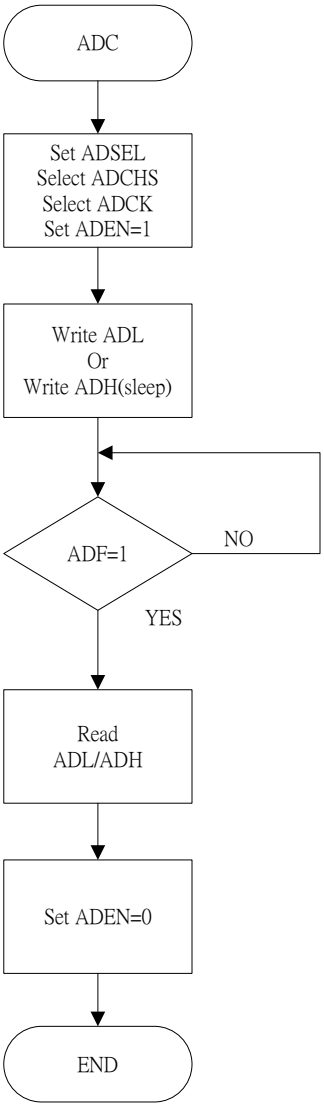
Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	PB2/AIN6	PA3/AIN5	PA2/AIN4
Read/Write	-	R/W	R/W	R/W

AIN6~4 : A/D / IO set bit .

0 : Set to IO port.

1 : Set to the A/D.

ADC Flowchart as follow:



P-9: IO Pad Cell Structure and Function Description

- IO port with touch pad input

The input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control register=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. Software can performs a configuration (output data register=0, changing the IO control register to 0) for open drain type that specifies suitable for key scan application. An additional feature supports the touch pad input.

Extern input	IO control data	Output data	Pull-up R	Wake-up feature
Disable	0	X	No	No
Disable	1	0	No	No
Disable	1	1	Enable	Enable
Enable and touch pad scan	X	X	No	No

X: don’t care the value.

IO control data	IO pad
0	Output register data
1	IO pad input data

Read PxI	Read input data
1	IO pad data

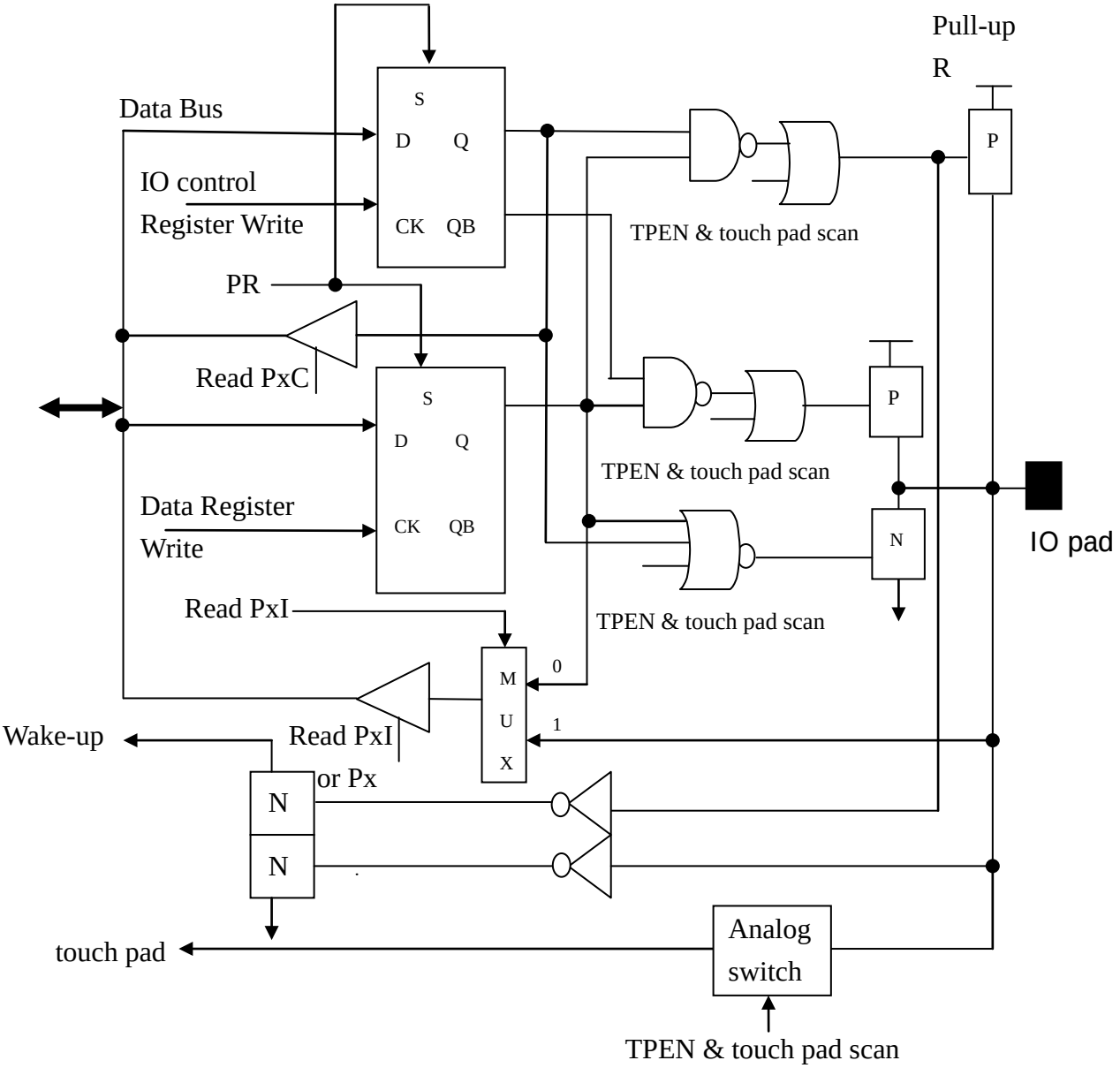


Figure IO-A: Standard IO port with touch pad input

- IO port with touch pad input and ADC input and PWM output

The input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control register=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. Software can performs a configuration (output data register=0, changing the IO control register to 0) for open drain type that specifies suitable for key scan application. An additional feature supports the touch pad input.

Extern input	IO control data	Output data	Pull-up R	Wake-up feature
Disable	0	X	No	No
Disable	1	0	No	No
Disable	1	1	Enable	Enable
Enable and touch pad scan	X	X	No	No
Enable ADC and run	X	X	No	No

X: don’t care the value.

IO control data	Internal output	IO pad
0	Enable	Output internal data
0	Disable	Output register data
1	X	IO pad input data

X: don’t care the value

Read PxI	Read input data
1	IO pad data

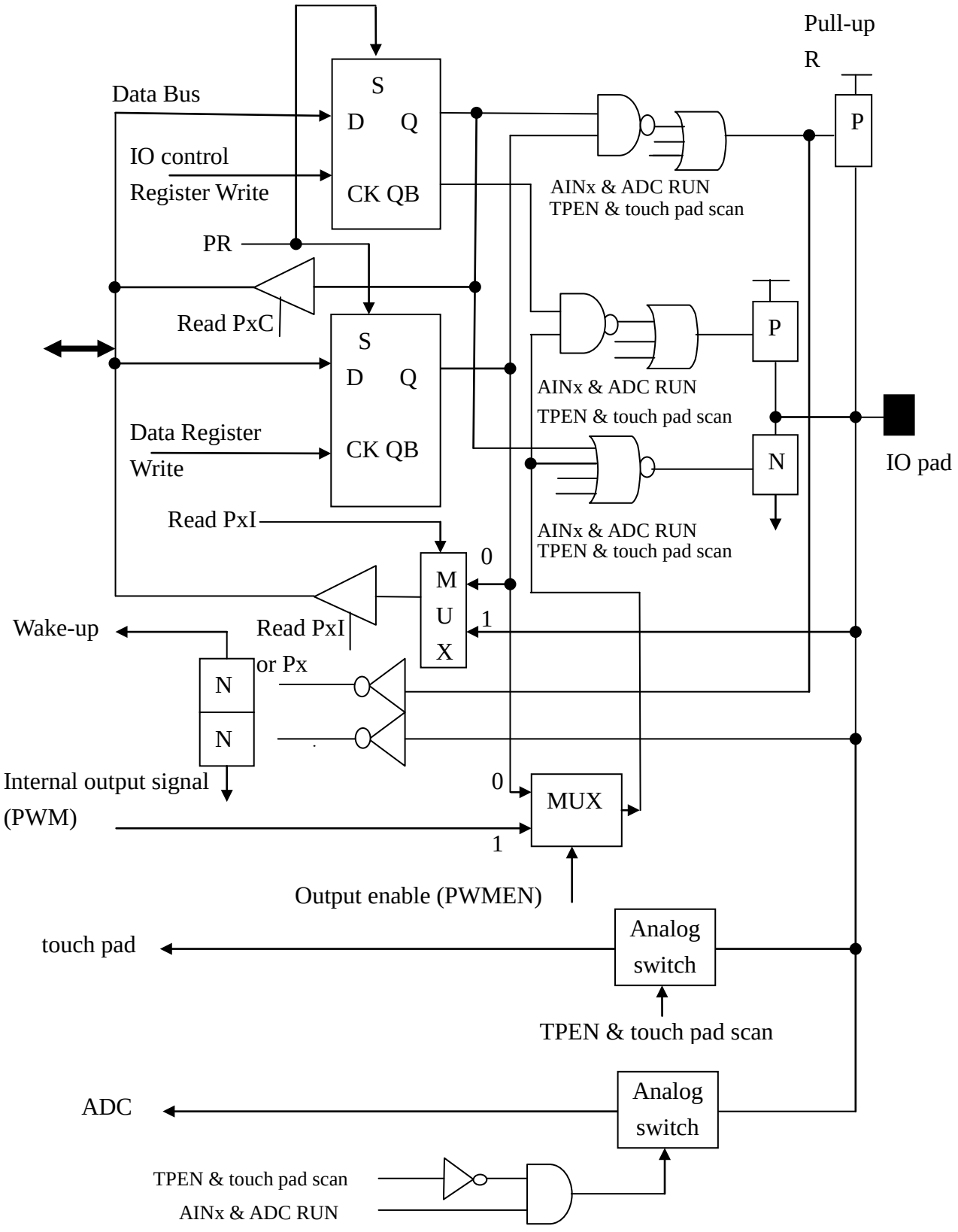


Figure IO-B: Standard IO port with touch pad input and ADC input and PWM output

- IO port with external interrupt trigger input with bandgap and PWM output

The standard input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control data=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. If enable internal output, the IO port must set as output (IO control data=0). An additional feature supports the internal PWM output and external interrupt trigger input.

IO control data	Output data	Pull-up R	Wake-up feature	External input
0	X	No	No	No
1	0	No	No	Enable
1	1	Enable	Enable	Enable

X: don’t care the value

IO control data	external interrupt trigger input	IO pad
0	Disable	Output internal data
0	Disable	Output register data
1	enable	IO pad input data

Read PxI	Read input data
1	IO pad data

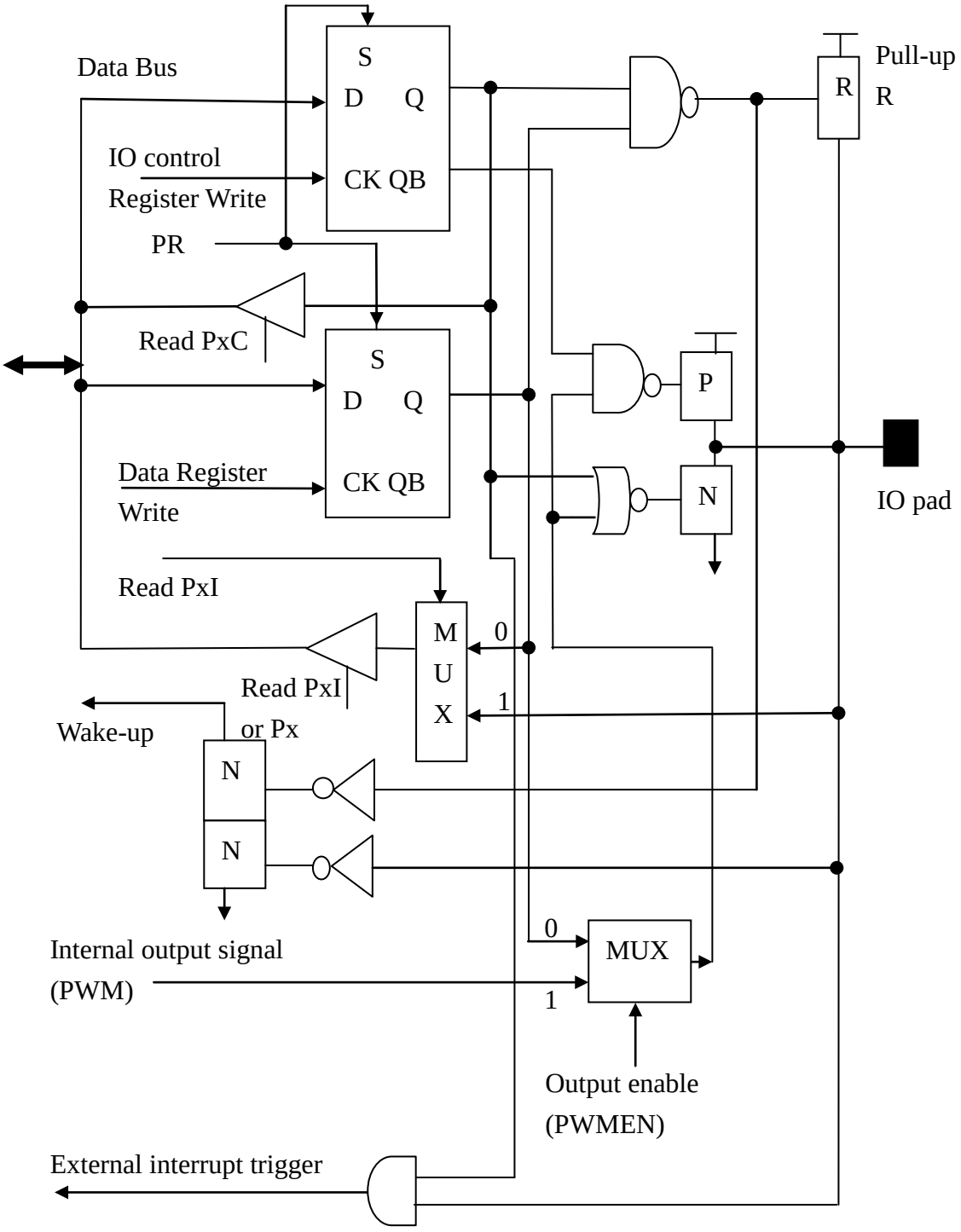


Figure IO-C Standard IO port with external interrupt trigger input and PWM output

- IO port with touch pad input and external interrupt trigger input with bandgap and PWM output

The input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control register=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. Software can performs a configuration (output data register=0, changing the IO control register to 0) for open drain type that specifies suitable for key scan application. An additional feature supports the touch pad input.

Extern input	IO control data	Output data	Pull-up R	Wake-up feature
Disable	0	X	No	No
Disable	1	0	No	No
Disable	1	1	Enable	Enable
Enable and touch pad scan	X	X	No	No

X: don’t care the value.

IO control data	Internal output	IO pad
0	Enable	Output internal data
0	Disable	Output register data
1	X	IO pad input data

X: don’t care the value

Read PxI	Read input data
1	IO pad data

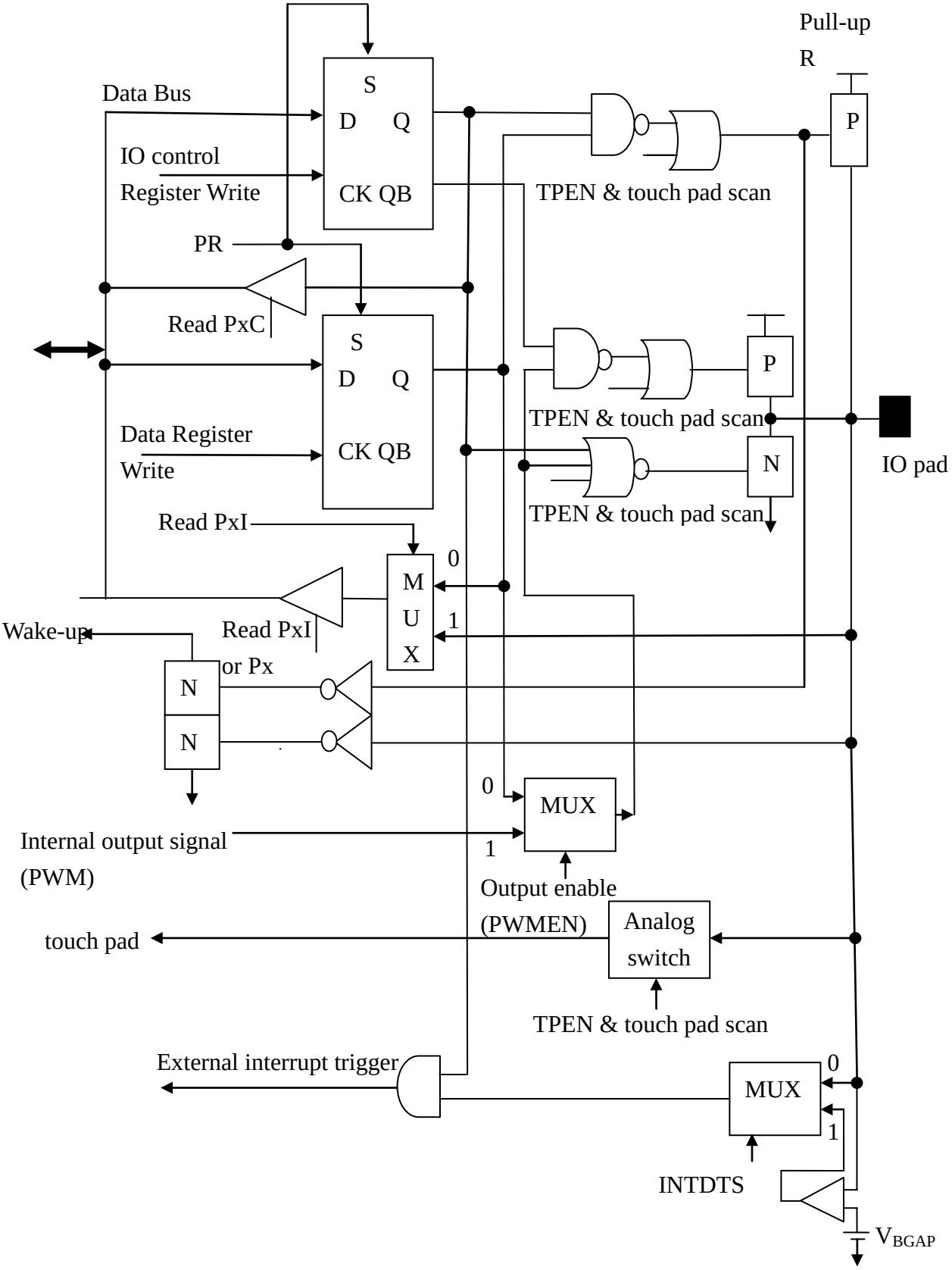


Figure IO-D: Standard IO port with touch pad input and external interrupt trigger input with bandgap and internal PWM output

- IO port with internal PWM output and IIC

The standard input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control data=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. If enable internal output, the IO port must set as output (IO control data=0). An additional feature supports the internal PWM output and external interrupt trigger input and IIC.

IO control data	Output data	Pull-up R	Wake-up feature
0	X	No	No
1	0	No	No
1	1	Enable	Enable

X: don’t care the value

IO control data	Internal output	IO pad
0	Enable	Output internal data
0	Disable	Output register data
1	X	IO pad input data

X: don’t care the value

Read PxI	Read input data
1	IO pad data

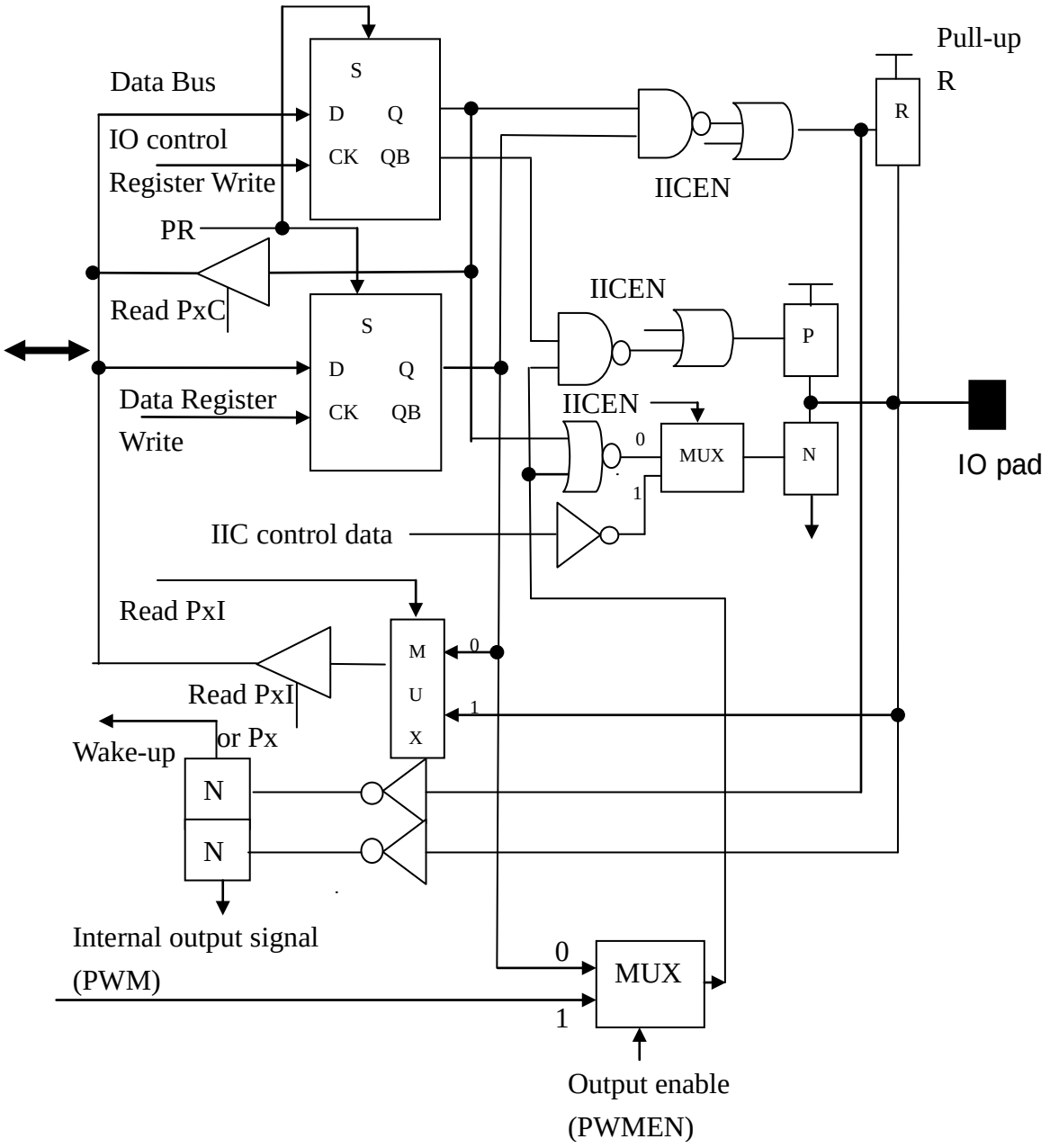


Figure IO-E: Standard IO port with internal PWM output and IIC-BUS(SDA)

- IO port with internal PWM output and external interrupt trigger input and IIC

The standard input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control data=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. If enable internal output, the IO port must set as output (IO control data=0). An additional feature supports the internal PWM output and external interrupt trigger input and IIC.

IO control data	Output data	Pull-up R	Wake-up feature	External input
0	X	No	No	No
1	0	No	No	Enable
1	1	Enable	Enable	Enable

X: don’t care the value

IO control data	Internal output	IO pad
0	Enable	Output internal data
0	Disable	Output register data
1	X	IO pad input data

X: don’t care the value

Read PxI	Read input data
1	IO pad data

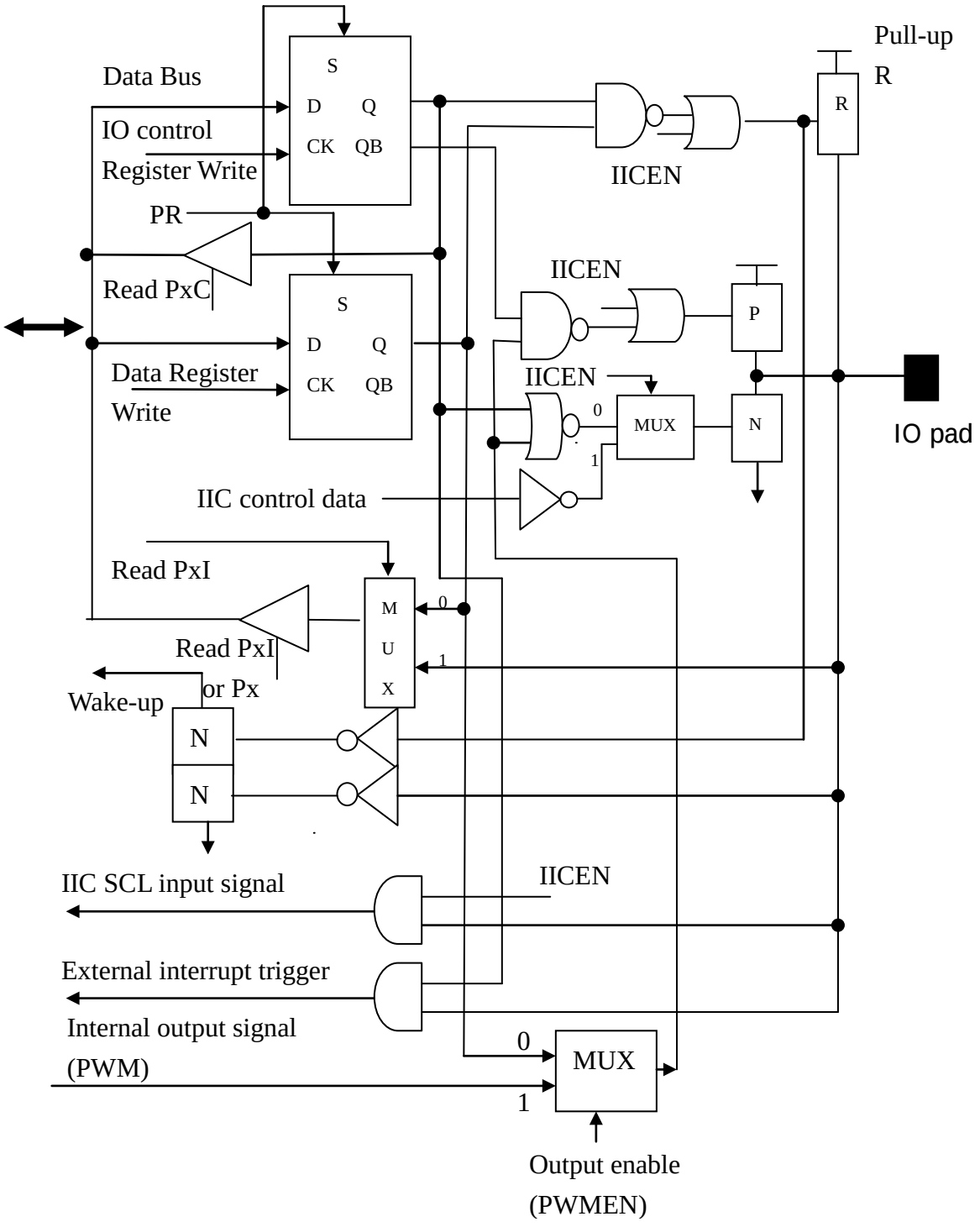


Figure IO-F: Standard IO port with internal PWM output and external interrupt trigger input and IIC-BUS(SCL)

- IO port with internal PWM output and external TCP1 clock input

The standard input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control data=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. If enable internal output, the IO port must set as output (IO control data=0). An additional feature supports the internal PWM output and external TCP1 clock input.

IO control data	Output data	Pull-up R	Wake-up feature	External input
0	X	No	No	No
1	0	No	No	Enable
1	1	Enable	Enable	Enable

X: don’t care the value

IO control data	Internal output	IO pad
0	Enable	Output internal data
0	Disable	Output register data
1	X	IO pad input data

X: don’t care the value

Read PxI	Read input data
1	IO pad data

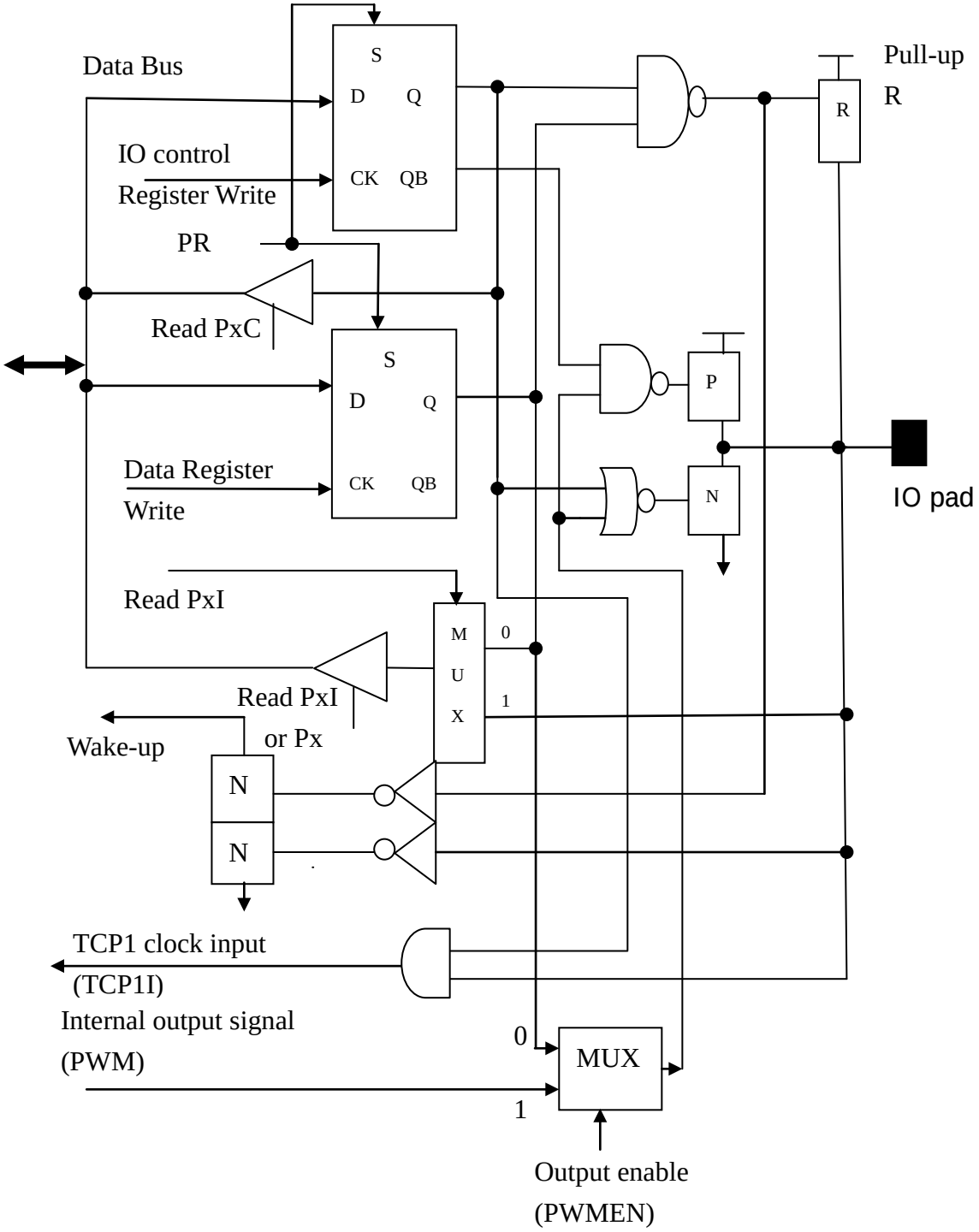


Figure IO-G: Standard IO port with internal PWM output and external TCP1 clock input

- IO port with touch pad input and PFD output

The input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control register=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. Software can performs a configuration (output data register=0, changing the IO control register to 0) for open drain type that specifies suitable for key scan application. An additional feature supports the touch pad input.

Extern input	IO control data	Output data	Pull-up R	Wake-up feature
Disable	0	X	No	No
Disable	1	0	No	No
Disable	1	1	Enable	Enable
Enable and touch pad scan	X	X	No	No

X: don’t care the value.

IO control data	Internal output	IO pad
0	Enable	Output internal data
0	Disable	Output register data
1	X	IO pad input data

X: don’t care the value

Read PxI	Read input data
1	IO pad data

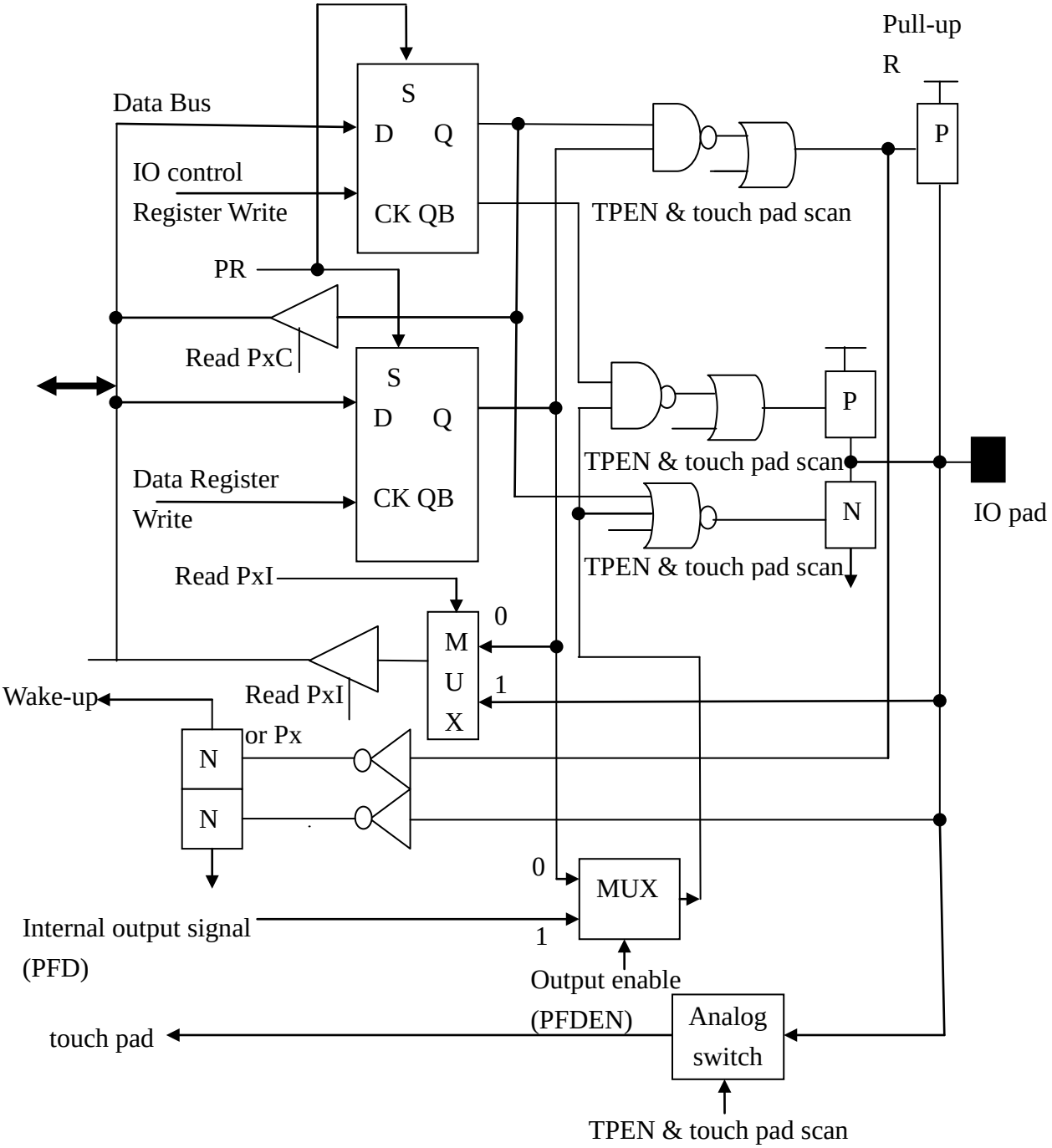


Figure IO-H: Standard IO port with internal touch pad and PFD output

- IO port with touch pad input and ADC input

The input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control register=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. Software can performs a configuration (output data register=0, changing the IO control register to 0) for open drain type that specifies suitable for key scan application. An additional feature supports the touch pad input.

Extern input	IO control data	Output data	Pull-up R	Wake-up feature
Disable	0	X	No	No
Disable	1	0	No	No
Disable	1	1	Enable	Enable
Enable and touch pad scan	X	X	No	No
Enable ADC and run	X	X	No	No

X: don’t care the value.

IO control data	IO pad
0	Output register data
1	IO pad input data

Read PxI	Read input data
1	IO pad data

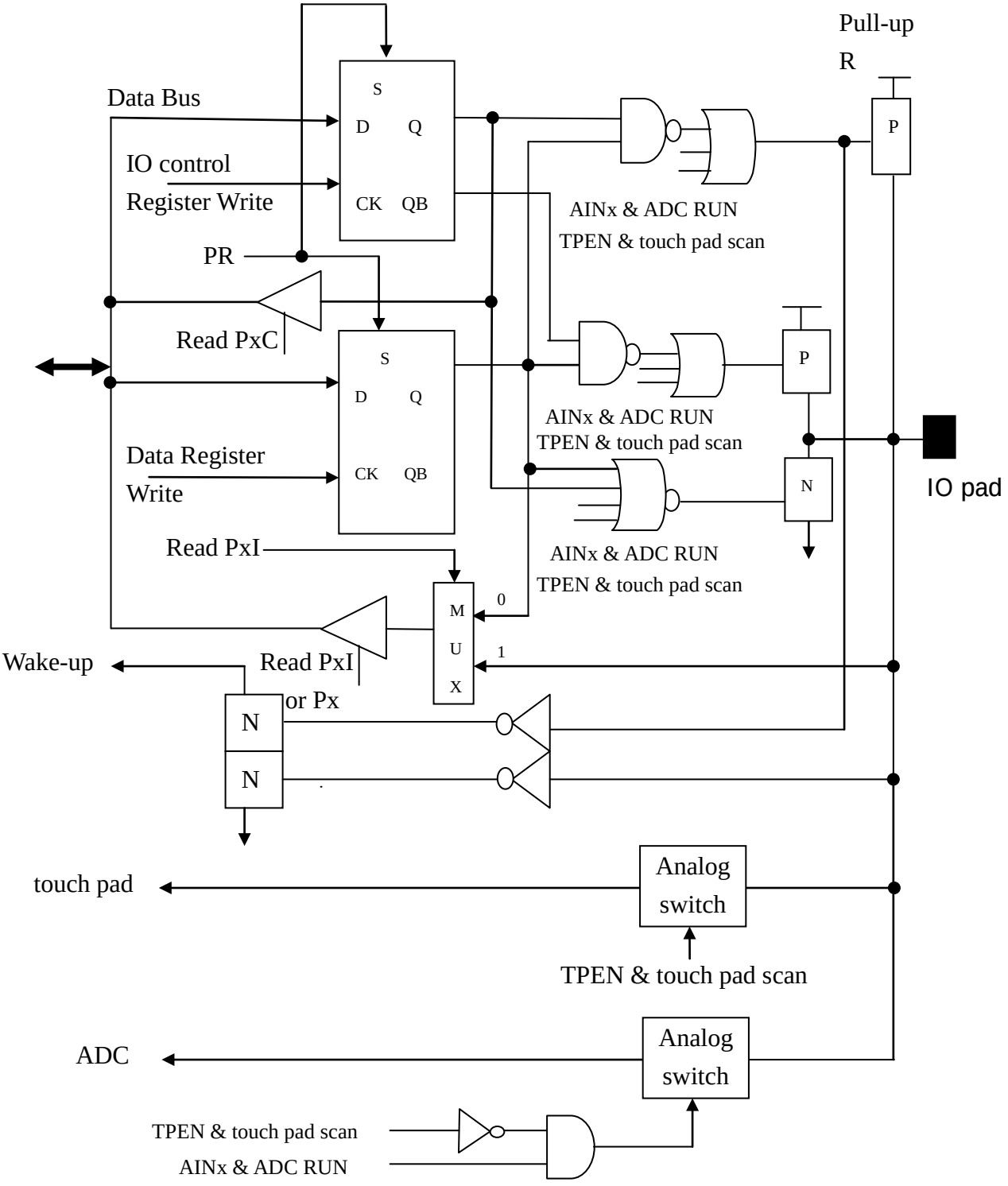


Figure IO-I: Standard IO port with touch pad input and ADC input

- IO port with touch pad input and external interrupt trigger input with bandgap and PWM output

The input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control register=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. Software can performs a configuration (output data register=0, changing the IO control register to 0) for open drain type that specifies suitable for key scan application. An additional feature supports the touch pad input.

Extern input	IO control data	Output data	Pull-up R	Wake-up feature
Disable	0	X	No	No
Disable	1	0	No	No
Disable	1	1	Enable	Enable
Enable and touch pad scan	X	X	No	No
Enable ADC and run	X	X	No	No

X: don’t care the value.

IO control data	Internal output	IO pad
0	Enable	Output internal data
0	Disable	Output register data
1	X	IO pad input data

X: don’t care the value

Read PxI	Read input data
1	IO pad data

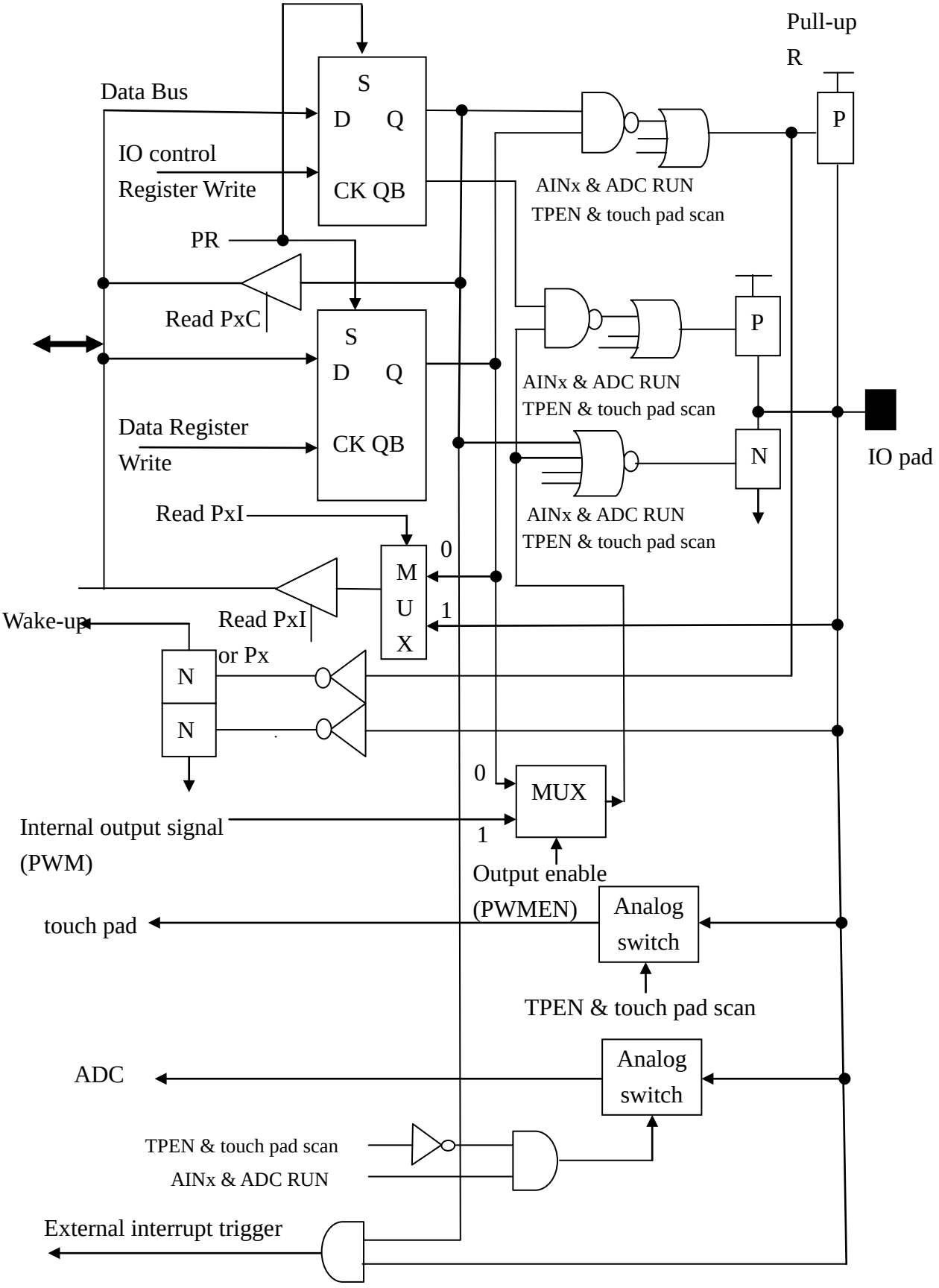


Figure IO-J: Standard IO port with touch pad input and external interrupt trigger input and ADC input and PWM output

- IO port with touch pad input and PWM output

The input/output port has the IO control register for switching input or output mode and data register stores the output data in output mode. If IO control register=1 and output data=1, the IO port is programmed as input with pull-up resistor and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PxI is reading data comes from IO pad data. The data register reading result will have the same value with output register data. Software can performs a configuration (output data register=0, changing the IO control register to 0) for open drain type that specifies suitable for key scan application. An additional feature supports the touch pad input.

Extern input	IO control data	Output data	Pull-up R	Wake-up feature
Disable	0	X	No	No
Disable	1	0	No	No
Disable	1	1	Enable	Enable
Enable and touch pad scan	X	X	No	No

X: don’t care the value.

IO control data	Internal output	IO pad
0	Enable	Output internal data
0	Disable	Output register data
1	X	IO pad input data

X: don’t care the value

Read PxI	Read input data
1	IO pad data

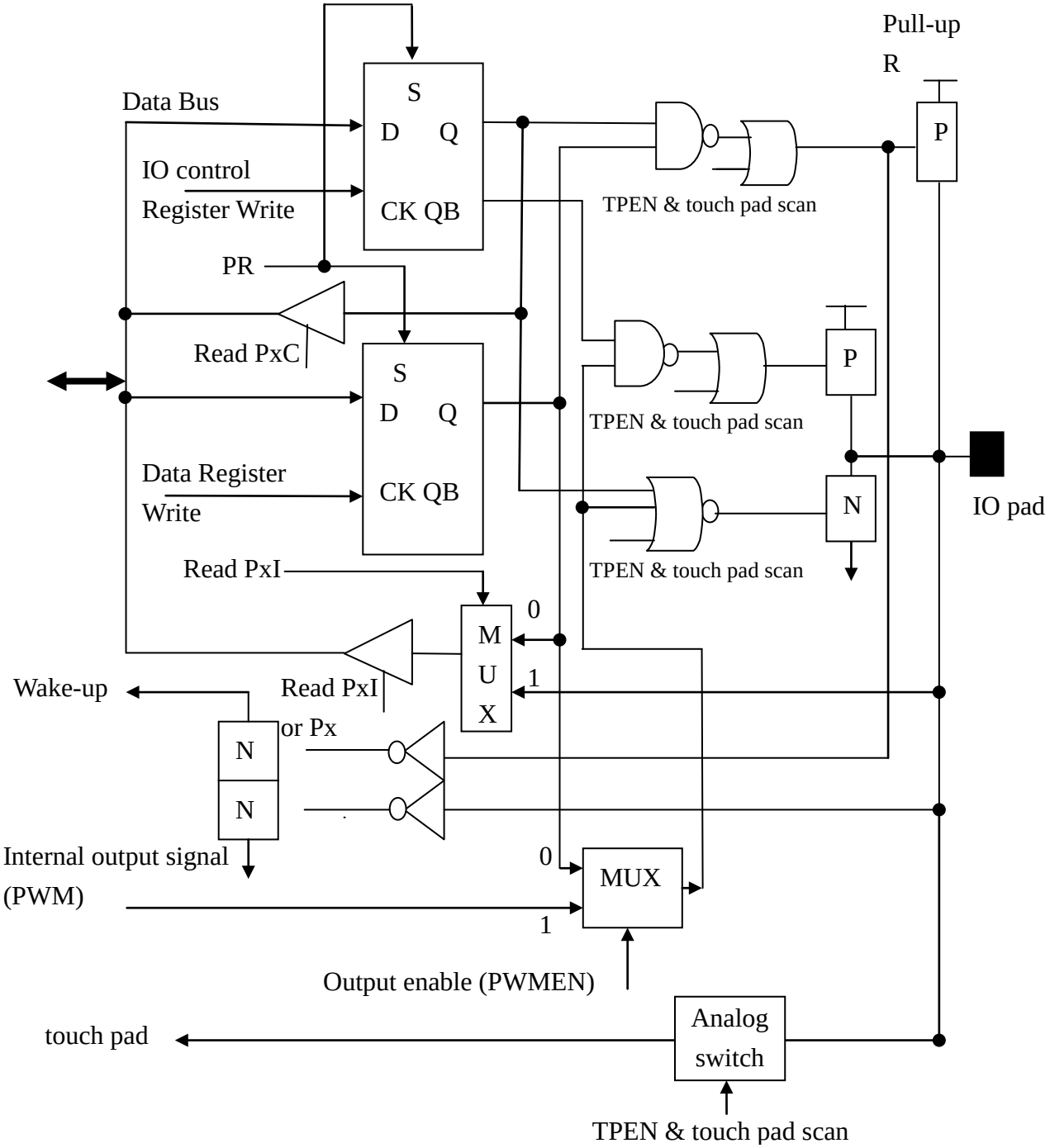


Figure IO-K: Standard IO port with touch pad input and and PWM output

P-9-1 IO Pad Cells

The main features of pad cell are including ESD/EFT protection and general IO access. A general IO pad cell can be configured as input with or without pull-up resistor, or working as a CMOS or NMOS output driver. The input pad cell must have pull-up resistor for avoiding a floating state when user doesn't care or not be used. For concerning the standby current, user can use data register or IO control register to fit the application.

P-9-2 IO File Register

PAC[010H]: Port A IO control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PAC3	PAC2	PAC1	PAC0
Read/Write	R/W	R/W	R/W	R/W

PAC3~PAC0: Port A IO control data.

PA[011H]: Port A output data register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PA3	PA2	PA1	PA0
Read/Write	R/W	R/W	R/W	R/W

PA3~PA0: Port A output data.

PBC[012H]: Port B IO control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PBC3	PBC2	PBC1	PBC0
Read/Write	R/W	R/W	R/W	R/W

PBC3~PBC0: Port B IO control data.

PB[013H]: Port B output data register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PB3	PB2	PB1	PB0
Read/Write	R/W	R/W	R/W	R/W

PB3~PB0: Port B output data.

PCC[014H]: Port C IO control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PCC3	PCC2	PCC1	PCC0
Read/Write	R/W	R/W	R/W	R/W

PCC3~PCC0: Port C IO control data.

PC[015H]: Port C output data register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PC3	PC2	PC1	PC0
Read/Write	R/W	R/W	R/W	R/W

PC3~PC0: Port C output data.

PDC[016H]: Port D IO control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PDC3	PDC2	PDC1	PDC0
Read/Write	R/W	R/W	R/W	R/W

PDC3~PDC0: Port D IO control data.

PD[017H]: Port D output data register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PD3	PD2	PD1	PD0
Read/Write	R/W	R/W	R/W	R/W

PD3~PD0: Port D output data.

PEC[018H]: Port E IO control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PEC3	PEC2	PEC1	PEC0
Read/Write	R/W	R/W	R/W	R/W

PEC3~PEC0: Port E IO control data.

PE[019H]: Port E output data register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PE3	PE2	PE1	PE0
Read/Write	R/W	R/W	R/W	R/W

PE3~PE0: Port E output data.

PFC[01AH]: Port F IO control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PFC3	PFC2	PFC1	PFC0
Read/Write	R/W	R/W	R/W	R/W

PFC3~PFC0: Port F IO control data.

PF[01BH]: Port F output data register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PF3	PF2	PF1	PF0
Read/Write	R/W	R/W	R/W	R/W

PF3~PF0: Port F output data.

PAI[200H]: Port A pad data reading address register [R], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PAI3	PAI2	PAI1	PAI0
Read/Write	R	R	R	R

PAI3~PAI0: Port A pad data.

PBI[201H]: Port B pad data reading address register [R], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PBI3	PBI2	PBI1	PBI0
Read/Write	R	R	R	R

PBI3~PBI0: Port B pad data.

PCI[202H]: Port C pad data reading address register [R], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PCI3	PCI2	PCI1	PCI0
Read/Write	R	R	R	R

PCI3~PCI0: Port C pad data.

PDI[203H]: Port D pad data reading address register [R], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PDI3	PDI2	PDI1	PDI0
Read/Write	R	R	R	R

PDI3~PDI0: Port D pad data.

PEI[204H]: Port E pad data reading address register [R], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PEI3	PEI2	PEI1	PEI0
Read/Write	R	R	R	R

PEI3~PEI0: Port E pad data.

PFI[205H]: Port F pad data reading address register [R], default value [----]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PFI3	PFI2	PFI1	PFI0
Read/Write	R	R	R	R

PFI3~PFI0: Port F pad data.

P-9-3 IO Port's Special function

When SpecIO is selected by mask option, PA0, PB0 and PB1 is special IO function. It can output ODATA register to user. ODATA can be store Key touch information by software. User set PA0 for input, PB0, PB1 for output. User can use this function to get Key touch information. Only one-key data with 15 keys can be sent.

When using special IO function, do not use IIC function. If not, PB0, PB1 are unexpected signal.

ODATA[21FH]: Touch pad output register for special function [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	ODATA3	ODATA2	ODATA1	ODATA0
Read/Write	R/W	R/W	R/W	R/W

ODATA3~ODATA0: Touch pad information.

PA0 (input)	PB0 (output)	PB1(output)
1	ODATA0	ODATA1
0	ODATA2	ODATA3

P-10: 20 non-contact inputs touch pad detector

The touch pad detector applies the charge sharing conception. The inputs share the pad with IO ports. Built-in charge sharing control, duty detector and de-bounce feature can response the input with varied output refresh rate that dependant on the system request. For power saving concern, auto power off function and wake up de-bounce capability can support a lower average operating current.

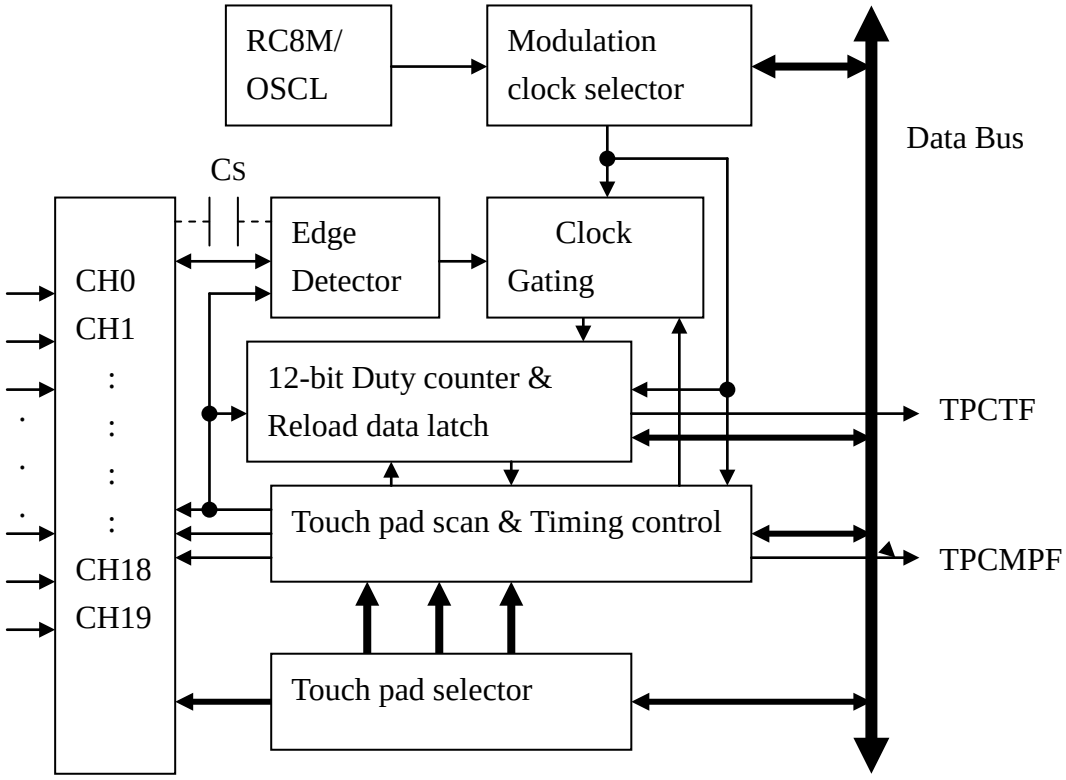
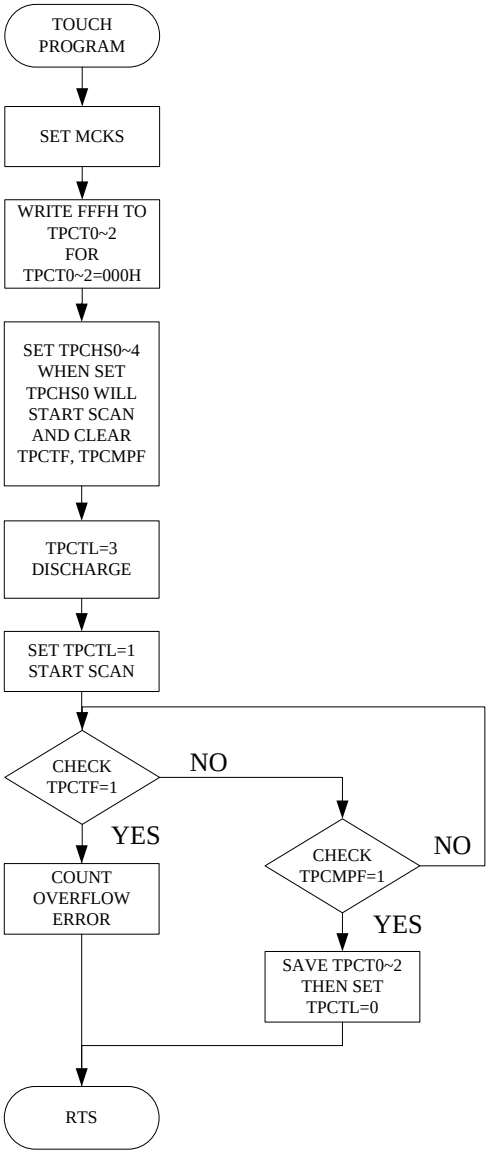


Figure: 20 pads touch pad detector

Parameters	Target Value	Remark
Touch pad clock	RC8M or OSCL	8MHz or 32KHz (typical)
Modulation clock	RC8M/N or OSCL	N=2,3,4,5,8,16,32
Duty counter	12-bit	With INT
Reload data latch	12-bit	Write only
Touch pads	1~20 Pad	-
Key de-bounce time	s/w implements	By application or cover thickness
Sensitivity level	Offset value by s/w	Resolution=1 modulation clock

The flowchart as follow:



CDSC [20DH]: Charge and discharge sequence control for touch pad detection [R/W] , default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	CDSC2	CDSC1	CDSC0
Read/write	-	R/W	R/W	R/W

CDSC2~CDSC0: Charge and discharge sequence control for touch pad detection function. When Random sequence mode is selected, CDSC function will be inhibited.

CDSC2~CDSC0	Sequence change clock N
000	OFF
001	2
010	4
011	6
100	8
101	12
110	16
111	Reserve

ADJSTAT [219H]: Frequency Adjustment Status flag register [R], default value [--11]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	OSCHADJF	TBADJF
Read/write	-	-	R	R

TBADJF: Time base adjustment status flag. (0: busy; 1: idle)

OSCHADJF: OSCH frequency adjustment status flag. (0: busy; 1: idle)

OSCHADJ [218H]: OSCH frequency adjustment register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	FADJ1	FADJ0	FST1	FST0
Read/write	R/W	R/W	R/W	R/W

FST1~FST0: Frequency Shift Time selector.

FST1~FST0	Frequency Shift Time (us)
00	6
01	10
10	16
11	20

FADJ1~FADJ0: OSCH Frequency adjustment range selector.

FADJ1~FADJ0	Frequency adjustment range	value
00	Disable	0
01	-1,0,+1	±1
10	-2,-1,0,+1,+2	±2
11	-3,-2,-1,0,+1,+2,+3	±3

FADJ set the frequency swing range, when the change time in register FST is set, frequency shift function will be activated. Swing shift back and forth from the center frequency. Set FADJ=0 to off frequency shift function. When frequency shift function is executing, OSCHADJF will be set 0. Then user can not change FADJ and FST, but only can be set 0 to off function. Frequency shift function will not immediately stop, when FST is set to 0, the need to wait until the frequency back to the original frequency, while OSCHADJF will be set to 1.

The frequency shift shift function needs to be linked with the TP RUN. When the TP scan starts, the frequency shift starts. When TP STOP, the frequency shift stops. During the initial period of CS, the frequency shift does not start and the OSCH can be returned to the 0 position. In this way, each time TP RUN, the frequency can be guaranteed to start from the direction of 0->1->2->3..., that is, the frequency change is consistent during each TP process, and the stray capacitance is relatively large. Under the slightest change in frequency will affect the data, the data does not jump.

(When TP STOP, return to 0 as soon as possible and stop shifting, evaluate the longest time)

TPCON0 [241H]: Touch pad control 0 register [R/W], default value [--00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	TPNIS	CSAMODE
Read/write	-	-	R/W	R/W

CSAMODE: CSA mode selector for touch pad scan.

0: C array as a touch pad capacitance compensation.(Load)

1: C array as a touch pad current compensation.(Gain)

TPNIS: Touch pad detection type selector.

0: Touch pad detector use Schmitt trigger output signal.

1: Touch pad detector use comparator output signal.

TPCON1 [242H]: Touch pad control 0 register [R/W], default value [-010]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	VREFS2	VREFS1	VREFS0
Read/write	-	R/W	R/W	R/W

VREFS2~VREFS0: Voltage reference selector for touch pad detector.

000: 5/14 $V_{TP.}$

001: 6/14 $V_{TP.}$

010:7/14 $V_{TP.}$

011:8/14 $V_{TP.}$

100: 9/14 $V_{TP.}$

101: Reserved.

110: Reserved

111: Reserved.

(V_{TP} = VDD when LDO disable, V_{TP} = V_{LDO} when LDO enable.)

TPINTC[00EH]: Touch pad interrupt control register [R/W], default value [000-]

TPINTC	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTIE	TPCMPIE	TPATIE	-
Read/Write	R/W	R/W	R/W	-

TPATIE: TP auto mode measure interrupt enable. (0: disable; 1: enable)

TPCMPIE: Capacitor overcharge interrupt enable. (0: disable; 1: enable)

TPCTIE: Duty counter overflow interrupt enable. (0: disable; 1: enable)

TPINTF[00FH]: Touch pad interrupt request flag register [R/W], default value [000-]

TPINTF	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTF	TPCMF	TPATF	-
Read/Write	R/W	R/W	R/W	-

TPATF: TP auto mode measure flag. (0: inactive; 1: active)

TPCMPF: Capacitor overcharge's flag. (0: inactive; 1: active)

TPCTF: Duty counter's overflow flag. (0: inactive; 1: active)

TPCT0[249H]: Touch pad duty counter & latch data 0 register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCT3	TPCT2	TPCT1	TPCT0
Read/Write	R/W	R/W	R/W	R/W

TPCT3~TPCT0: Duty counter 1st nibble for counter read.

TPCT1[24AH]: Touch pad duty counter & latch data 1 register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCT7	TPCT6	TPCT5	TPCT4
Read/Write	R/W	R/W	R/W	R/W

TPCT7~TPCT4: Duty counter 2nd nibble for counter read.

TPCT2[24BH]: Touch pad duty counter & latch data 2 register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCT11	TPCT10	TPCT9	TPCT8
Read/Write	R/W	R/W	R/W	R/W

TPCT11~TPCT8: Duty counter 3rd nibble for counter read.

Duty counter value= TPCT2*256 +TPCT1*16+TPCT0

When user writes data to the TPCT2~TPCT0, the data just keep in TPCT2~TPCT0 latch register. When TPCHS0 is writing, the TPCT2~TPCT0 latch register's complement value will load into TPCT2~TPCT0 duty counter as initial value and start the scan function.

The duty counter will be enabled by writing the TPCHS0 register and will set the TPCTF

flag if duty counter overflow. As writing any of the TPCHS0 addresses will reload the 12 bit counters and clear the TPCTF & TPCMPF.

The TPCMPF will be set as no modulation clock going into duty counter with de-bounce feature and will also call the interrupt as TPCMPIE=1.

MCKS[240H]: Modulation clock selector register [R/W], default value [0111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	MCKS3	MCKS2	MCKS1	MCKS0
Read/Write	R/W	R/W	R/W	R/W

MCKS3~MCKS0: Modulation clock selector.

MCKS3~MCKS0	Sample time	MCKS3~MCKS0	Sample time
0000	RC8M/2	0100	RC8M/8
0001	RC8M/3	0101	RC8M/16
0010	RC8M/4	0110	RC8M/32
0011	RC8M/5	0111	OSCL
1000	Random sequence	-	-

OSCL=32KHz.

Random sequence:

With the half-wave period T=62.5nS of RC8M, they are divided into the following combinations:

Item	Positive half cycle *T	Negative half cycle *T	Frequency (MHz)
1	2	2	4
2	2	3	3.2
3	2	4	2.65
4	3	2	3.2
5	3	3	2.65
6	3	4	2.285
7	3	5	2
8	3	6	1.775
9	4	2	2.65
10	4	3	2.285
11	4	4	2
12	4	5	1.775
13	4	6	2.6
14	5	3	2
15	5	4	1.775
16	5	5	2.6

At the beginning of TP, the charge and discharge frequency is switched according to a fixed random sequence {f1, f2, f3, f4, f5....., fn}.

Where fi is an arbitrary number between 1 and 16, the corresponding frequency and duty ratio are as shown above; The arrangement between f1 and fn is irregular; When n to 400, the sequence can be repeated to reduce the complexity.

After each TP charge and discharge starts, it should be performed in the same arrangement until the TP process is completed.

When Random sequence mode is selected, CDSC function will be inhibited.

TPCHS0[243H]: Touch pad channel selector 0 register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPEN3	TPEN2	TPEN1	TPEN0
Read/Write	R/W	R/W	R/W	R/W

TPEN3~TPEN0: Touch pad channel selector 1st nibble.

TPCHS1[244H]: Touch pad channel selector 1 register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPEN7	TPEN6	TPEN5	TPEN4
Read/Write	R/W	R/W	R/W	R/W

TPEN7~TPEN4: Touch pad channel selector 2nd nibble.

TPCHS2[245H]: Touch pad channel selector 2 register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPEN11	TPEN10	TPEN9	TPEN8
Read/Write	R/W	R/W	R/W	R/W

TPEN11~TPEN8: Touch pad channel selector 3rd nibble.

TPCHS3[246H]: Touch pad channel selector 3 register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPEN15	TPEN14	TPEN13	TPEN12
Read/Write	R/W	R/W	R/W	R/W

TPEN15~TPEN12: Touch pad channel selector 4th nibble.

TPCHS4[247H]: Touch pad channel selector 4 register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPEN19	TPEN18	TPEN17	TPEN16
Read/Write	R/W	R/W	R/W	R/W

TPEN19~TPEN16: Touch pad channel selector 5th nibble.

As program writes the TPCHS0 register hardware automatically discharges the external capacitor and enables the sensor clock input until period end.

Channel Enable State	TPCHS0 TPEN3~0	TPCHS1 TPEN7~4	TPCHS2 TPEN11~8	TPCHS3 TPEN15~12	TPCHS4 TPEN19~16
TP0	0001	0000	0000	0000	0000
TP1	0010	0000	0000	0000	0000
TP2	0100	0000	0000	0000	0000
TP3	1000	0000	0000	0000	0000
TP4	0000	0001	0000	0000	0000
TP5	0000	0010	0000	0000	0000
TP6	0000	0100	0000	0000	0000
TP7	0000	1000	0000	0000	0000
TP8	0000	0000	0001	0000	0000
TP9	0000	0000	0010	0000	0000
TP10	0000	0000	0100	0000	0000
TP11	0000	0000	1000	0000	0000
TP12	0000	0000	0000	0001	0000
TP13	0000	0000	0000	0010	0000
TP14	0000	0000	0000	0100	0000
TP15	0000	0000	0000	1000	0000
TP16	0000	0000	0000	0000	0001
TP17	0000	0000	0000	0000	0010
TP18	0000	0000	0000	0000	0100
TP19	0000	0000	0000	0000	1000

When TPCHS0 is writing, TPCTL will be set TP RUN mode, and touch pad begin to scan touch pad.

Users can enable multi-channel by setting corresponding bit 1, which will turn on all enable channel at the same time.

Set TP RUN or TP AUTO mode in TPCTL and start touch pad scanning

TPCTL[248H]: Touch pad control register [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	TPCTL2	TPCTL1	TPCTL0
Read/Write	-	R/W	R/W	R/W

TPCTL2~TPCTL0: Touch pad control selector.

As program writes the TPCTL register hardware automatically discharges the external capacitor and enables the sensor clock input until period end.

TPCTL2~TPCTL0	Channel Enable State
000	TP STOP
001	TP RUN
010	TP AUTO
011	Discharge
100	Inner pad
101	-
110	TP SLPH
111	TP SLPL

TP STOP: STOP the touch pad feature and release pad for IO port.
TP RUN: TP RUN is touchpad scan start signal, its scan the channel by TPCHS4~0 select.
TP AUTO: TP AUTO is automatically scanned according to the settings of CSINIT and RPTTM and the result is placed in TPACTx. RPTTM repeats up to 6 times, if the number of times is set to 7, the 7th result will cover the first time register.
Discharge: Discharge can hold touch pad in discharge state, to avoid discharge time too short.
Inner pad: Select switch select Inner pad. Inner pad is reference Key, this pad is no bounding to package.
TP SLPH: TP SLPH is high speed automatically scanned according to the settings of CSINIT and TPSPLLH and TPSLPLL and TB1OV and MCU into sleep mode. If the measured value exceeds or equal the upper limit or falls below or equal the lower limit, wake up.
TP SLPL: TP SLPL is low speed automatically scanned according to the settings of CSINIT and TPSPLLH and TPSLPLL and MCU into sleep mode. If the measured value exceeds or equal the upper limit or falls below or equal the lower limit, wake up.

As writing the TPCTL register (exclude select TP STOP) will reload the 12-bit duty counter and clear the TPCTF and TPCMPF.
As touch pad analog switch keeps on, the relative IO port is disabled as tri-state by hardware.

CSAL[23EH]: Capacity load low nibble selector register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	CSA3	CSA2	CSA1	CSA0
Read/Write	R/W	R/W	R/W	R/W

CSA3~CSA0: Capacity load selector for touch pad.

CSAH[23FH]: Capacity load high nibble selector register [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	CSA6	CSA5	CSA4
Read/Write	-	R/W	R/W	R/W

CSA6~CSA4: Capacity load selector for touch pad.

TPCON0 [241H]: Touch pad control 0 register [R/W], default value [--00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	TPNIS	CSAMODE
Read/write	-	-	R/W	R/W

CSAMODE: CSA mode selector for touch pad scan.

0: C array as a touch pad capacitance compensation.(Load)

1: C array as a touch pad current compensation.(Gain)

TPNIS: Touch pad detection type selector.

0: Touch pad detector use Schmitt trigger output signal.

1: Touch pad detector use comparator output signal.

CSA6~ CSA0	Capacity load	CSA6~ CSA0	Capacity load	CSA6~ CSA0	Capacity load	CSA6~ CSA0	Capacity load
000 0000	0.0 pf	010 0000	16.0 pf	100 0000	32.0 pf	110 0000	48.0 pf
000 0001	0.5 pf	010 0001	16.5 pf	100 0001	32.5 pf	110 0001	48.5 pf
000 0010	1.0 pf	010 0010	17.0 pf	100 0010	33.0 pf	110 0010	49.0 pf
000 0011	1.5 pf	010 0011	17.5 pf	100 0011	33.5 pf	110 0011	49.5 pf
000 0100	2.0 pf	010 0100	18.0 pf	100 0100	34.0 pf	110 0100	50.0 pf
000 0101	2.5 pf	010 0101	18.5 pf	100 0101	34.5 pf	110 0101	50.5 pf
000 0110	3.0 pf	010 0110	19.0 pf	100 0110	35.0 pf	110 0110	51.0 pf
000 0111	3.5 pf	010 0111	19.5 pf	100 0111	35.5 pf	110 0111	51.5 pf
000 1000	4.0 pf	010 1000	20.0 pf	100 1000	36.0 pf	110 1000	52.0 pf
000 1001	4.5 pf	010 1001	20.5 pf	100 1001	36.5 pf	110 1001	52.5 pf
000 1010	5.0 pf	010 1010	21.0 pf	100 1010	37.0 pf	110 1010	53.0 pf
000 1011	5.5 pf	010 1011	21.5 pf	100 1011	37.5 pf	110 1011	53.5 pf
000 1100	6.0 pf	010 1100	22.0 pf	100 1100	38.0 pf	110 1100	54.0 pf
000 1101	6.5 pf	010 1101	22.5 pf	100 1101	38.5 pf	110 1101	54.5 pf
000 1110	7.0pf	010 1110	23.0pf	100 1110	39.0pf	110 1110	55.0pf
000 1111	7.5 pf	010 1111	23.5 pf	100 1111	39.5 pf	110 1111	55.5 pf
001 0000	8.0 pf	011 0000	24.0 pf	101 0000	40.0 pf	111 0000	56.0 pf
001 0001	8.5 pf	011 0001	24.5 pf	101 0001	40.5 pf	111 0001	56.5 pf
010 0010	9.0 pf	011 0010	25.0 pf	101 0010	41.0 pf	110 0010	57.0 pf
001 0011	9.5 pf	011 0011	25.5 pf	101 0011	41.5 pf	111 0011	57.5 pf
001 0100	10.0 pf	011 0100	26.0 pf	101 0100	42.0 pf	111 0100	58.0 pf
001 0101	10.5 pf	011 0101	26.5 pf	101 0101	42.5 pf	111 0101	58.5 pf
001 0110	11.0 pf	011 0110	27.0 pf	101 0110	43.0 pf	111 0110	59.0 pf
001 0111	11.5 pf	011 0111	27.5 pf	101 0111	43.5 pf	111 0111	59.5 pf
001 1000	12.0 pf	011 1000	28.0 pf	101 1000	44.0 pf	111 1000	60.0 pf
001 1001	12.5 pf	011 1001	28.5 pf	101 1001	44.5 pf	111 1001	60.5 pf
001 1010	13.0 pf	011 1010	29.0 pf	101 1010	45.0 pf	111 1010	61.0 pf
001 1011	13.5 pf	011 1011	29.5 pf	101 1011	45.5 pf	111 1011	61.5 pf
001 1100	14.0 pf	011 1100	30.0 pf	101 1100	46.0 pf	111 1100	62.0 pf
001 1101	14.5 pf	011 1101	30.5 pf	101 1101	46.5 pf	111 1101	62.5 pf
001 1110	15.0 pf	011 1110	31.0 pf	101 1110	47.0 pf	111 1110	63.0 pf
001 1111	15.5 pf	011 1111	31.5 pf	101 1111	47.5 pf	111 1111	63.5 pf

TPINTC[00EH]: Touch pad interrupt control register [R/W], default value [000-]

TPINTC	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTIE	TPCMPIE	TPATIE	-
Read/Write	R/W	R/W	R/W	-

TPATIE: TP auto mode measure interrupt enable. (0: disable; 1: enable)

TPCMPIE: Capacitor overcharge interrupt enable. (0: disable; 1: enable)

TPCTIE: Duty counter overflow interrupt enable. (0: disable; 1: enable)

TPINTF[00FH]: Touch pad interrupt request flag register [R/W], default value [000-]

TPINTF	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTF	TPCMF	TPATF	-
Read/Write	R/W	R/W	R/W	-

TPATF: TP auto mode measured flag. (0: inactive; 1: active)

TPCMPF: Capacitor overcharge’s flag. (0: inactive; 1: active)

TPCTF: Duty counter’s overflow flag. (0: inactive; 1: active)

P-10-1 TP Auto Scan

TP AUTO is automatically scanned according to the settings of CSINIT and RPTTM and the result is placed in TPACTx. RPTTM repeats up to 6 times, if the number of times is set to 7, the 7th result will cover the first time register, if the measurement overflow occurs (TPCTF=1), stop the measurement and record the result as FFFH, If the number of set measurements is not completed, continue to measure. The TPCTF and TPCMPF flags are cleared before the measurement. Therefore, if the interrupt is enabled, the possible flag in the interrupt subroutine is cleared. It is recommended not to use the interrupt function. Users cannot clear TPCMF and TPCTF by themselves during TP AUTO measurement, otherwise the function will not be completed normally.

The interrupt request flag TPATF will be set when the measurement ends, if software enables the corresponding interrupt enable bit, interrupt hardware will cause MCU interrupt service routine.

CSINIT[280H]: Cs capacitor initialization timer register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	CSIT3	CSIT2	CSIT1	CSIT0
Read/Write	R/W	R/W	R/W	R/W

CSIT3~CSIT0: Cs capacitor initialization timer.

CSIT3~CSIT0	value	CSIT3~CSIT0	value
0000	0	1000	128
0001	1	1001	256
0010	2	1010	512
0011	4	1011	1024
0100	8	1100	2048
0101	16	1101	4096
0110	32	1110	Reserved
0111	64	1111	Reserved

CS Initialization time = TP Modulation clock period x (Value)

RPTTM[282H]: Repeat counter [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	REPT2	REPT1	REPT0
Read/Write	-	R/W	R/W	R/W

REPT2~REPT0: Repeat measurement times for touch pad auto mode.

RPTTM repeats up to 6 times.

TPACT00 [24EH]: TP Auto measurement counter 0_0 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT03	TPACT02	TPACT01	TPACT00
Read/Write	R	R	R	R

TPACT03~ TPACT00: TP Auto measurement counter 0 low nibble data.

TPACT01 [24FH]: TP Auto measurement counter 0_1 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT07	TPACT06	TPACT05	TPACT04
Read/Write	R	R	R	R

TPACT07~ TPACT04: TP Auto measurement counter 0 middle nibble data.

TPACT02 [250H]: TP Auto measurement counter 0_2 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT011	TPACT010	TPACT09	TPACT08
Read/Write	R	R	R	R

TPACT011~ TPACT08: TP Auto measurement counter 0 high nibble data.

TPACT10 [251H]: TP Auto measurement counter 1_0 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT13	TPACT12	TPACT11	TPACT10
Read/Write	R	R	R	R

TPACT13~ TPACT10: TP Auto measurement counter 1 low nibble data.

TPACT11 [252H]: TP Auto measurement counter 1_1 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT17	TPACT16	TPACT15	TPACT14
Read/Write	R	R	R	R

TPACT17~ TPACT14: TP Auto measurement counter 1 middle nibble data.

TPACT12 [253H]: TP Auto measurement counter 1_2 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT111	TPACT110	TPACT19	TPACT18
Read/Write	R	R	R	R

TPACT111~ TPACT18: TP Auto measurement counter 1 high nibble data.

TPACT20 [254H]: TP Auto measurement counter 2_0 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT23	TPACT22	TPACT21	TPACT20
Read/Write	R	R	R	R

TPACT23~ TPACT20: TP Auto measurement counter 2 low nibble data.

TPACT21 [255H]: TP Auto measurement counter 2_1 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT27	TPACT26	TPACT25	TPACT24
Read/Write	R	R	R	R

TPACT27~ TPACT24: TP Auto measurement counter 2 middle nibble data.

TPACT22 [256H]: TP Auto measurement counter 2_2 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT211	TPACT210	TPACT29	TPACT28
Read/Write	R	R	R	R

TPACT211~ TPACT28: TP Auto measurement counter 2 high nibble data.

TPACT30 [257H]: TP Auto measurement counter 3_0 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT33	TPACT32	TPACT31	TPACT30
Read/Write	R	R	R	R

TPACT33~ TPACT30: TP Auto measurement counter 3 low nibble data.

TPACT31 [258H]: TP Auto measurement counter 3_1 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT37	TPACT36	TPACT35	TPACT34
Read/Write	R	R	R	R

TPACT37~ TPACT34: TP Auto measurement counter 3 middle nibble data.

TPACT32 [259H]: TP Auto measurement counter 3_2 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT311	TPACT310	TPACT39	TPACT38
Read/Write	R	R	R	R

TPACT311~ TPACT38: TP Auto measurement counter 3 high nibble data.

TPACT40 [25AH]: TP Auto measurement counter 4_0 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT43	TPACT42	TPACT41	TPACT40
Read/Write	R	R	R	R

TPACT43~ TPACT40: TP Auto measurement counter 4 low nibble data.

TPACT41 [25BH]: TP Auto measurement counter 4_1 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT47	TPACT46	TPACT45	TPACT44
Read/Write	R	R	R	R

TPACT47~ TPACT44: TP Auto measurement counter 4 middle nibble data.

TPACT42 [25CH]: TP Auto measurement counter 4_2 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT411	TPACT410	TPACT49	TPACT48
Read/Write	R	R	R	R

TPACT411~ TPACT48: TP Auto measurement counter 4 high nibble data.

TPACT50 [25DH]: TP Auto measurement counter 5_0 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT53	TPACT52	TPACT51	TPACT50
Read/Write	R	R	R	R

TPACT53~ TPACT50: TP Auto measurement counter 5 low nibble data.

TPACT51 [25EH]: TP Auto measurement counter 5_1 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT57	TPACT56	TPACT55	TPACT54
Read/Write	R	R	R	R

TPACT57~ TPACT54: TP Auto measurement counter 5 middle nibble data.

TPACT52 [25FH]: TP Auto measurement counter 5_2 register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPACT511	TPACT510	TPACT59	TPACT58
Read/Write	R	R	R	R

TPACT511~ TPACT58: TP Auto measurement counter 5 high nibble data.

P-10-2 Hardware Sleep

TP SLPH is high speed automatically scanned according to the settings of CSINIT and TPSPLLH and TPSLPLL and TB1OV and MCU enters low speed SLEEP mode. CSINIT is the CS initialization time before measurement, and the time is the set value multiplied by the modulation frequency selected by MCKS. If the measured value exceeds the upper limit or falls below the lower limit, wake up and display the comparison result in TPSLPS. Every time TB1OV is triggered, it must be reset to avoid the triggering of the trigger in the middle and not wake up normally. TP SLPH uses a high-speed modulation frequency to start the high-speed OSCH. After the measurement is completed, return to the low speed SLEEP mode and wait for the next trigger. The TPCTF and TPCMPF flags are cleared before the measurement. Therefore, if the interrupt is enabled, the possible flag in the interrupt subroutine is cleared. It is recommended not to use the interrupt function.

TP SLPL is low speed automatically scanned according to the settings of CSINIT and TPSPLLH and TPSLPLL and MCU enters low speed SLEEP mode. CSINIT is the CS initialization time before measurement, and the time is the set value multiplied by the OSCL frequency. If the measured value exceeds the upper limit or falls below the lower limit, wake up and display the comparison result in TPSLPS, otherwise continue to measure. The TPCTF and TPCMPF flags are cleared before the measurement. Therefore, if the interrupt is enabled, the possible flag in the interrupt subroutine is cleared. It is recommended not to use the interrupt function.

CSINIT[280H]: Cs capacitor initialization timer register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	CSIT3	CSIT2	CSIT1	CSIT0
Read/Write	R/W	R/W	R/W	R/W

CSIT3~CSIT0: Cs capacitor initialization timer.

CSIT3~CSIT0	value	CSIT3~CSIT0	value
0000	0	1000	128
0001	1	1001	256
0010	2	1010	512
0011	4	1011	1024
0100	8	1100	2048
0101	16	1101	4096
0110	32	1110	Reserved
0111	64	1111	Reserved

CS Initialization time = TP Modulation clock period x (Value)

TPSLPLL0[283H]: TP sleep limit low value register 0 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPLL3	TPLL2	TPLL1	TPLL0
Read/Write	R/W	R/W	R/W	R/W

TPLL3~ TPLL0: TP sleep limit low value low nibble data.

TPSLPLL1[284H]: TP sleep limit low value register 1 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPLL7	TPLL6	TPLL5	TPLL4
Read/Write	R/W	R/W	R/W	R/W

TPLL7~ TPLL4: TP sleep limit low value middle nibble data.

TPSLPLL2[285H]:TP sleep limit low value register 2 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPLL11	TPLL10	TPLL9	TPLL8
Read/Write	R/W	R/W	R/W	R/W

TPLL11~ TPLL8: TP sleep limit low value high nibble data.

TPSLPLH0[286H]: TP sleep limit high value register 0 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPLH3	TPLH2	TPLH1	TPLH0
Read/Write	R/W	R/W	R/W	R/W

TPLH3~ TPLH0: TP sleep limit high value low nibble data.

TPSLPLH1[287H]: TP sleep limit high value register 1 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPLH7	TPLH6	TPLH5	TPLH4
Read/Write	R/W	R/W	R/W	R/W

TPLH7~ TPLH4: TP sleep limit high value middle nibble data.

TPSLPLH2[288H]: TP sleep limit high value register 2 [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPLH11	TPLH10	TPLH9	TPLH8
Read/Write	R/W	R/W	R/W	R/W

TPLH11~ TPLH8: TP sleep limit high value high nibble data.

TPSLPS[24CH]: Touch pad sleep status register [R], default value [--00]

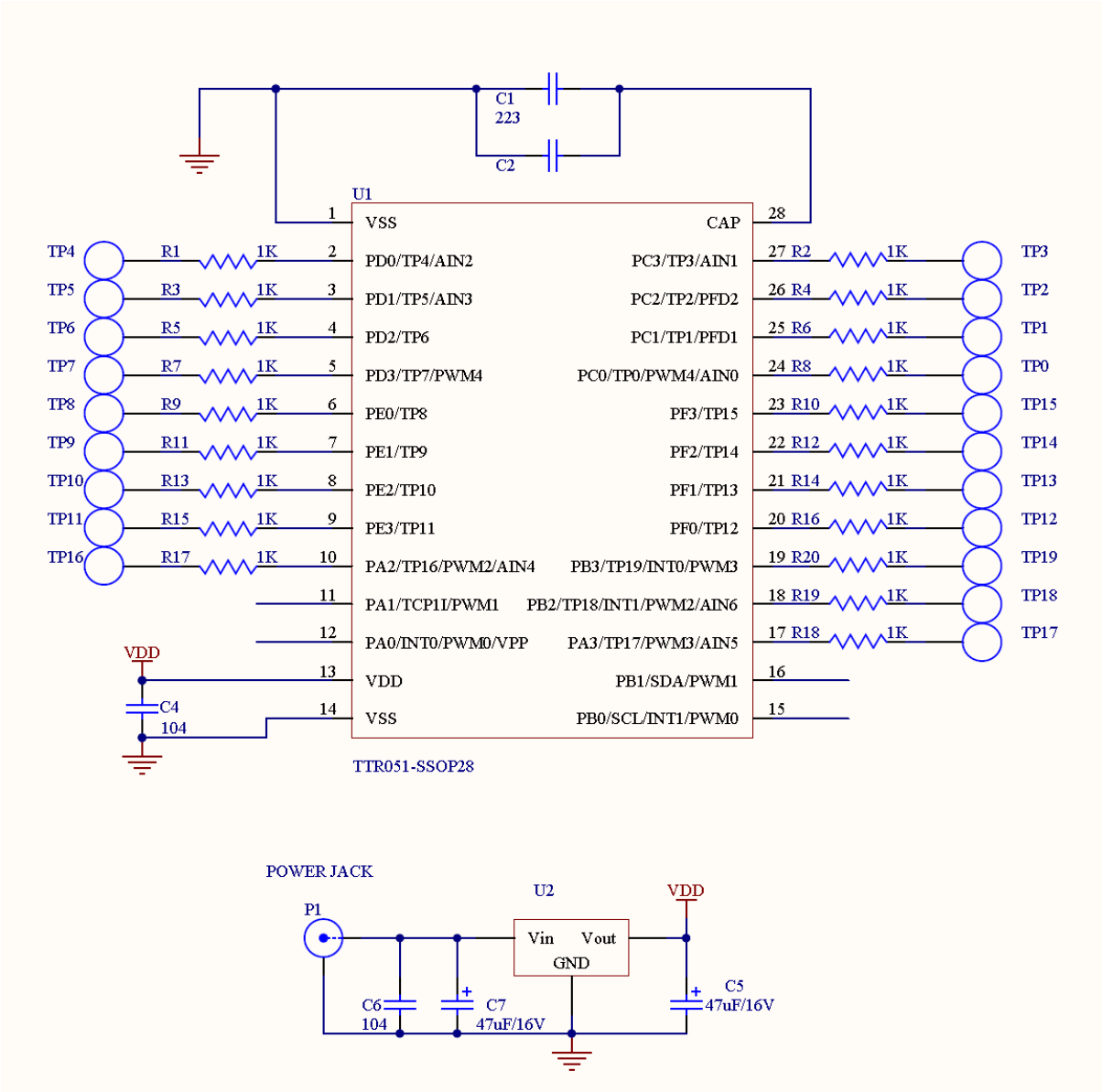
TPINTF	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	TPSLPLLS	TPSLPLHB
Read/Write	-	-	R	R

TPSLPLHB: The TP sleep scan result bigger than TPSLPLH value flag. (0: not bigger or equal; 1: bigger)

TPSLPLLS: The TP sleep scan result smaller than TPSLPLL value flag. (0: not smaller; 1: smaller or equal)

Application Circuit:

Reference only



Package Information:

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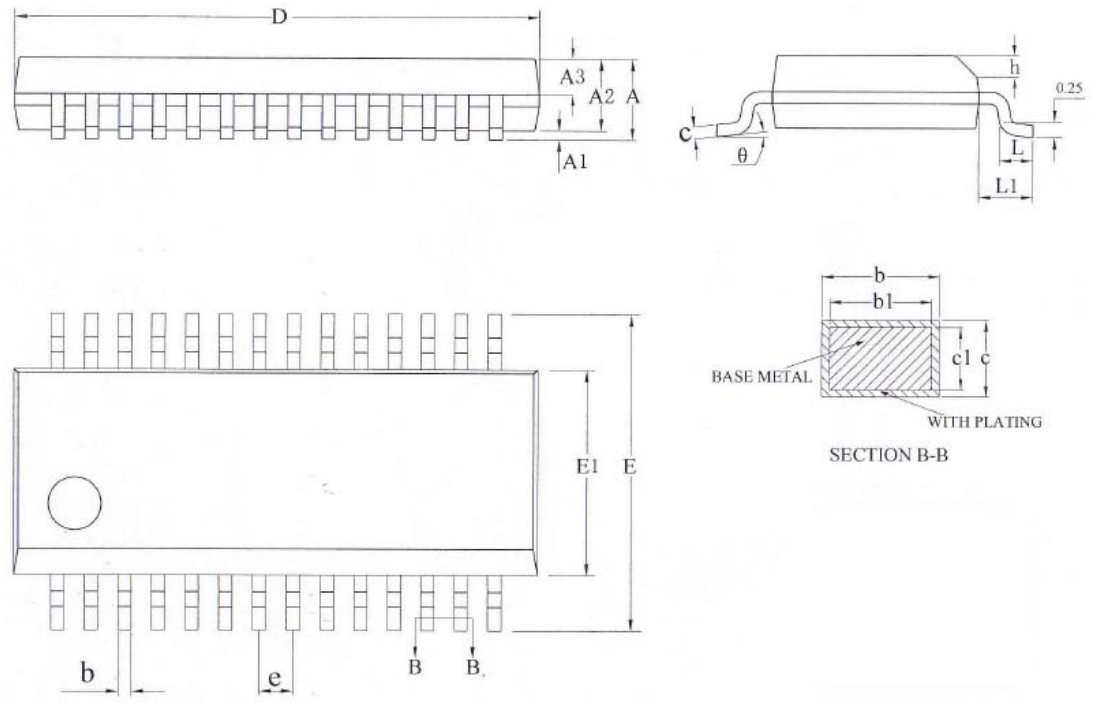

Symbol Parameter (Unit : mm)														
A			A1			A2			A3			b		
Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
		1.75	0.05		0.225	1.30	1.40	1.50	0.60	0.65	0.70	0.23		0.31

Symbol Parameter (Unit : mm)														
b1			c			c1			D			E		
Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
0.22	0.25	0.28	0.20		0.24	0.19	0.20	0.21	9.80	9.90	10.00	5.80	6.00	6.20

Symbol Parameter (Unit : mm)														
E1			e			h			L			L1		
Min	Nom	Max		Typ		Min	Nom	Max	Min	Nom	Max		Typ	
3.80	3.90	4.00	0.635 BSC			0.25		0.50	0.50		0.80	1.05 BSC		

Symbol Parameter (Unit : mm)		
θ		
Min	Nom	Max
0		8°

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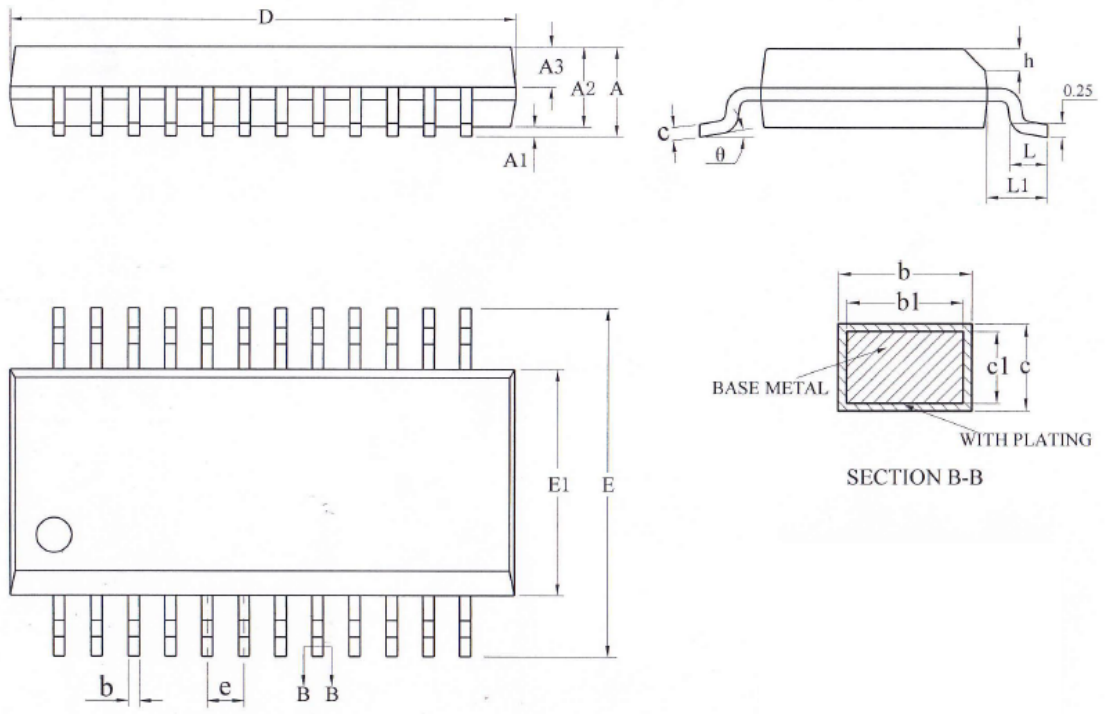
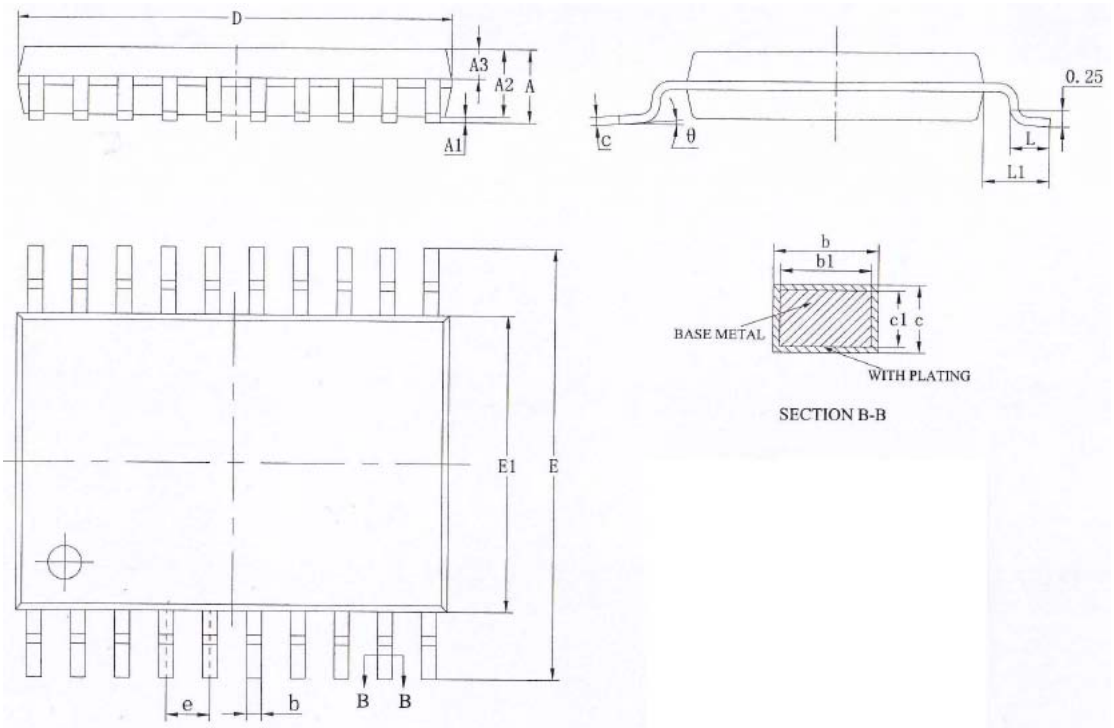


Symbol Parameter (Unit : mm)														
A			A1			A2			A3			b		
Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
		1.75	0.10	0.15	0.25	1.30	1.40	1.50	0.60	0.65	0.70	0.23		0.31

Symbol Parameter (Unit : mm)														
b1			c			c1			D			E		
Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
0.22	0.25	0.28	0.20		0.24	0.19	0.20	0.21	8.55	8.65	8.75	5.80	6.00	6.20

Symbol Parameter (Unit : mm)														
E1			e		h			L			L1		θ		
Min	Nom	Max	Typ		Min	Nom	Max	Min	Nom	Max	Typ		Min	Nom	Max
3.80	3.90	4.00	0.635 BSC		0.30		0.50	0.50		0.80	1.05 REF		0		8°

TSSOP 20



Symbol Parameter (Unit : mm)														
A			A1			A2			A3			b		
Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
		1.20	0.05		0.15	0.80	1.00	1.05	0.39	0.44	0.49	0.20		0.28

Symbol Parameter (Unit : mm)														
b1			c			c1			D			E1		
Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
0.19	0.22	0.25	0.13		0.17	0.12	0.13	0.14	6.40	6.50	6.60	4.30	4.40	4.50

Symbol Parameter (Unit : mm)														
E			e			L			L1			θ		
Min	Nom	Max		Typ		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
6.20	6.40	6.60	0.65 BSC			0.45	0.60	0.75	1.00 REF			0		8°

Ordering Information

TTR051	
Package Item	**Package Type**
TTR051-ASFN	SSOP28
TTR051-HSEN	SSOP24
TTR051-DTDN	TSSOP20

Revision History:

1. 2022/05/25：Version: 1.0
   Initial version.
2. 2022/06/07：Version: 2.0
   Add description of ADC
3. 2023/02/20：Version:2.1
   Add TTR051-SSOP24