8-CHANNEL ADPCM VOICE SYNTEHSIS LSI

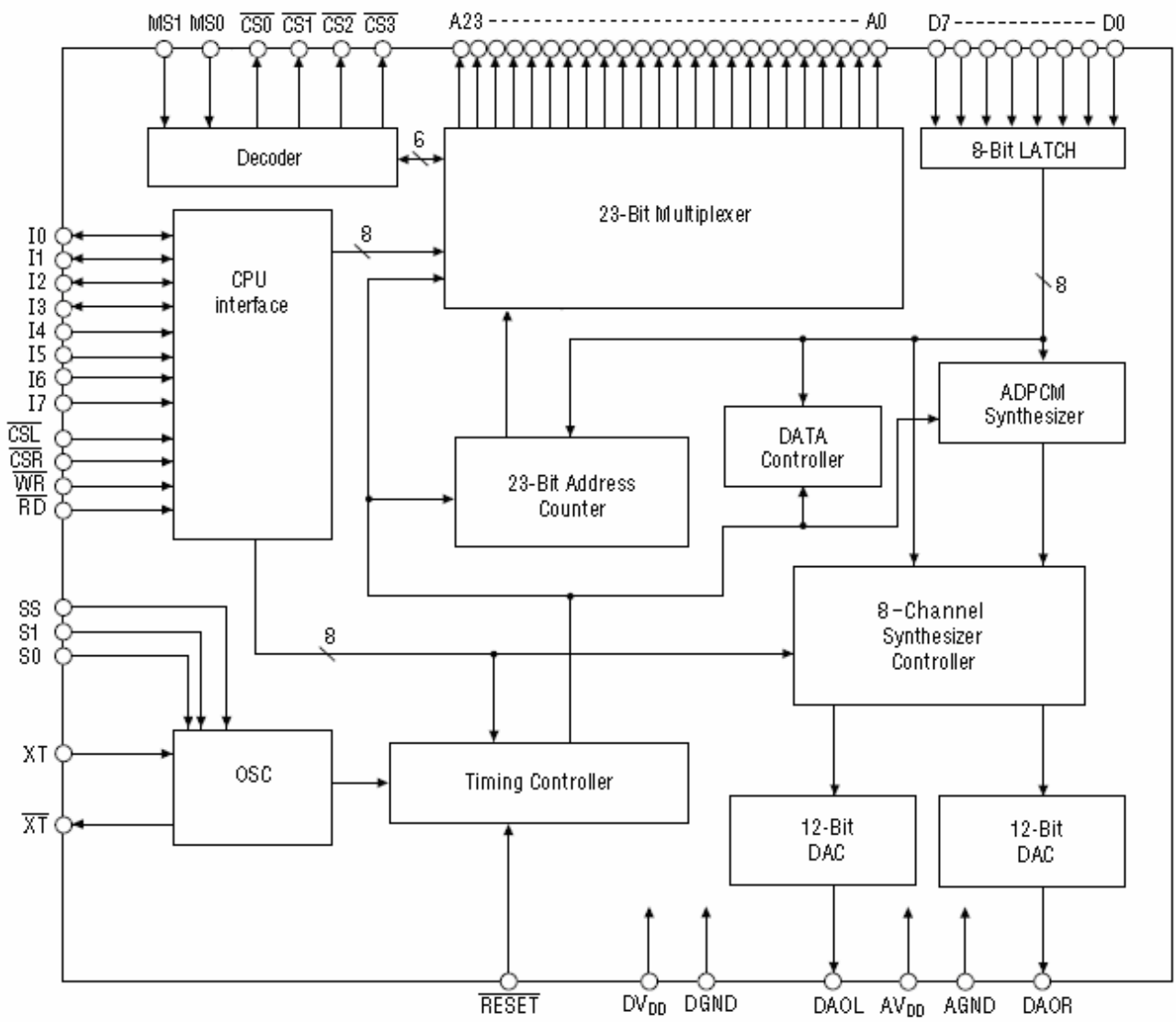
GENERAL DESCRIPTION

The TT5665 is a 8-channel mixing ADPCM voice synthesis LSI which offers R & L sound outputs with 4 channels for each. The TT5665 can access an external voice data ROM for sound effects or speech voice. The maximum external ROM size is 16M*8 bit and can direct access. The TT5665 has an 8-channel synthesis stage which allows the simultaneous playback of eight different channels. It is used to have a voice with BGM (Back Ground Music) effect, instrumental sound, echo effect etc.

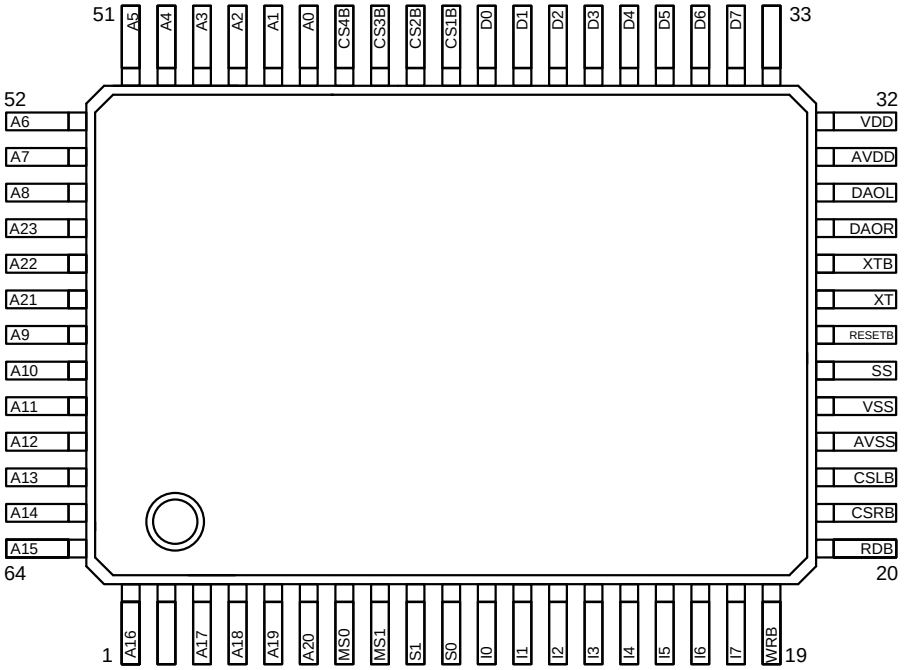
FEATURES

- Advance ADPCM algorithm
- Number of bits/sample: 4
- 24 address lines for external ROM
- 8-bit control bus for mode setting
- External memory capacity 128Mbit
- Interface with common CPU and MPU
- Clock frequency with Sampling frequency: (clock 1 MHz to 4 MHz)
  - At 1.088 MHz clock
    DAOR : 8 kHz and 6.4 kHz
    DAOL : 8 kHz , 4 kHz , and 6.4 kHz , 3.2 kHz
  - At 2.176 MHz clock
    DAOR : 16 kHz and 12.8 kHz
    DAOL : 16 kHz , 8 kHz , 4 kHz and 12.8 kHz , 6.4 kHz
    3.2 kHz
  - At 4.352 MHz clock
    DAOR : 32 kHz and 25.6 kHz
    DAOL : 32 kHz , 16 kHz , 8 kHz , 4 kHz and 25.6 kHz , 12.8 kHz
    6.4 kHz , 3.2 kHz
- Number of words: 511 maximum
- Vocalization time: 64 minutes maximum (at 8 kHz, sample rate)
- Sound output channel (DAOR/L with 4 channels for each)
- Built-in DA converter: 12-bit
- DAO output format: A-class
- Voice level attenuation: OdB~-24dB on each channel (9steps) with -3dB/step
- Advance low power CMOS process
- 5 V or 3.3 V single power supply
- 64-pin plastic QFP

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>Pin No(64)</th><th>I/O</th><th>Function</th></tr>
<tr><td>I_0 ~ I_3</td><td>11~14</td><td>I/O</td><td rowspan="2">Instruction bus and condition outputs.
These pins are inputs for phrase specification Maximum number of phrases is 511, l_0~ l_3 pins are also outputs of the operating state, busy state, for channels 1~4 and are further used to select the channel attenuation rate.</td></tr>
<tr><td>I_4 ~ I_7</td><td>15~18</td><td>I</td></tr>
<tr><td>WRB</td><td>19</td><td>I</td><td>Write enable input. Data is written on the data bus of l_0~ l_7 The data is written when $\overline{WR}$ goes low</td></tr>
<tr><td>RDB</td><td>20</td><td>I</td><td>Read enable input.
The output busy state of channels 1~4 on the data bus of l_0~ l_3 can be read using this input. A high level indicates busy</td></tr>
<tr><td>CSRB
CSLB</td><td>21,22</td><td>I
I</td><td>Chip select input. Input “L” level either when $\overline{WR}$ signal is input or when $\overline{RD}$ signal is input</td></tr>
<tr><td>RESETB</td><td>26</td><td>I</td><td>Reset input. Reset condition is available by inputting “L” level
All functions are suspended during reset</td></tr>
<tr><td>A_0~A_{23}</td><td>46~64
1~6</td><td>O</td><td>Address outputs.
These pins are to address the external ROM in which voice data is stored</td></tr>
<tr><td>D_0 ~ D_7</td><td>34~41</td><td>I</td><td>Voice data inputs.</td></tr>
<tr><td>SS
S1
S0</td><td>25
9
10</td><td>PIH
PIL
PIL</td><td>Sampling frequency select input:
When oscillation frequency is 1.088 MHz or 4.352 MHz, the following choices are available by inputting “H” level or “L” level to SS.
And “<u>DAOL</u>” can be setting the other sampling frequency by “S1”&”S0” option pins.
The setting is below the table: (* not suggestion)
Unit :KHz
<table>
<tr><td></td><td></td><td colspan="4">SS= “1”</td><td colspan="4">SS=:”0”</td></tr>
<tr><td colspan="2">(S1,S0)</td><td>00</td><td>01</td><td>10</td><td>11</td><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td rowspan="2">Osc = 1.088M</td><td>DAOR</td><td>8</td><td>8</td><td>8</td><td>8</td><td>6.4</td><td>6.4</td><td>6.4</td><td>6.4</td></tr>
<tr><td>DAOL</td><td>8</td><td>4</td><td>2*</td><td>1*</td><td>6.4</td><td>3.2</td><td>1.6*</td><td>0.8*</td></tr>
<tr><td rowspan="2">Osc = 2.176M</td><td>DAOR</td><td>16</td><td>16</td><td>16</td><td>16</td><td>12.8</td><td>12.8</td><td>12.8</td><td>12.8</td></tr>
<tr><td>DAOL</td><td>16</td><td>8</td><td>4</td><td>2*</td><td>12.8</td><td>6.4</td><td>3.2</td><td>1.6*</td></tr>
<tr><td rowspan="2">Osc = 4.352M</td><td>DAOR</td><td>32</td><td>32</td><td>32</td><td>32</td><td>25.6</td><td>25.6</td><td>25.6</td><td>25.6</td></tr>
<tr><td>DAOL</td><td>32</td><td>16</td><td>8</td><td>4</td><td>25.6</td><td>12.8</td><td>6.4</td><td>3.2</td></tr>
</table></td></tr>
<tr><td>DAOR
DAOL</td><td>29
30</td><td>O
O</td><td>Voice synthesis output.
Voice synthesized analog signal is output from this pin.</td></tr>
<tr><td>XT</td><td>27</td><td>I</td><td>Crystal oscillator pin.</td></tr>
<tr><td>XTB</td><td>28</td><td>O</td><td>Crystal oscillator pin.</td></tr>
<tr><td>VDD</td><td>32</td><td>P</td><td>Power Supply pin.</td></tr>
<tr><td>AVDD</td><td>31</td><td>P</td><td>Analog Power Supply pin.</td></tr>
<tr><td>VSS</td><td>24</td><td>P</td><td>Ground pin.</td></tr>
<tr><td>AVSS</td><td>23</td><td>P</td><td>Analog Ground pin.</td></tr>
<tr><td>MS0
MS1</td><td>7
8</td><td>PIL
PIL</td><td>Memory size selection bits:
00: 1M; 01: 2M; 10: 4M; 11:8M byte (MS1,MS0)</td></tr>
<tr><td>CS1B</td><td>42</td><td>O</td><td>00: 0~1M; 01: 0~2M; 10: 0~4M; 11:0~8M byte.</td></tr>
<tr><td>CS2B</td><td>43</td><td>O</td><td>00: 1~2M; 01: 2~4M; 10: 4~8M; 11:8~16M byte.</td></tr>
<tr><td>CS3B</td><td>44</td><td>O</td><td>00: 2~3M; 01: 4~6M; 10: 8~12M; 11:8~16M byte.</td></tr>
<tr><td>CS4B</td><td>45</td><td>O</td><td>00: 3~4M; 01: 6~8M; 10: 12~16M; 11:8~16M byte.</td></tr>
</table>

ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	VDD	Ta=25°C	-0.3~+7.0	V
Input voltage	V_{IN}	Ta=25°C	-0.3~VDD +0.3	V
Storage temperature	T_{stg}	—	-55 ~ 150	°C

- **Recommended Operating Conditions**

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	VDD	VSS=0V	2.9 ~ +5.5	V
Operating temperature	T_{op}	VSS=0V	-40 ~ +85	°C
Oscillation frequency	f_{osc}	VSS=0V	1~5	MHz

- **DC Characteristics**

(Vdd = 2. 9 ~ 5.5V,VSS=0V,Ta = -40 ~ 85°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
"L" input current	I_{IL}	V_{IL}=VSS	-10	—	—	μA
"H" input current	I_{IH}	V_{IH}=VDD	—	—	10	
"L" input voltage	V_{IL}	—	—	—	0.2Vdd	V
"H" input voltage	V_{IH}	—	0.8Vdd	—	—	
"L" output voltage	V_{OL}	I_{LO}=0.8mA	—	—	0.45	V
"H" output voltage	V_{OH}	I_{OH}=-40μA	Vdd	—	—	
Output leakage current	I_{LO}	VSS≤V_{OUT}≤VDD	-10	—	10	μA
Operating current	I_{DD}	f_{OSC}=4.0MHz	—	5	10	mA
DA output relative error	$\lvert V_{DAE} \rvert$	No load	—	—	20	mV
DA output impedance	R_{DAOUT}	—	—	15	—	kΩ

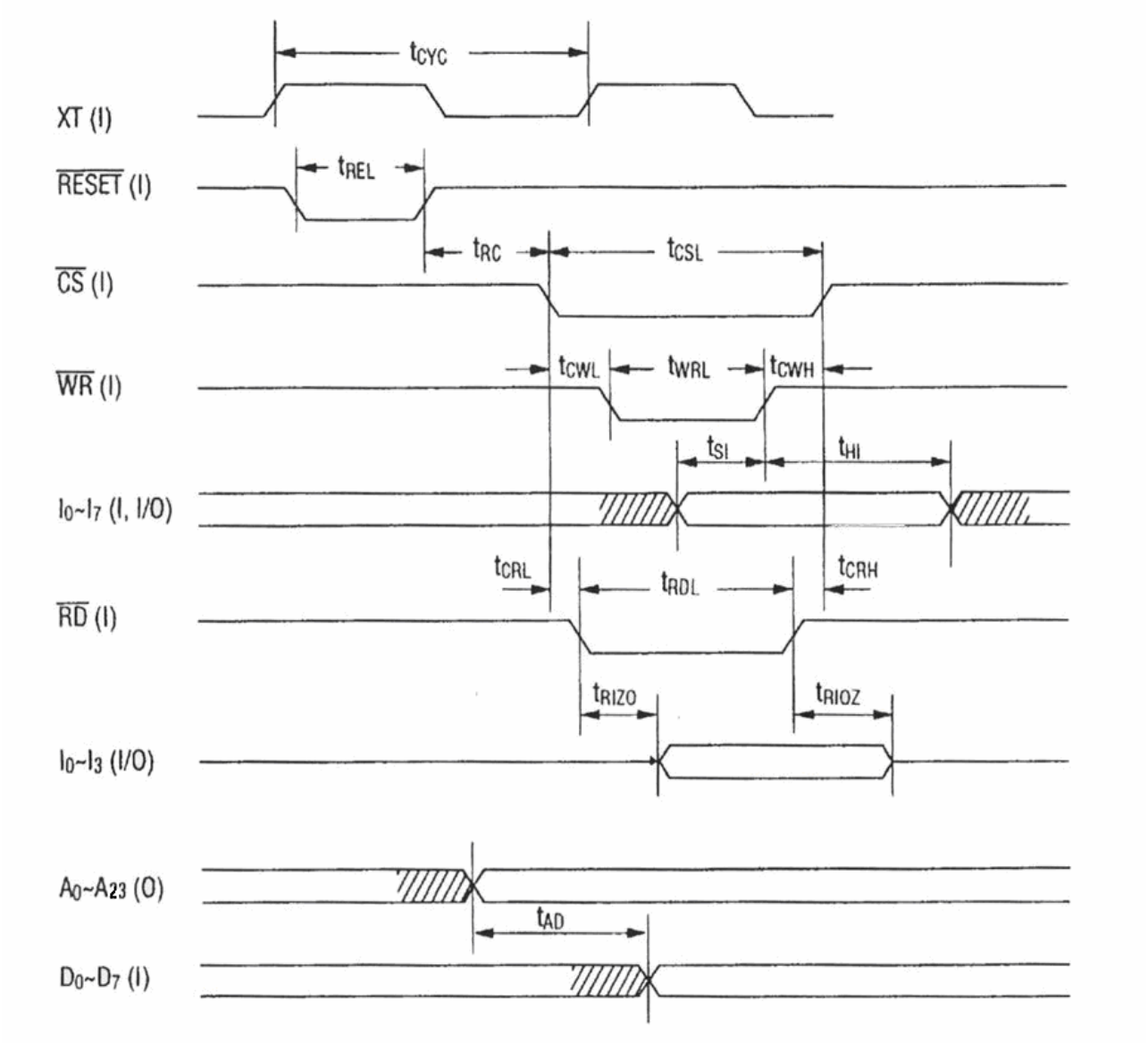
• **AC Characteristics**

VDD = 4.5~5.5V,VSS=0V,Ta= -40 ~ +85°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Clock cycle	t_{CYC}	200	-	-	ns
Clock duty cycle	f_{DUTY}	40	50	60	%
$\overline{RESET}$ pulse width	t_{REL}	100	-	-	ns
$\overline{CS}$ pulse width	t_{CSL}	250	-	-	ns
$\overline{WR}$ pulse width	t_{WRL}	200	-	-	ns
$\overline{RD}$ pulse width	t_{RDL}	300	-	-	ns
$\overline{RESET}$ fall to $\overline{CS}$ fall	t_{RC}	250	-	-	ns
$\overline{CS}$ fall to $\overline{WR}$ fall	t_{CWL}	50	-	-	ns
$\overline{WR}$ raise to $\overline{CS}$ raise	t_{CWH}	0	-	-	ns
Data set up time of I_0-I_7 in respect to $\overline{WR}$ raise	t_{SI}	80	-	-	ns
Data hold time of I_0-I_7 in respect to $\overline{WR}$ raise	t_{HI}	80	-	-	ns
$\overline{RD}$ fall to stable output of I_0-I_3	t_{RIZO}	-	-	120	ns
$\overline{RD}$ raise to flow status output of I_0-I_3	t_{RIOZ}	0	-	120	ns
$\overline{CS}$ fall to $\overline{RD}$ fall	t_{CRL}	20	-	-	ns
$\overline{RD}$ raise to $\overline{CS}$ raise	t_{CRH}	0	-	-	ns
Address stable (A_0-A_{23}) to data input of D_0-D_7	t_{AD}	-	-	$5 \cdot t_{CYC}+90$	ns

PS : CS => $\overline{CSR}$, $\overline{CSL}$

TIMMING CHART



FUNCTION EXPLANATION

1. Phrase Selection

Phrase Selection Phrases are specified and read into the 2 byte data which consists of I_0~ I_7 data bus. The phrase selection data is latched when WRB goes high while CSLB or CSRB is low (L).The format of the phrase specification input is as follows.

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
1st Byte	1	Phrase selection data						
2nd Byte	**Phrase expansion II6,II7 & Channel specification II4,II5**				Reduction specification II3~II0			

As shown in the above chart, I_7 of the first 1 data byte is always 1. I_0~I_6 of the first data byte specifies the low phrase address and the I7,I6 of second byte are used as high phrase address. The phrase selection data has a selection of 511 phrases which corresponds to 000000001~111111111. The phrase selection data is used for to A_3~A_{11} address outputs, and they specify both start and stop address which are stored in the external ROM.

Relation between Phrase Selection Data and ROM Address

Phrase Selection Data		**II_7**	**II_6**	I_6	I_5	I_4	I_3	I_2	I_1	I_0	-	-	-
External ROM address	A_{23}~A_{10}	**A_{11}**	**A_{10}**	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Selection													
Not valid	0~0	0	0	0	0	0	0	0	0	0	0	0	0
Phrase 1	0~0	0	0	0	0	0	0	0	0	1	0	0	0
Phrase 2	0~0	0	0	0	0	0	0	0	1	0	0	0	0
Phrase 3	0~0	0	0	0	0	0	0	0	1	1	0	0	0
Phrase 510	0~0	1	1	1	1	1	1	1	1	0	0	0	0
Phrase 511	0~0	1	1	1	1	1	1	1	1	1			

* Phrases can not be specified with all inputs = “0”

The second byte of data specifies the high phrase address, the synthesis operating channel as well as specific channel reduction of the synthesized play-back. The channel selection format is shown below. It is not possible to specify multiple channels at the same time.

Phrase expansion bits

The data bits II7 & II6 of second byte and the data bits I6~I0 of first byte will Combine as the total phrase address A11~A3.

Channel Specification

Channel	II_5	II_4
1	0	0
2	0	1
3	1	0
4	1	1

Reduction Specification

All zero is considered as 0 dB of the relative sound itself. The reduction is made through 9 levels from about 0 dB to - 24 dB with the steps of about - 3 dB. Reduction format is shown below.

Reduction Selection

Attenuation level	I_3	I_2	I_1	I_0
0dB	0	0	0	0
-3.2 dB	0	0	0	1
-6.0 dB	0	0	1	0
-9.2 dB	0	0	1	0
-12.0dB	0	1	0	0
-14.5dB	0	1	0	1
-18.0dB	0	1	1	0
-20.5dB	0	1	1	1
-24.0dB	1	0	0	0

2. Voice Synthesis Channel Suspension

Voice synthesis operation of any channel can be suspended. Channel suspension is controlled by bits I_3~ I_6 of data bytes I_0~I_{07}. To suspend a channel, make I_7=0, while I_3~ I_6 represent the channels which should be suspended Channel suspension occurs even if multiple channels are selected. For example, if I_3~ I_6 are all 1 and I_7=0, then channels 1~4 are suspended simultaneously.

Suspended channel	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
1	0	0	0	0	1	×	×	×
2	0	0	0	1	0	×	×	×
3	0	0	1	0	0	×	×	×
4	0	1	0	0	0	×	×	×

3 .Data ROM

1) ADDRESS DATA

This specifics start and stop address of ADPCM speech data. One phrase start and end address consists of 8 bytes. The first 3 bytes show start address while the last 3 bytes show stop address. The other 2 bytes are empty. By selecting the first address in which the start address is stored, the selected speech data is played back.

Address 0	SA_1
Address 1	SA_2
Address 2	SA_3
Address 3	EA_1
Address 4	EA_2
Address 5	EA_3
Address 6	EMPTY
Address 7	EMPTY

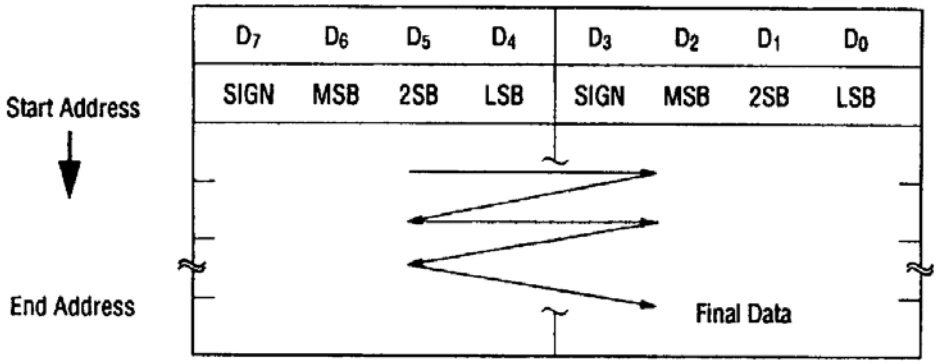
Start addresses (SA_1~SA_3) and stop addresses (EA_1~EA_3) are stored according to the chart shown below

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SA_1/ EA_1	**A23**	**A22**	**A21**	**A20**	**A19**	**A18**	A_{17}	A_{16}
SA_2/ EA_2	A_{15}	A_{14}	A_{13}	A_{11}	A_{10}	A_{15}	A_9	A_8
SA_3/ EA_3	A_7	A_6	A_5	A_3	A_2	A_{15}	A_1	A_0

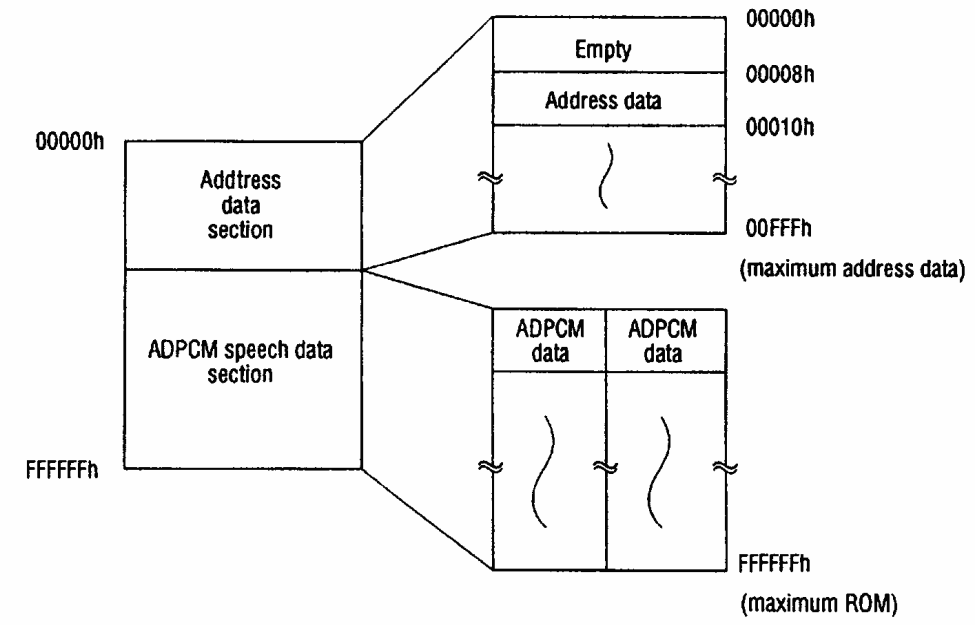
2) ADPCM SPEECH DATA

ADPCM speech data consists of (2) 4-bit samples. So, 1 byte stores 2 samples. The data arrangement proceeds from higher rank bits (D_4~D_7) to lower rank bits (D_0~D_3). The storage of speech data should always be ended with the lower rank bit, So, always store an even number of samples, Speech data is produced by Speech Development Tool TT5665.

3) DATA ROM STRUCTURE



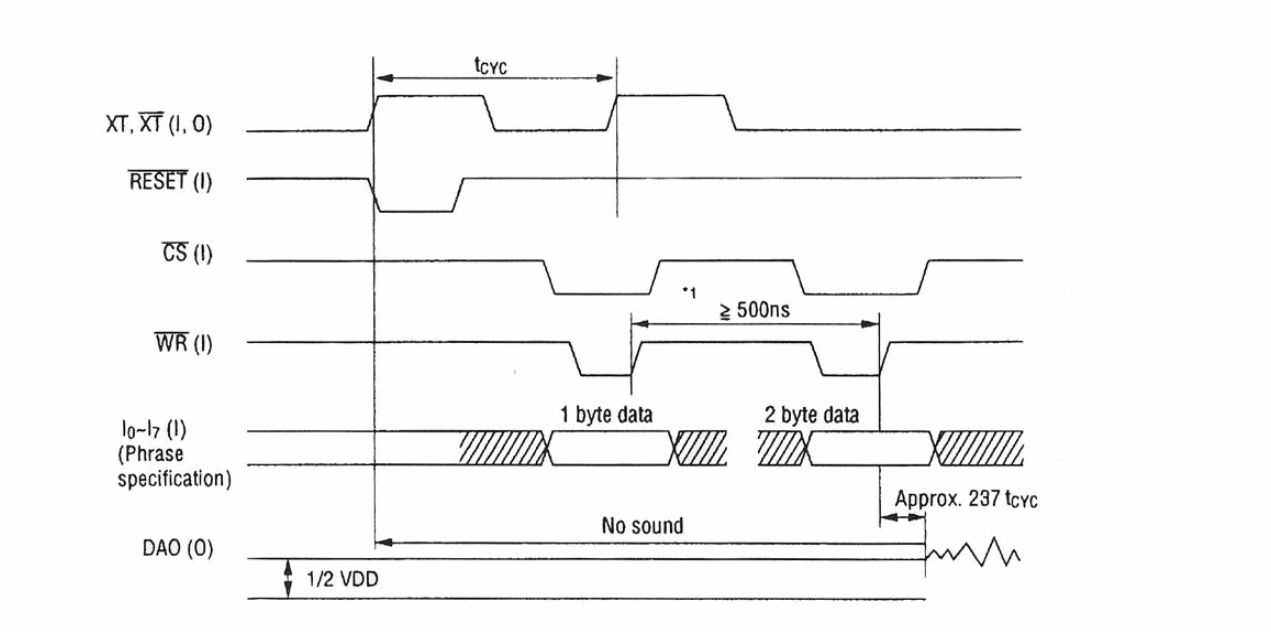
When 1 phrase is selected, address data is written from ROM address 00008h to 0000Fh, When the maximum 511 phrases are selected in address data section, the data is written up to ROM address 00FFFh. and the rest is used as the ADPCM data section. The following chart shows the memory map of the source data ROM.



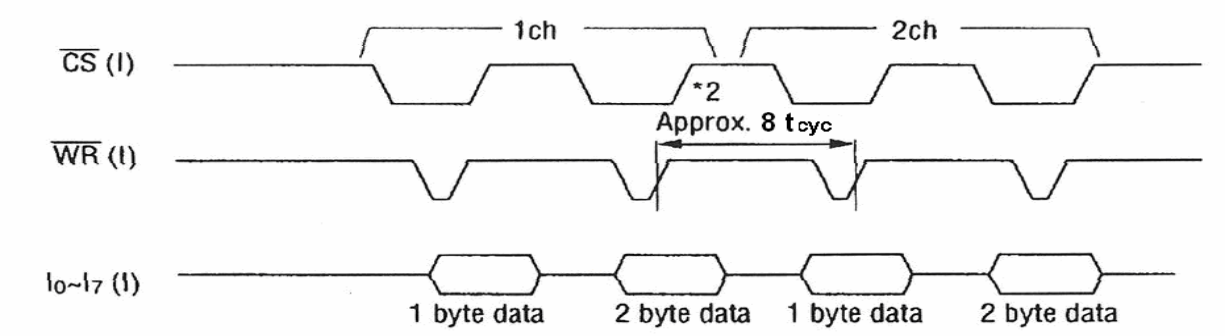
FUNCTIONAL DESCRIPTION

1. Phrase Selection Input

This procedure is to input phrase selection data onto the data bus inputs I_0~I_7. The data is latched internally when $\overline{WR}$ rises from "L" to "H", while $\overline{CSL}$ or $\overline{CSR}$ remains "L". Voice synthesis operation does not start till the second byte is fully latched



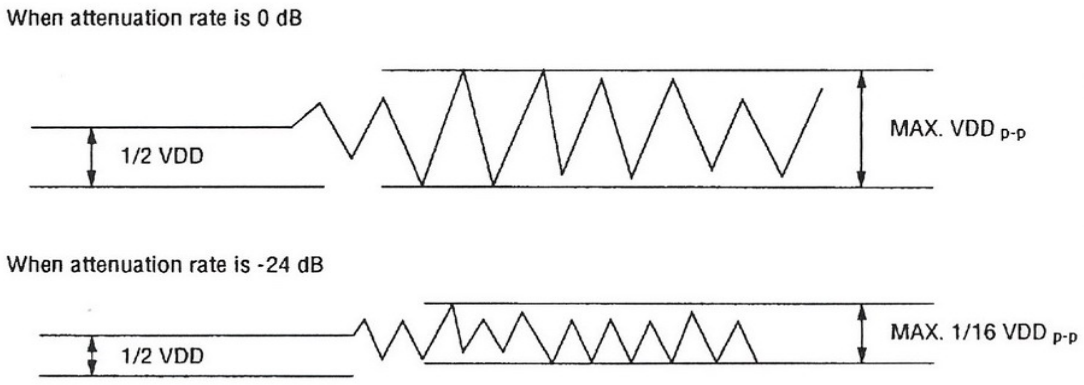
Note： Phrase selection is from channel 1 to channel 8 continuously
If all of CH1~CH8 CMM are latched, then the DAO(R/L) output Arrrox.. 420 tcyc.
*1 An interval of 75 T_{CYC} (max.) is needed between phrases



Note*2 Oscillation frequency = 1.088 MHz SS = "L'

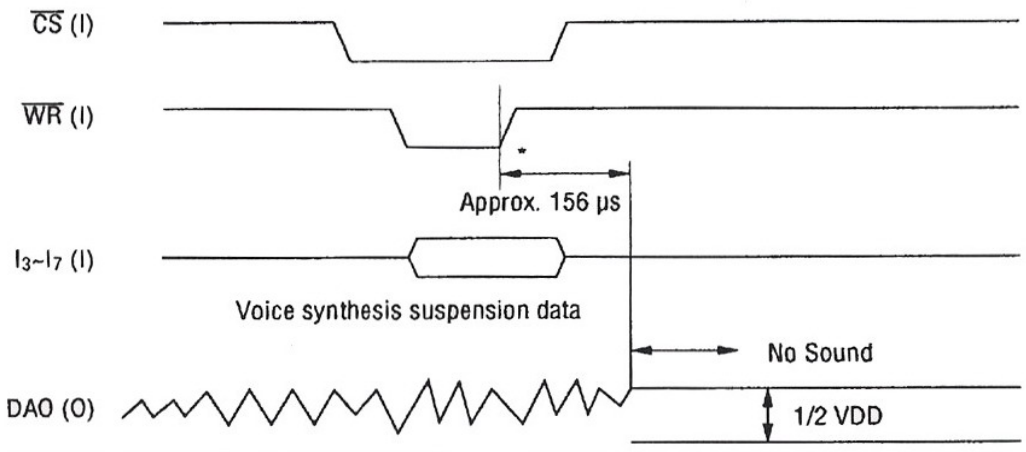
Voice synthesis playback can be started from any channel, l to 8. The arrangement of each channel can be in any order. The second byte of the phrase selection data contains the phrase attenuation data in bits D_0 - D_3. Synthesized data is attenuated in -3 dB steps from 0 dB to -24 dB.

2. Attenuation of Synthesized Speech



3. Speech Synthesis Channel Suspension

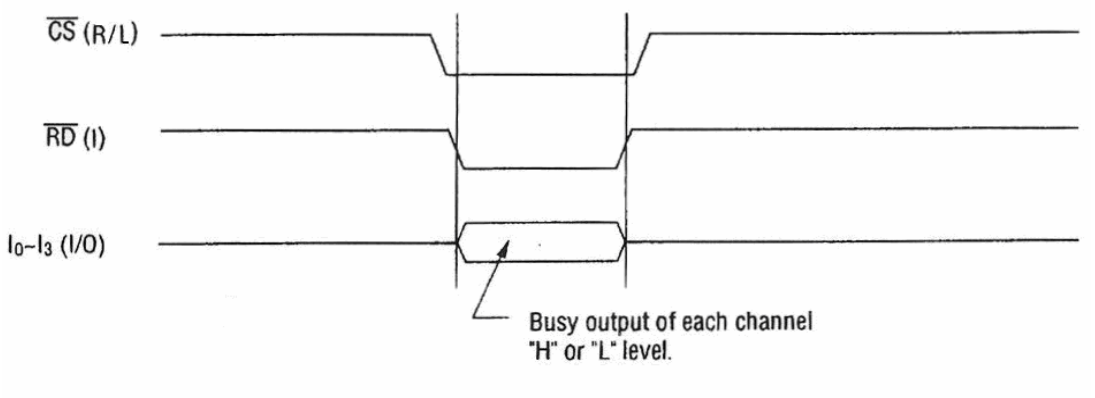
This is accomplished by writing the synthesis channel suspension data onto data bus inputs I_3~I_7 The data is latched internally when $\overline{WR}$ goes from "L" to "H" while $\overline{CS}$ (R/L) remains active (L). Since synthesis suspension data is 1 byte data, synthesis operation is suspended right after the rising edge of $\overline{WR}$. Multiple channels can be specified, making it possible to suspend channels 1~4 simultaneously.



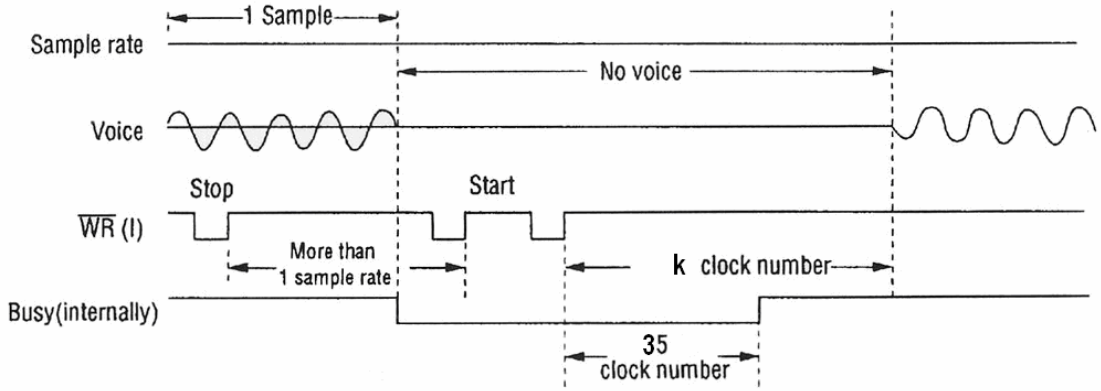
Note: * Oscillation frequency = 1.088 MHz SS= “L”

4. Reading the Busy Status

While $\overline{CS}$ (R/L) is "L" and $\overline{RD}$ is "L", each operation state, the busy state of channels 1~4 is output on I_0~I_3. "H" is output during synthesized playback.



5. Start and Stop of 1 Channel

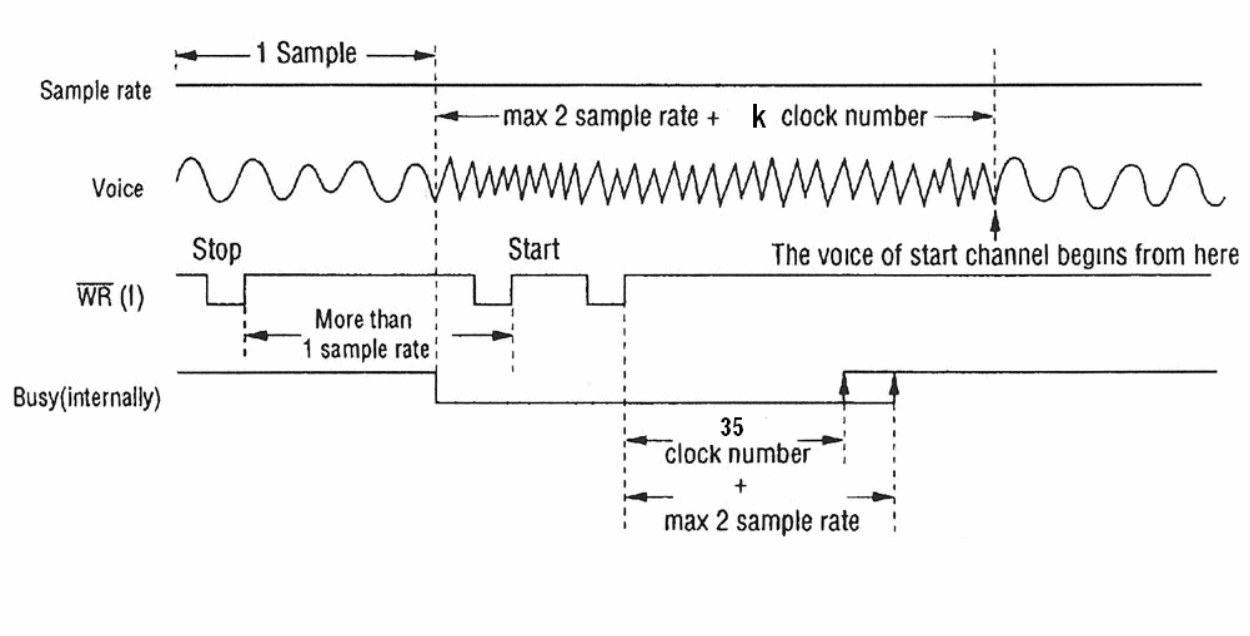


1 sample rate : R: 136 + $\overline{SS}$ x 34 clock number
L: (136 + $\overline{SS}$ x 34) x n clock number
n: 1 ,2 ,4 ,8

k = 238 + $\overline{SS}$ x 34

Start and Stop of Signal Channel

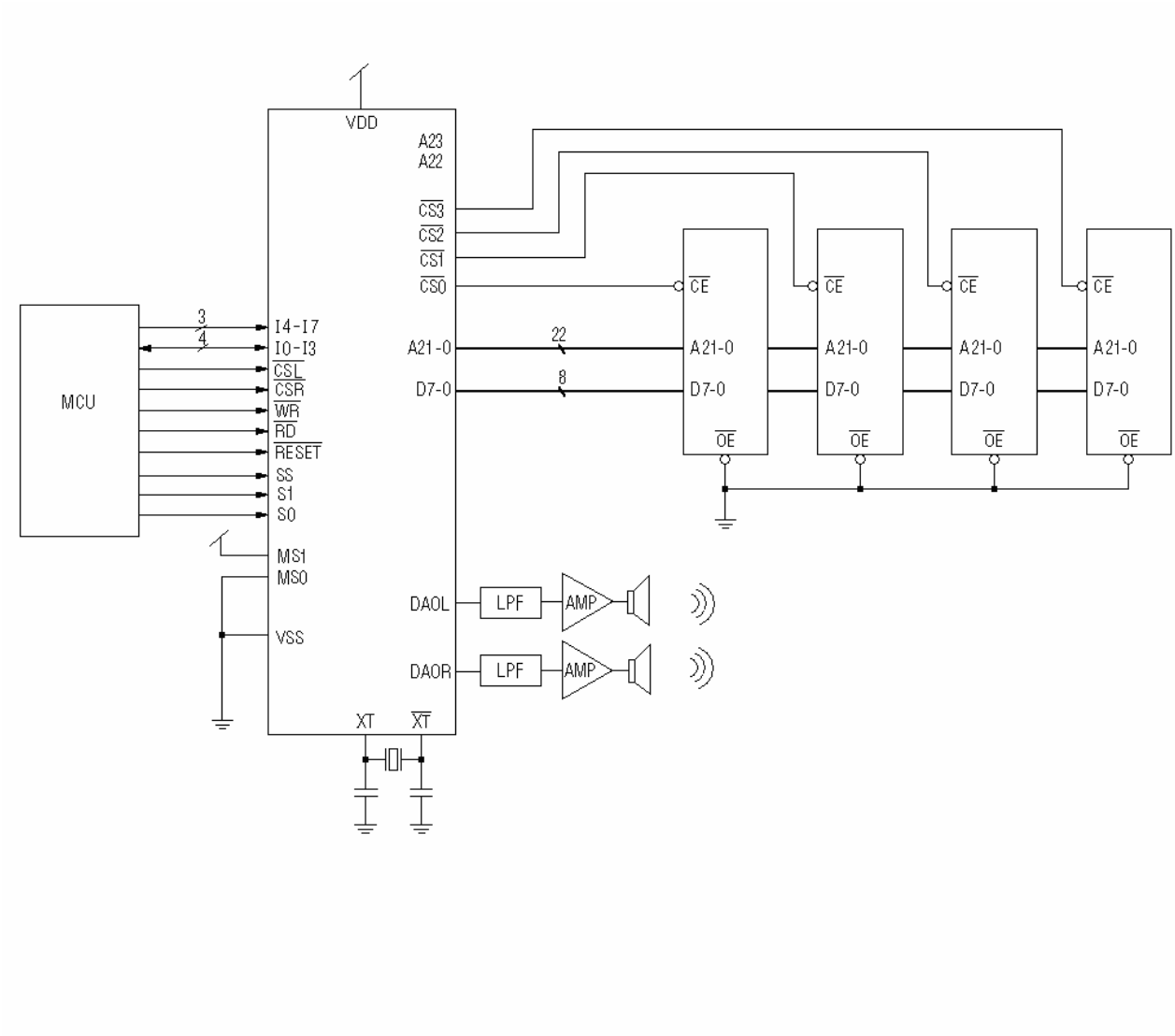
When a single channel (either of channels 1-4) starts again after it has stopped, the first write for start must be input with a delay of more than one sample rate from the stop write as shown in the figure above. When stop is entered, voice playback stops all the next sample and BUSY becomes "L" When start is entered again, voice is output after 238 + (the reverse of SS pin) x 34 clock from the second byte write. BUSY becomes "H" after 35 clock internally



Start and Stop in Plural Channels

When channels are operating, the first byte write for start must be input with a delay of more than one sample rate from stop writing. The channel where stop was input, stops at every sample. Voice off the channel where stop was again input is output after a maximum 2 samples +k clocks from the preceding sample point.
The BUSY signal becomes "H" state after the 35 clock + maximum 2 samples time.

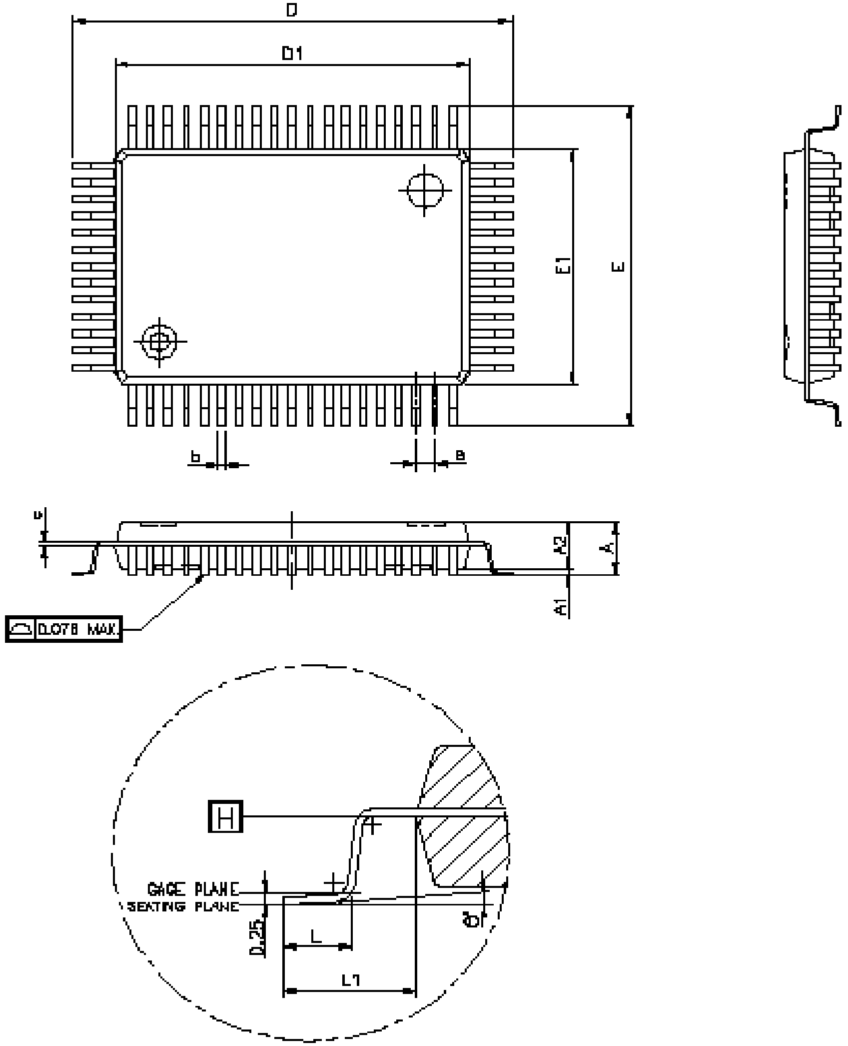
APPLICATION CIRCUIT



For 4M Byte ROM × 4 (MS0 = “0” , MS1 = “1”)

Reference Only

PACKAGE OUTLINE (64 pin QFP)

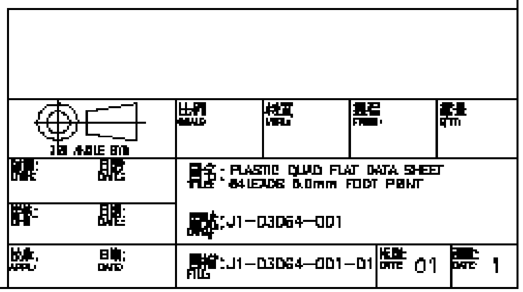


SYMBOLS	MIN.	NOM	MAX.
A	–	–	3.40
A1	0.25	–	–
A2	2.55	2.72	3.05
b	0.35	0.40	0.50
c	0.11	0.15	0.23
D	25.00 BASIC		
D1	20.00 BASIC		
e	1.00 BASIC		
E	19.00 BASIC		
E1	14.00 BASIC		
L	1.15	1.30	1.45
L1	2.50 REF		
θ°	0	3.5	7

UNIT : mm

NOTES:

1. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .



REVISE HISTORY

1. 2007/6/20 (V1.0)
-Original version

2. 2007/9/7 (V1.1)
-Fix page 4：
1.056MHz → 1.088MHz
2.112MHz → 2.176MHz
4.224MHz → 4.352MHz