

# TT6297/TT6298

## 4-CHANNEL ADPCM VOICE SYNTEHSIS LSI

### GENERAL DESCRIPTION

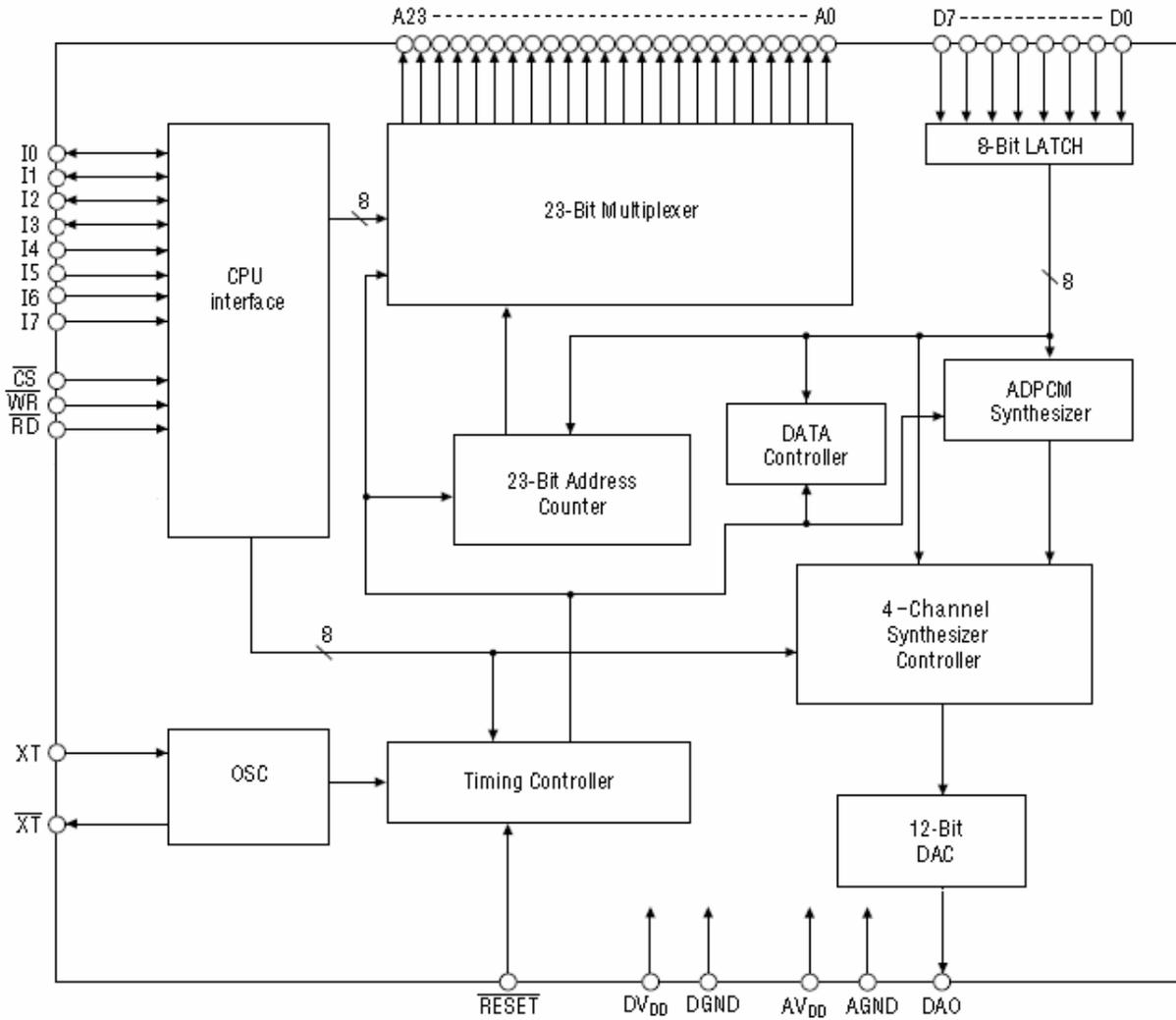
The TT6297/TT6298 is a 4-channel mixing ADPCM voice synthesis LSI which offers one sound outputs with 4 channels . The TT6297/TT6298 can access an external voice data ROM for sound effects or speech voice. The maximum external ROM size is 16M/8M \*8 bit and can direct access. The TT6297/TT6298 has an 4-channel synthesis stage which allows the simultaneous playback of four different channels. It is used to have a voice with BGM (Back Ground Music) effect, instrumental sound, echo effect etc.

### FEATURES

- Advance ADPCM algorithm
- Number of bits/sample: 4
- 24 address lines (TT6297), 23 address lines (TT6298)for external ROM
- 8-bit control bus for mode setting
- External memory capacity 128Mbit for TT6297/64Mbit for TT6298
- Interface with common CPU and MPU
- Clock frequency with Sampling frequency: (clock 1 MHz to 4 MHz)
  - At 1.088 MHz clock  
DAO : 8 kHz
  - At 2.176 MHz clock  
DAO : 16 kHz
  - At 4.352 MHz clock  
DAO : 32 kHz
- Number of words: 511 maximum
- Vocalization time:TT6297 :64 minutes maximum (at 8 kHz, sample rate)  
TT6298 :32 minutes maximum (at 8 kHz, sample rate)
- Sound output channel (DAO with 4 channels)
- Built-in DA converter: 12-bit
- DAO output format: A-class
- Voice level attenuation: 0dB~-24dB on each channel (9steps)  
with -3dB/step
- Advance low power CMOS process
- 5 V or 3.3 V single power supply
- 48-pin plastic SSOP

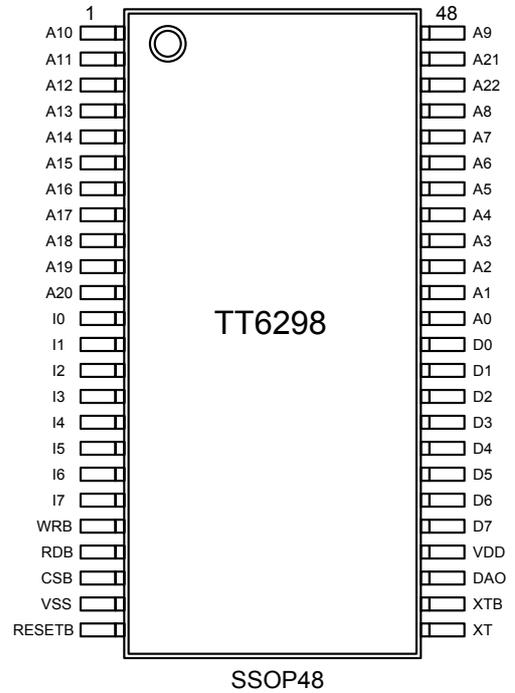
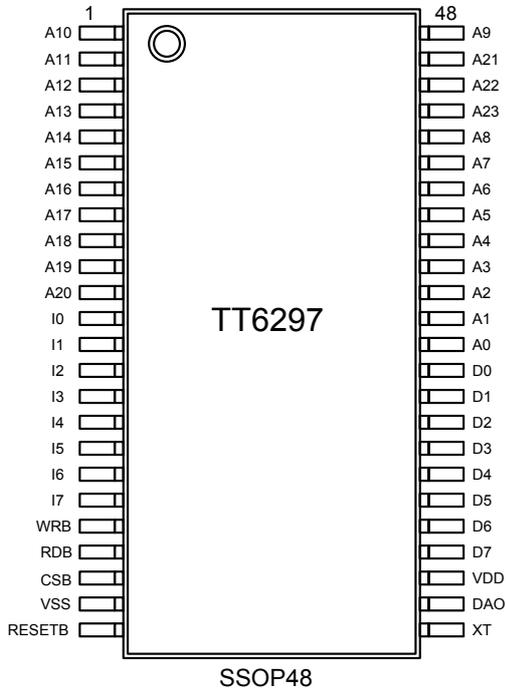
# TT6297/TT6298

## BLOCK DIAGRAM



# TT6297/TT6298

## PIN CONFIGURATION



TT6297 : for external clk input , 24 address lines (A0~A23)  
External memory capacity 128Mbit

TT6298 : for crystal osc , 23 address lines (A0~A22)  
External memory capacity 64Mbit

# TT6297/TT6298

## PIN DESCRIPTION

Pin Name	Pin NO TT6297	Pin NO TT6298	I/O	Function
I <sub>0</sub> ~I <sub>3</sub>	12~15	12~15	I/O	Instruction bus and condition outputs. These pins are inputs for phrase specification Maximum number of phrases is 511, I <sub>0</sub> ~I <sub>3</sub> pins are also outputs of the operating state- busy state, for channels 1~4 and are further used to select the channel attenuation rate.
I <sub>4</sub> ~I <sub>7</sub>	16~19	16~19	I	
WRB	20	20	I	Write enable input. Data is written on the data bus of I <sub>0</sub> ~I <sub>7</sub> The data is written when $\overline{WR}$ goes low.
RDB	21	21	I	Read enable input. The output busy state of channels 1~4 on the data bus of I <sub>0</sub> ~I <sub>3</sub> can be read using this input. A high level indicates busy.
CSB	22	22	I	Chip select input. Input "L" level either when $\overline{WR}$ signal is input or when $\overline{RD}$ signal is input.
RESETB	24	24	I	Reset input. Reset condition is available by inputting "L" level All functions are suspended during reset.
A <sub>0</sub> ~A <sub>23</sub> / A <sub>22</sub>	36~48 1~11	37~48 1~11	O	Address outputs. These pins are to address the external ROM in which voice data is stored. TT6297 : A <sub>0</sub> ~A <sub>23</sub> TT6298 : A <sub>0</sub> ~A <sub>22</sub>
D <sub>0</sub> ~D <sub>7</sub>	28~35	29~36	I	Voice data inputs.
DAO	26	27	O	Voice synthesis output. Voice synthesized analog signal is output from this pin.
XT	25	25	I	External clk input (Crystal oscillator pin.).
XTB	-	26	O	Crystal oscillator pin.
VDD	28	28	P	Power Supply pin.
VSS	23	23	P	Ground pin.

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## ELECTRICAL CHARACTERISTICS

### • Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	VDD	Ta=25°C	-0.3~+7.0	V
Input voltage	V <sub>IN</sub>	Ta=25°C	-0.3~VDD+0.3	V
Storage temperature	T <sub>stg</sub>	—	-55 ~ 150	°C

### • Recommended Operating Conditions

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	VDD	VSS=0V	2.9 ~ +5.5	V
Operating temperature	T <sub>op</sub>	VSS=0V	-40 ~ +85	°C
Oscillation frequency	f <sub>osc</sub>	VSS=0V	1~5	MHz

### • DC Characteristics

(Vdd = 2.9 ~ 5.5V, VSS=0V, Ta = -40 ~ 85°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
“L” input current	I <sub>IL</sub>	V <sub>IL</sub> =VSS	-10	—	—	μA
“H” input current	I <sub>IH</sub>	V <sub>IH</sub> =VDD	—	—	10	
“L” input voltage	V <sub>IL</sub>	—	—	—	0.2Vdd	V
“H” input voltage	V <sub>IH</sub>	—	0.8Vdd	—	—	
“L” output voltage	V <sub>OL</sub>	I <sub>LO</sub> =0.8mA	—	—	0.45	V
“H” output voltage	V <sub>OH</sub>	I <sub>OH</sub> =-40μA	Vdd	—	—	
Output leakage current	I <sub>LO</sub>	VSS ≤ V <sub>OUT</sub> ≤ V <sub>D</sub>	-10	—	10	μA
Operating current	I <sub>DD</sub>	f <sub>OSC</sub> =4.0MHz	—	5	10	mA
DA output relative error	V <sub>DAE</sub>	No load	—	—	20	mV
DA output impedance	R <sub>DAOUT</sub>	—	—	15	—	kΩ

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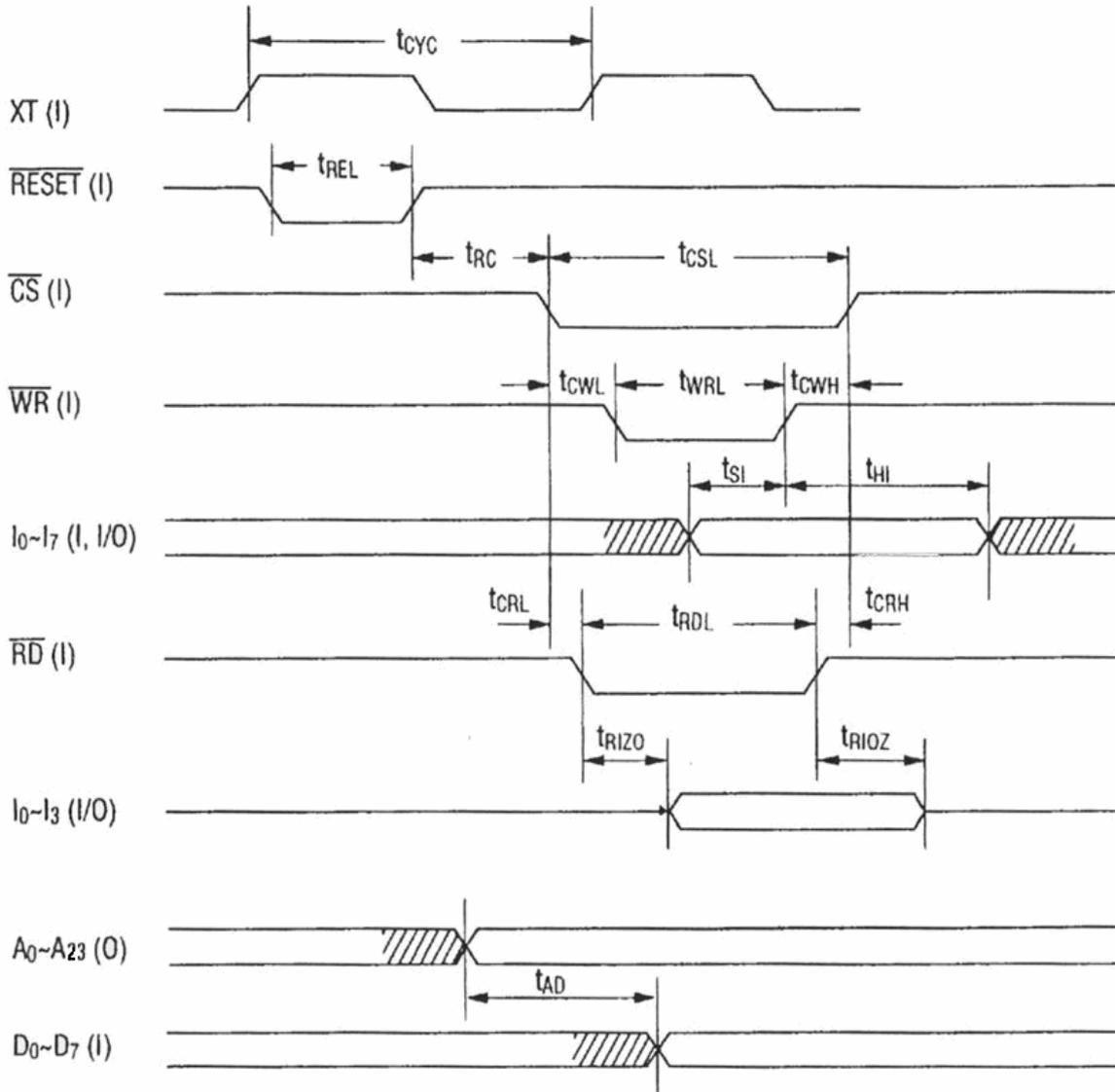
## • AC Characteristics

VDD = 4.5~5.5V, VSS=0V, Ta= -40 ~ +85°C)

Parameter	Symbol	Min.	Typ	Max.	Unit
Clock cycle	t <sub>CYC</sub>	200	-	-	ns
Clock duty cycle	f <sub>DUTY</sub>	40	50	60	%
$\overline{RESET}$ pulse width	t <sub>REL</sub>	100	-	-	ns
$\overline{CS}$ pulse width	t <sub>CSL</sub>	250	-	-	ns
$\overline{WR}$ pulse width	t <sub>WRL</sub>	200	-	-	ns
$\overline{RD}$ pulse width	t <sub>RDL</sub>	300	-	-	ns
$\overline{RESET}$ fall to $\overline{CS}$ fall	t <sub>RC</sub>	250	-	-	ns
$\overline{CS}$ fall to $\overline{WR}$ fall	t <sub>CWL</sub>	50	-	-	ns
$\overline{WR}$ raise to $\overline{CS}$ raise	t <sub>CWH</sub>	0	-	-	ns
Data set up time of I <sub>0</sub> -I <sub>7</sub> in respect to $\overline{WR}$ raise	t <sub>SI</sub>	80	-	-	ns
Data hold time of I <sub>0</sub> -I <sub>7</sub> in respect to $\overline{WR}$ raise	t <sub>HI</sub>	80	-	-	ns
$\overline{RD}$ fall to stable output of I <sub>0</sub> -I <sub>3</sub>	t <sub>RIZO</sub>	-	-	120	ns
$\overline{RD}$ raise to flow status output of I <sub>0</sub> -I <sub>3</sub>	t <sub>RIOZ</sub>	0	-	120	ns
$\overline{CS}$ fall to $\overline{RD}$ fall	t <sub>CRL</sub>	20	-	-	ns
$\overline{RD}$ raise to $\overline{CS}$ raise	t <sub>CRH</sub>	0	-	-	ns
Address stable (A <sub>0</sub> -A <sub>23</sub> ) to data input of D <sub>0</sub> -D <sub>7</sub>	t <sub>AD</sub>	-	-	5•t <sub>CYC</sub> +90	ns

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## TIMMING CHART



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## FUNCTION EXPLANATION

### 1. Phrase Selection

Phrase Selection Phrases are specified and read into the 2 byte data which consists of I<sub>0</sub>~ I<sub>7</sub> data bus. The phrase selection data is latched when WRB goes high while CSB is low .The format of the phrase specification input is as follows.

	I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>
1st Byte	1	Phrase selection data						
2nd Byte	<b>Phrase expansion II6,II7 &amp; Channel specification II4,II5</b>				Reduction specification II3~II0			

As shown in the above chart, I<sub>7</sub> of the first 1 data byte is always 1. I<sub>0</sub>~I<sub>6</sub> of the first data byte specifies the low phrase address and the I<sub>7</sub>,I<sub>6</sub> of second byte are used as high phrase address. The phrase selection data has a selection of 511 phrases which corresponds to 00000001~11111111. The phrase selection data is used for to A<sub>3</sub>~A<sub>11</sub> address outputs, and they specify both start and stop address which are stored in the external ROM.

### Relation between Phrase Selection Data and ROM Address

Phrase Selection Data		II <sub>7</sub>	II <sub>6</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	-	-	-
External ROM address	A <sub>23</sub> ~A <sub>10</sub>	A <sub>11</sub>	A <sub>10</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>
Selection Not valid	0~0	0	0	0	0	0	0	0	0	0	0	0	0
Phrase 1	0~0	0	0	0	0	0	0	0	0	1	0	0	0
Phrase 2	0~0	0	0	0	0	0	0	0	1	0	0	0	0
Phrase 3	0~0	0	0	0	0	0	0	0	1	1	0	0	0
Phrase 510	0~0	1	1	1	1	1	1	1	1	0	0	0	0
Phrase 511	0~0	1	1	1	1	1	1	1	1	1			

\* Phrases can not be specified with all inputs = "0"

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The second byte of data specifies the high phrase address, the synthesis operating channel as well as specific channel reduction of the synthesized play-back. The channel selection format is shown below. It is not possible to specify multiple channels at the same time.

## Phrase expansion bits

The data bits I17 & I16 of second byte and the data bits I6~I0 of first byte will Combine as the total phrase address A11~A3.

## Channel Specification

Channel	I15	I14
1	0	0
2	0	1
3	1	0
4	1	1

## Reduction Specification

All zero is considered as 0 dB of the relative sound itself. The reduction is made through 9 levels from about 0 dB to - 24 dB with the steps of about - 3 dB. Reduction format is shown below.

## Reduction Selection

Attenuation level	I3	I2	I1	I0
0dB	0	0	0	0
-3.2 dB	0	0	0	1
-6.0 dB	0	0	1	0
-9.2 dB	0	0	1	0
-12.0dB	0	1	0	0
-14.5dB	0	1	0	1
-18.0dB	0	1	1	0
-20.5dB	0	1	1	1
-24.0dB	1	0	0	0

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## 2. Voice Synthesis Channel Suspension

Voice synthesis operation of any channel can be suspended. Channel suspension is controlled by bits  $I_3 \sim I_6$  of data bytes  $I_0 \sim I_07$ . To suspend a channel, make  $I_7=0$ , while  $I_3 \sim I_6$  represent the channels which should be suspended. Channel suspension occurs even if multiple channels are selected. For example, if  $I_3 \sim I_6$  are all 1 and  $I_7=0$ , then channels 1~4 are suspended simultaneously.

Suspended channel	$I_7$	$I_6$	$I_5$	$I_4$	$I_3$	$I_2$	$I_1$	$I_0$
1	0	0	0	0	1	×	×	×
2	0	0	0	1	0	×	×	×
3	0	0	1	0	0	×	×	×
4	0	1	0	0	0	×	×	×

## 3 .Data ROM

### 1) ADDRESS DATA

This specifies start and stop address of ADPCM speech data. One phrase start and end address consists of 8 bytes. The first 3 bytes show start address while the last 3 bytes show stop address. The other 2 bytes are empty. By selecting the first address in which the start address is stored, the selected speech data is played back.

Address 0	SA <sub>1</sub>
Address 1	SA <sub>2</sub>
Address 2	SA <sub>3</sub>
Address 3	EA <sub>1</sub>
Address 4	EA <sub>2</sub>
Address 5	EA <sub>3</sub>
Address 6	EMPTY
Address 7	EMPTY

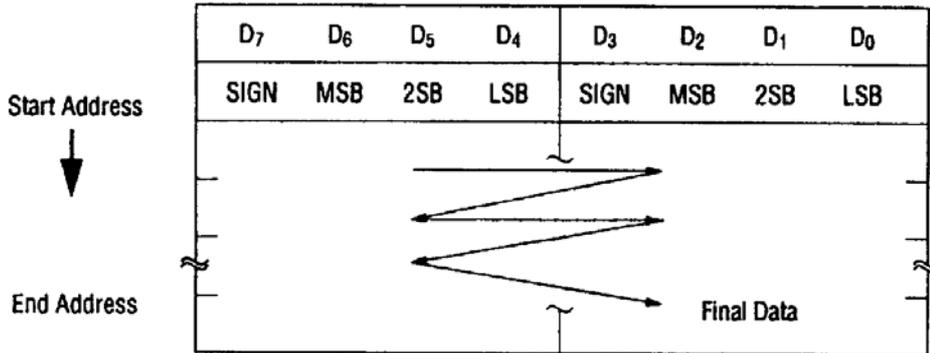
Start addresses (SA<sub>1</sub>~SA<sub>3</sub>) and stop addresses (EA<sub>1</sub>~EA<sub>3</sub>) are stored according to the chart shown below

	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
SA <sub>1</sub> / EA <sub>1</sub>	<b>A23</b>	<b>A22</b>	<b>A21</b>	<b>A20</b>	<b>A19</b>	<b>A18</b>	A <sub>17</sub>	A <sub>16</sub>
SA <sub>2</sub> / EA <sub>2</sub>	A <sub>15</sub>	A <sub>14</sub>	A <sub>13</sub>	A <sub>11</sub>	A <sub>10</sub>	A <sub>15</sub>	A <sub>9</sub>	A <sub>8</sub>
SA <sub>3</sub> / EA <sub>3</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>15</sub>	A <sub>1</sub>	A <sub>0</sub>

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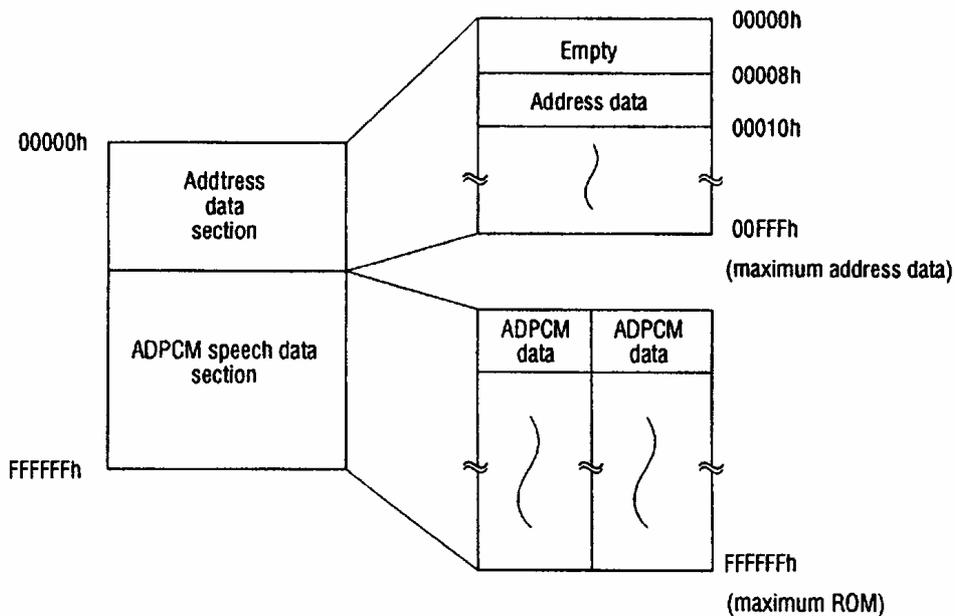
## 2) ADPCM SPEECH DATA

ADPCM speech data consists of 4-bit samples. So, 1 byte stores 2 samples. The data arrangement proceeds from higher rank bits (D<sub>4</sub>~D<sub>7</sub>) to lower rank bits (D<sub>0</sub>~D<sub>3</sub>). The storage of speech data should always be ended with the lower rank bit, So, always store an even number of samples, Speech data is produced by Speech Development Tool TT6297/TT6298.



## 3) DATA ROM STRUCTURE

When 1 phrase is selected, address data is written from ROM address 00008h to 0000Fh, When the maximum 511 phrases are selected in address data section, the data is written up to ROM address 00FFFh. and the rest is used as the ADPCM data section. The following chart shows the memory map of the source data ROM.

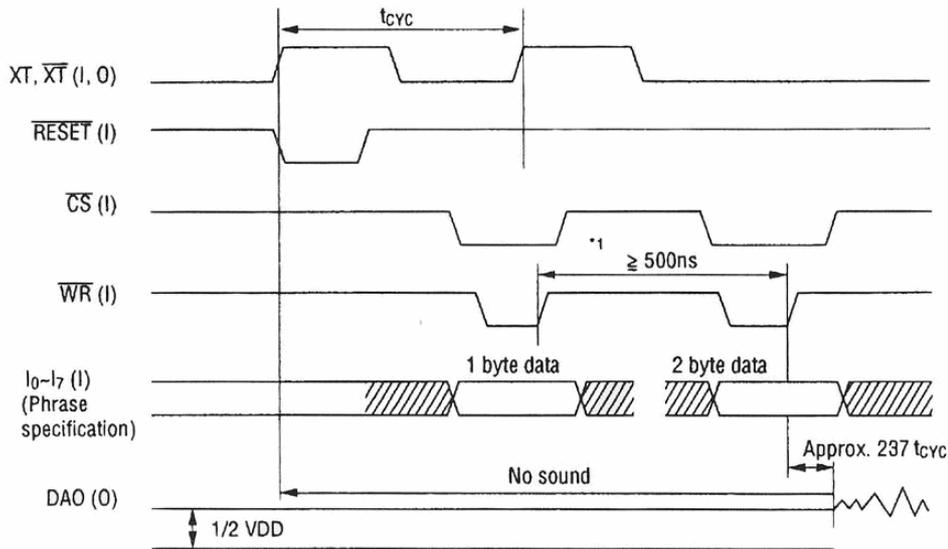


# TT6297/TT6298

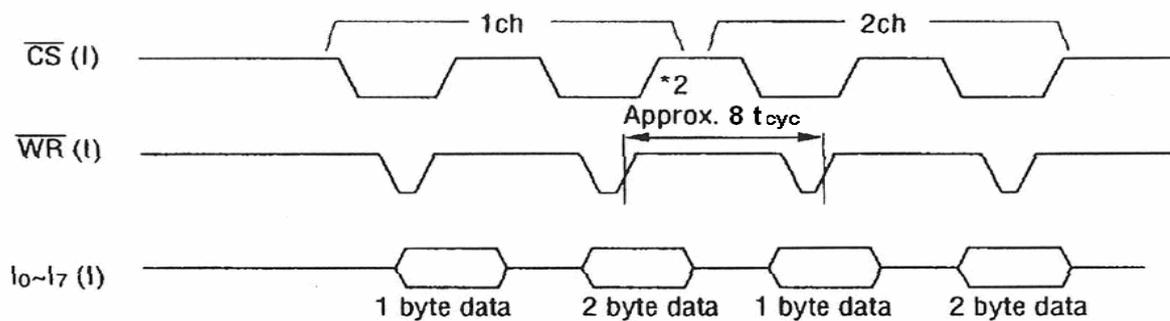
## FUNCTIONAL DESCRIPTION

### 1. Phrase Selection Input

This procedure is to input phrase selection data onto the data bus inputs I<sub>0</sub>~I<sub>7</sub>. The data is latched internally when  $\overline{WR}$  rises from "L" to "H", while CSB remains "L". Voice synthesis operation does not start till the second byte is fully latched



Note : Phrase selection is from channel 1 to channel 8 continuously  
 If all of CH1~CH4 CMM are latched, then the DAO output Arrox.. 420  $t_{cyc}$ .  
 \*1 An interval of 75  $T_{CYC}$  (max.) is needed between phrases

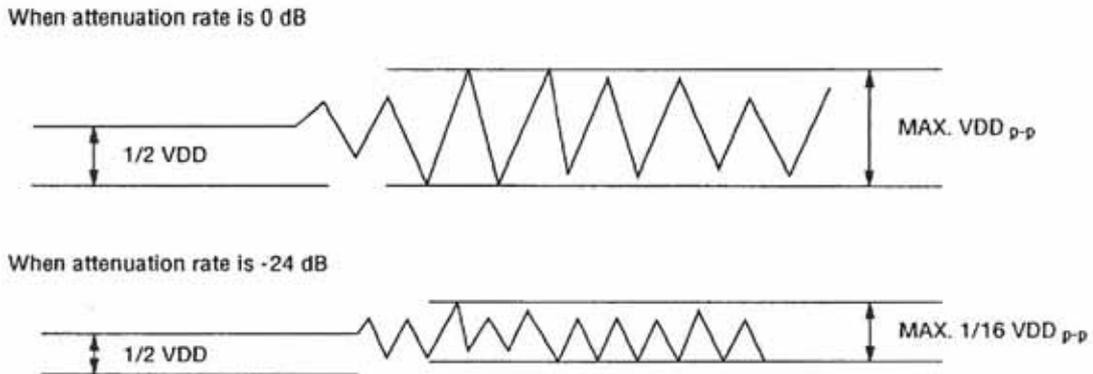


Note\*2 Oscillation frequency = 1.088 MHz SS = "L"

Voice synthesis playback can be started from any channel, 1 to 8. The arrangement of each channel can be in any order. The second byte of the phrase selection data contains the phrase attenuation data in bits D<sub>0</sub> - D<sub>3</sub>. Synthesized data is attenuated in -3 dB steps from 0 dB to -24 dB.

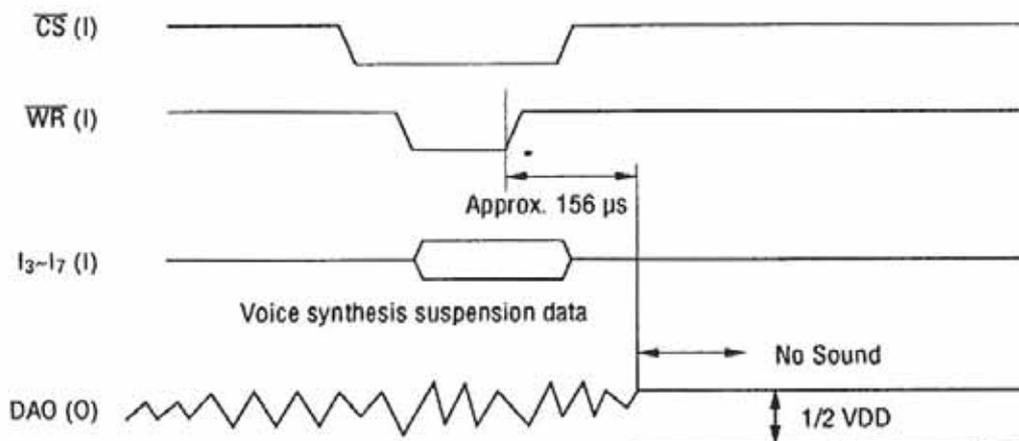
# TT6297/TT6298

## 2. Attenuation of Synthesized Speech



## 3. Speech Synthesis Channel Suspension

This is accomplished by writing the synthesis channel suspension data onto data bus inputs I<sub>3</sub>~I<sub>7</sub>. The data is latched internally when  $\overline{WR}$  goes from "L" to "H" while CSB remains active (L). Since synthesis suspension data is 1 byte data, synthesis operation is suspended right after the rising edge of  $\overline{WR}$ . Multiple channels can be specified, making it possible to suspend channels 1~4 simultaneously.

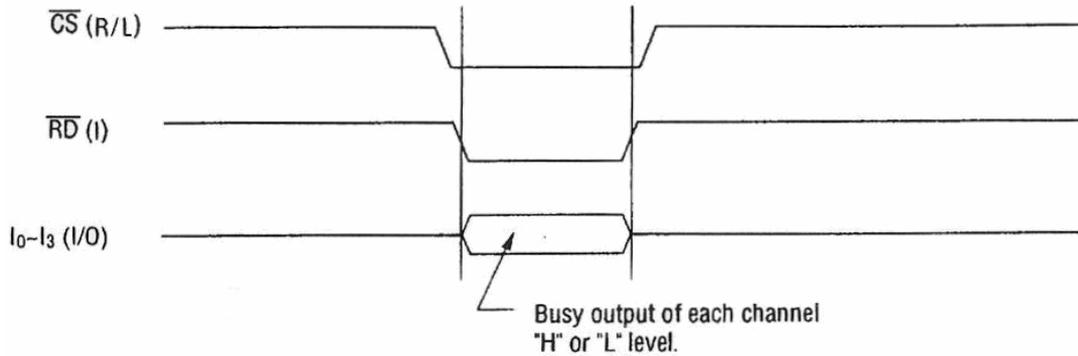


**Note: \* Oscillation frequency = 1.088 MHz SS= "L"**

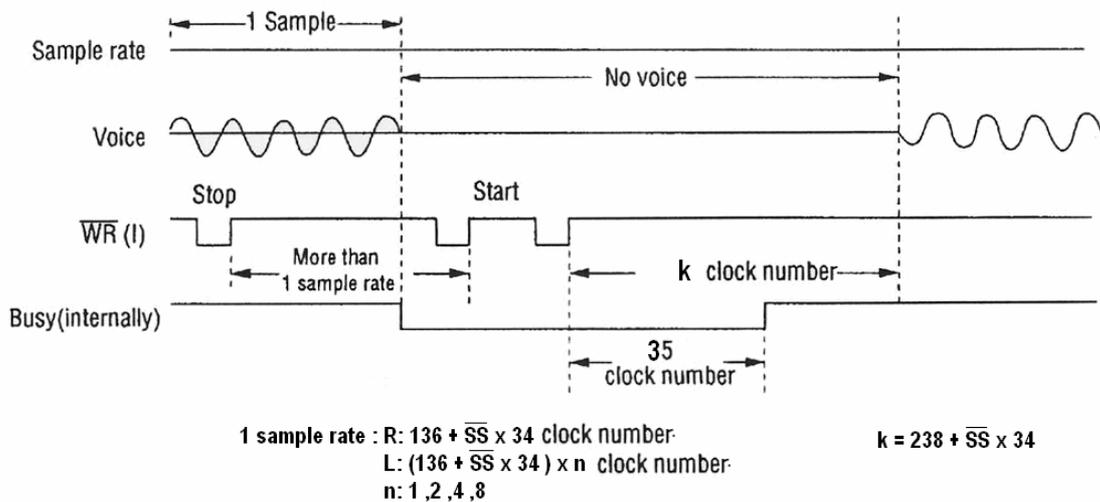
# TT6297/TT6298

## 4. Reading the Busy Status

While CSB is "L" and  $\overline{RD}$  is "L", each operation state, the busy state of channels 1~4 is output on  $I_0\sim I_3$ . "H" is output during synthesized playback.



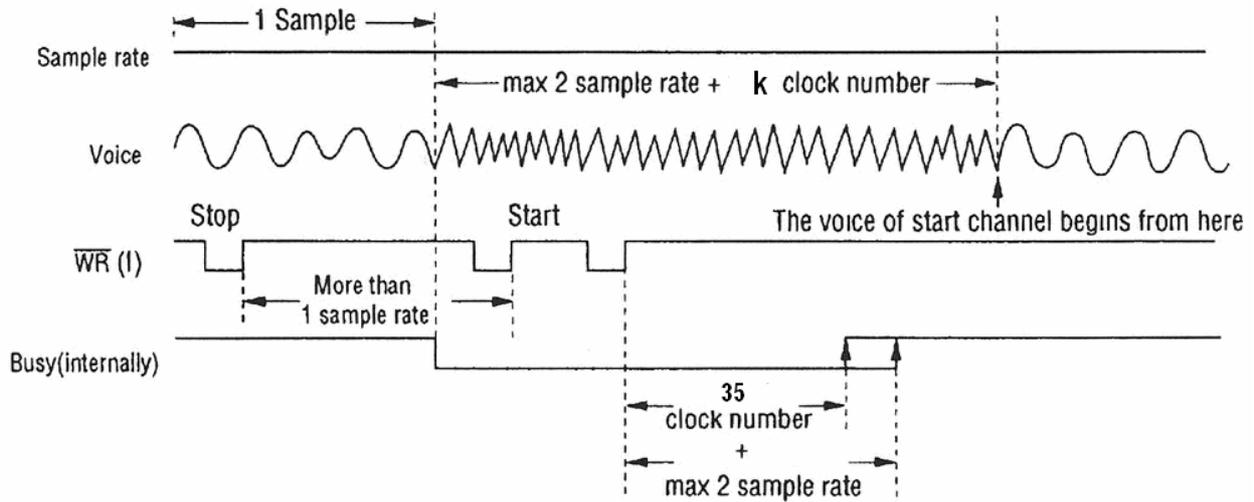
## 5. Start and Stop of 1 Channel



### Start and Stop of Signal Channel

When a single channel (either of channels 1-4) starts again after it has stopped, the first write for start must be input with a delay of more than one sample rate from the stop write as shown in the figure above. When stop is entered, voice playback stops all the next sample and BUSY becomes "L". When start is entered again, voice is output after  $238 + (\text{the reverse of SS pin}) \times 34$  clock from the second byte write. BUSY becomes "H" after 35 clock internally.

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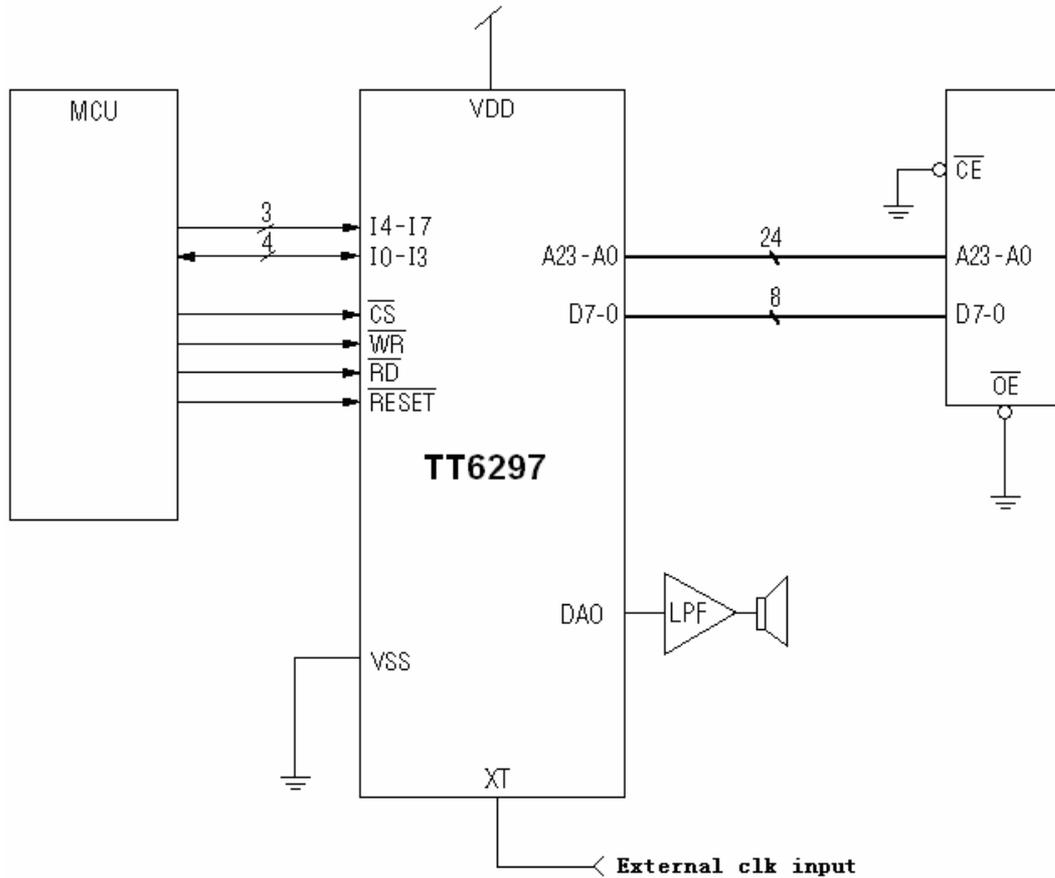


## Start and Stop in Plural Channels

When channels are operating, the first byte write for start must be input with a delay of more than one sample rate from stop writing. The channel where stop was input, stops at every sample. Voice off the channel where stop was again input is output after a maximum 2 samples +k clocks from the preceding sample point. The BUSY signal becomes "H" state after the 35 clock + maximum 2 samples time.

# TT6297/TT6298

## APPLICATION CIRCUIT FOR TT6297

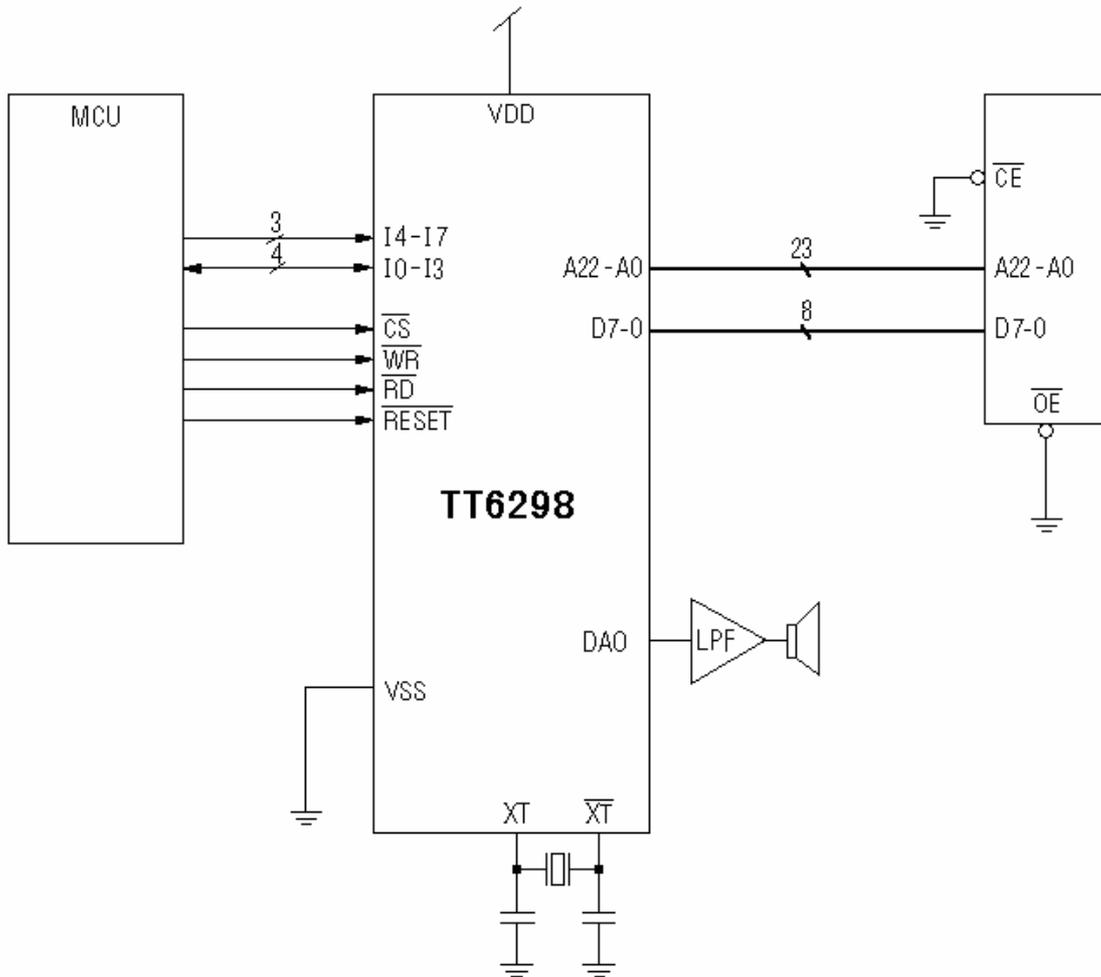


TT6297 : for external clk input , 24 address lines (A0~A23)  
External memory capacity 128Mbit

**Reference Only**

# TT6297/TT6298

## APPLICATION CIRCUIT FOR TT6298



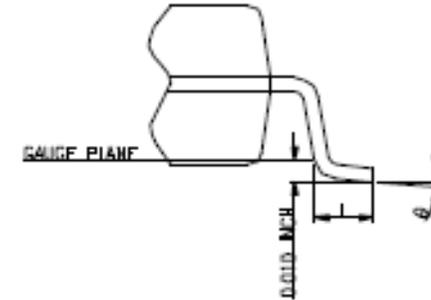
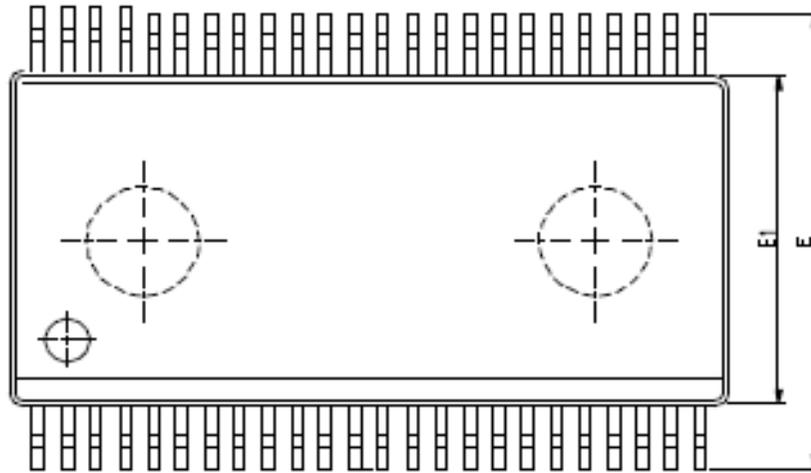
TT6298 : for crystal osc , 23 address lines (A0~A22)  
External memory capacity 64Mbit

**Reference Only**

# TT6297/TT6298

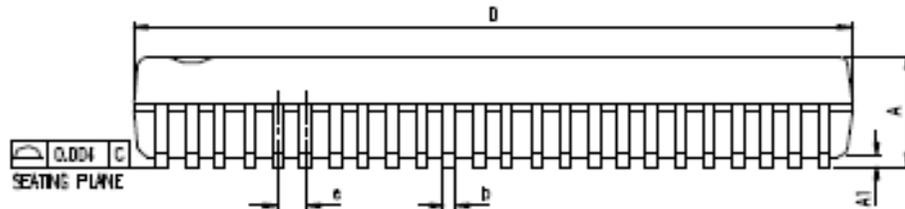
(48 pin SSOP)

REV.	DESCRIPTION	BY	DATE
ORIG.	DRAWING ISSUE	SANDY CHEN	97.11.04
A	MODIFY E-PIN	SANDY CHEN	97.12.06
B	ADD NOTES	SANDY CHEN	00.01.19



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.413	2.581	2.794	0.095	0.102	0.110
A1	0.203	0.305	0.406	0.008	0.012	0.016
b	0.203		0.343	0.008		0.0135
e	0.127		0.254	0.005		0.010
e	0.035 BASIC			0.025 BASIC		
E	10.033		10.668	0.395		0.420
E1	7.391	7.493	7.595	0.291	0.295	0.299
h	0.381		0.635	0.015		0.025
L	0.508		1.016	0.020		0.040
Ø	0		Ø	0		Ø

N	D DIMENSION (IN INCH)			JEDEC
48	0.620	0.625	0.630	MO-118 (AA)
56	0.720	0.725	0.730	MO-118 (AB)



▲ NOTES : DIMENSION " D " DONE NOT INCLUDE MOLD FLASH,  
 PROTRUSIONS OR GATE BURRS.  
 MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL  
 NOT EXCEED 0.006 INCH ( 0.1524 MM ) PER SIDE.

TITLE	SSOP OUTLINE PACKAGE BODY WIDTH 300 MIL	UNIT	INCH	QTY	
DESIGNED	SANDY CHEN 97.11.04	FILE NAME	P3P048P1		
CHECKED	C.C. CHO 00.01.26	DWG. NO.:	CW-P3-001C		
APPROVED	C.C. CHO 00.01.26				

## REVISE HISTORY

1. 2007/6/20 (V1.0)  
-Original version