TTP252 Target Spec.

§ PATENTED

1. PATENT：『電流源控制及補償觸控電容感測方法及其裝置』
   PAT NO. I339356 (Taiwan)
   PAT NO. ZL 2007 1 0202087. 0 (CHINA)
2. PATENT：『具環境變化校正的電容式觸控感測裝置』
   PAT NO. M383780 (Taiwan)
   PAT NO. ZL 2010 2 0141537. 7 (CHINA)
3. PATENT：『省電型多鍵觸摸開關感測裝置』
   PAT NO. M375250 (Taiwan)
   PAT NO. ZL 2010 2 0302392. 4 (CHINA)

§ General Description:

TTP252 MCU is an easy-used 4-bit CPU base microcontroller. It contains 1984-word ROM、96-nibble RAM、timer/Counter、timer/PWM、interrupt service 、IO control hardware、LVR、touch pad and LDO feature for specified applications. The device is also suitable for diverse simple applications in control appliance and consumer product.

§ Features:

1. Tontek RISC 4-bit CPU core
2. Total 26 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
4. advance CMOS process
5. Working memory with 1984*16 program ROM and 96*4 SRAM
6. 2-level stacks
7. Operating voltage: 2.0V~5.5V
8. System operating frequency: (at VDD=5V)
   . High speed system oscillator (OSCH):
   - ✧ Built-in RC oscillator: 4MHz(typical)

   .Low speed peripheral oscillator (OSCL):
   - ✧ Built-in RC oscillator: 16KHz(typical)
9. Offer 8 IO+8 touch pad or 16 general programmable I/O
   - ✧ IO port built-in key wake-up feature enable by software setting
   - ✧ Providing external interrupt inputs and Timer clock inputs
   - ✧ Offering internal signal outputs, like buzzer(PFD)
10. One 8-bit auto-reload timer/counter & one 8-bit timer/PWM & one time

base counter

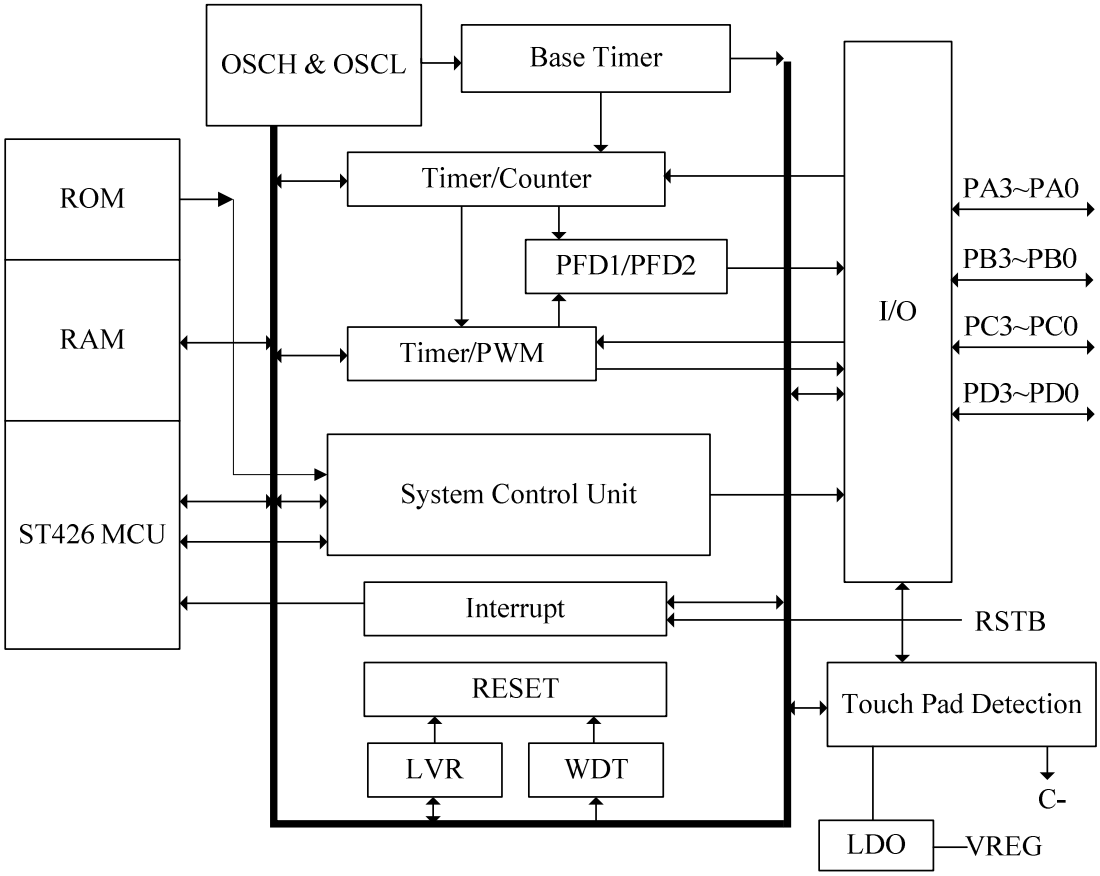
- ✧ 4 timer clock sources(internal & external) selected by software
- ✧ Timer provides the PFD feature for Buzzer output driver
- ✧ Time base offers 2 various period interrupt request

11. MCU system protection and power saving controlled mode:
    - ✧ Built-in watch dog timer (WDT) circuit
    - ✧ ROM code error detection
    - ✧ Out of user program's range detection
    - ✧ Providing high/low system operating speed、sleep、stop mode for power saving control
    - ✧ Built-in low voltage reset (LVR) function
12. 8 pins with touch pad detection
13. LDO voltage can select 2.7V or 4.2V output by option.
14. LVR voltage can select 2.2V or 3.0V by option.
15. Provides 8 interrupt sources
    - ✧ External: INT0 , INT1 shared with IO pad
    - ✧ Internal: Timer/counter, Timer/PWM, two Time base timer
    - ✧ Two touchpad's interrupt
16. Provide package types
    - ✧ DIP/SOP 8 pins, DIP/SOP/SSOP/QFN 16/20/24 pins, TSSOP 20pins
    - ✧ Dice available

§ Applications:

1. Household electric appliances
2. Consumer products
3. Measurement controller

§ Block Diagram:



§ Pin Description:

Pin Name	Share Pin	I/O	Pin no.	Mask Option	Pin Description
V_{DD}	-	Power	+1	-	Positive power supply
V_{SS}	-	Power	+1	-	Negative power supply, ground
RSTB	-	I	+1	-	External reset input, active low, 50kΩ pull-up(V_{DD} =5v)
PA0(INT0) PA1(TCP1I) PA2(PFD1) PA3(PFD2/PWM)		IO IO IO IO	+4	-	I/O port with external interrupt input (PA0). PA1 is used as clock inputs of timer/counter1. PA2 is shared with internal PFD1 output. PA3 is shared with internal PFD2 or PWM output.
PB0 PB1(TCP2I) PB2 PB3	-	IO IO IO IO	+4	-	I/O port with internal signal output. PB1 is used as clock inputs of timer/PWM .
PC0(VPP) PC1 PC2(INT1) PC3(PWM/PFD2/PFD1/INT0)	TP0 TP1 TP2 TP3	I IO/I IO/I IO/I	+4	PC/TP	IO port or touch pad input. PC2 is shared with external interrupt input. PC3 is shared with external interrupt input and PFD1/PFD2/PWM output.
PD0(PWM/PFD2/PFD1/INT1) PD1 PD2 PD3	TP4 TP5 TP6 TP7	IO/I IO/I IO/I IO/I	+4	PD/TP	IO port or touch pad input. PD0 is shared with external interrupt input and PFD1/PFD2/PWM output.
C-	-	O	+1	-	Touch signal output with pull up R
VREG	-	Power	+1	-	LDO output
			21		

* If PC3 select INT0 option, and PA0's INT0 will be disable. If PC3's option don't select INT0 , and PA0 have INT0 function.
* If PD0 select INT1 option, and PC2's INT1 will be disable. If PD0's option don't select INT1 , and PC2 have INT1 function.
* If PC3 or PD0 select PFD1, it will disable PA2's PFD1 function. PC3's PFD1 function and PD0's PFD1 function can be enable in same time.
* If PC3 or PD0 select PWM/PFD2, it will disable PA3's PWM/PFD2 function. PC3's PWM/PFD2 function and PD0's PWM/PFD2 function can be enable at same time.

§ IO Cell type Description:

Pin Name	I/O Type	Description
PA0~PA1	Figure IO-A	STD IO with external input
PA2~PA3	Figure IO-B	STD IO with internal output
PB0	Figure IO-C	STD IO
PB1	Figure IO-A	STD IO with external input
PB2~PB3	Figure IO-C	STD IO
PC0	Figure IO-E	Input Port
PC1	Figure IO-C	STD IO
PC2	Figure IO-A	STD IO with external input
PC3,PD0	Figure IO-D	STD IO with internal output & external input
PD0~PD3	Figure IO-A	STD IO with external input

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-40℃ ~ +85℃	℃
Storage Temperature	Tst	-50℃ ~ +125℃	℃
Supply Voltage	VDD	VSS-0.3 ~ VSS+6.0	V
OTP Supply Voltage	VPP	VSS-0.3 ~ VSS+12.5	V
Input Voltage	Vin	VSS -0.3 ~ VDD+0.3	V
Human Body Mode	ESD	>=5	KV

Note: VSS symbolizes for system ground

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	F_{OSCH}=4MHz (LVR OFF) (LVR ON)	2.0 2.0 2.2	- - -	5.5 5.5 5.5	V
Operating Current (Normal Mode CPU working, I/O no load)	I_{nd1}	VDD=5.0V, no load, F_{OSCH}=4MHz,	-	1.5	2.0	mA
	I_{nd2}	VDD=5.0V, no load, F_{OSCL} on	-	30	50	uA
Operating Current (Sleep Mode, CPU stop, I/O no load)	I_{sd1}	VDD=5.0V, no load, F_{OSCH}=4MHz,	-	1.5	2.0	mA
	I_{sd2}	VDD=3.0V, no load, F_{OSCL} on	-	5	10	uA
Standby Current	Istb	I/O no load, F_{OSCH} & F_{OSCL} stop	-	-	1.0	uA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	V_{DD}
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	V_{DD}
RSTB & INT	V_{IL}	Input Low Voltage	0	-	0.3	V_{DD}
RSTB & INT	V_{IH}	Input High Voltage	0.7	-	1.0	V_{DD}
Output port Sink Current	I_{OL}	VDD=5.0V, V_{OL}=0.6V	-	8	-	mA
Output Port Source Current	I_{OH}	VDD=5V, V_{OH}=VDD-0.7V	-	-4	-	mA
I/O Port Pull-High Resistor	R_{PH}	VDD=5.0V	100	150	200	KΩ
RSTB Pull-High Resistor	R_{PH}	VDD=5.0V	30	50	80	KΩ
Low Voltage Reset (LVR)	V_{LVR1}	-	2.0	2.2	2.4	V
	V_{LVR2}	-	2.7	3.0	3.3	V

§ AC Characteristics:

Parameter	Test Condition		Min	Typ	Max	Unit
External Reset	Low active pulse width t_{RES}		2	-	-	CPU clock
Interrupt input	Low active pulse width t_{INT}		2	-	-	
Wake up input	Low active pulse width t_{wkup}, Application de-bounce should be manipulated by user' software		2	-	-	OSCL
System Oscillator Frequency	F_{OSCH} (Built-in RC)	VDD=5.0V	-	4M	-	Hz
Peripheral Oscillator Frequency	Built-in F_{OSCL}(RC)	VDD=2.0~5.0V	12K	**16K**	21K	Hz
Startup Period of Oscillators	T_{OSCH} (Built-in RC)	wake-up from off mode	8	-	-	F_{OSCH}
	T_{OSCL} (Built-in RC)	Wake-up from off mode	8	-	-	F_{OSCL}
Stable Time Of System Clock Switching	T_{OSCH} (Built-in RC)	OSCL→OSCH & OSCH off	8	-	-	F_{OSCH}
	(If H/L=0 then OSCH stop)					
	T_{OSCL} (Built-in RC)	OSCH→OSCL & OSCL on	8	-	-	F_{OSCL}
Timer/Counter input clock frequency	Input frequency rating, no de-bounce circuit built-in ,at VDD=5V		DC	-	4M	Hz
System Stable Time after Power up	After power up, the system needs to initialize the configured state and OST.		-	-	40	ms

§ Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~$7BF_H$	-	Program ROM [1984*16]
-	000_H ~007_H	File Registers
-	008_H~$01F_H$	Peripheral registers (I)
-	020_H~$07F_H$	Working RAM [96*4]
-	200_H~$30F_H$	Peripheral registers (II)

§ Interrupt Vectors:

Interrupt Vectors	Function Description
$000	hardware RESET
$001	Hardware IRQ

§ File registers:

Address	Symbol	R/W	Default	Description
000_H	(DP1)	R/W	-	Indirect addressing register
001_H	ACC	R/W	-	Accumulator & Read Table 1st data
002_H	TB1	R/W	-	Read Table 2nd data
003_H	TB2	R/W	-	Read Table 3rd data
004_H	TB3	R/W	-	Read Table 4th data
005_H	DPL	R/W	-	Data Pointer low nibble
006_H	DPM	R/W	-	Data Pointer middle nibble
007_H	DPH	R/W	-	Data Pointer high nibble

§ Peripheral registers: Interrupt request flag register

Address	Symbol	R/W	Default	Description
008_H	PS	R/W	1100	CPU power saving control register
009_H	PSP	R/W	0000	Peripheral power saving control register
$00A_H$	INTC	R/W	0000	Interrupt enable control register
$00B_H$	INTF	R/W	0000	Interrupt request flag register
$00C_H$	INTC1	R/W	0000	Extended interrupt enable register
$00D_H$	INTF1	R/W	0000	Extended interrupt request flag register
$00E_H$	-	-	-	-
$00F_H$	-	-	-	-
010_H	-	-	-	-
011_H	-	-	-	-
012_H	PAC	R/W	1111	I/O port A control register
013_H	PA	R/W	1111	I/O port A data register
014_H	PBC	R/W	1111	I/O port B control register
015_H	PB	R/W	1111	I/O port B data register
016_H	PCC	R/W	1111	I/O port C control register
017_H	PC	R/W	1111	I/O port C data register
018_H	PDC	R/W	1111	I/O port D control register
019_H	PD	R/W	1111	I/O port D data register
$01A_H$				
$01B_H$	-	-	-	-
$01C_H$	-	-	-	-
$01D_H$	-	-	-	-
$01E_H$				
$01F_H$				

200_H	TCP1C	R/W	0000	Timer/counter 1 control register
201_H	TCP1L	R/W	xxxx	Timer/counter 1 data low register
202_H	TCP1H	R/W	xxxx	Timer/counter 1 data high register
203_H	TCP2C	R/W	0000	Timer/counter 2 control register
204_H	TCP2L	R/W	xxxx	Timer/counter 2 data low register
205_H	TCP2H	R/W	xxxx	Timer/counter 2 data high register
206_H	PAI	R	----	Port A pad data reading address
207_H	PBI	R	----	Port B pad data reading address
208_H	PCI	R	----	Port C pad data reading address
209_H	PDI	R	----	Port D pad data reading address
$20A_H$	-	-	-	-
$20B_H$	-	-	-	-
$20C_H$	TCPFS	R/W	0000	TCP clock source FS pre-scale register
$20D_H$	TBC	R/W	1111	Time base control register
$20E_H$				
$20F_H$				
210_H				
211_H				
212_H				
213_H				
214_H	-	-	-	-
215_H	-	-	-	-
216_H	-	-	-	-
217_H	-	-	-	-
218_H	LDO flag	R/W	0000	LDO fail flag address
219_H	CPUFS	R/W	0000	CPU freq. select.
$21A_H$	-	-	-	-
300_H	RESETF	R/W	0000	Reset flag
301_H	TBRB	W	xxxx	Time base counter clear address
302_H	MRO	W	xxxx	Reserved for testing

Note: a. Default means initial value after power on or reset.

b. R is “read” only, W is “write” only, R/W is both of “read” & “write”.

§ System function description:

S-1: System Oscillator

The high speed oscillator is operated in built-in RC mode. Built-in RC oscillator is fixed 4MHz

S-2: Peripheral Oscillator

The low speed oscillator was built-in an internal RC oscillator that is for low power consumption consideration and fixed peripheral device timing control. Built-in RC oscillator and the frequency range between 12 KHz ~ 21 KHz.

S-3: CPU clock

The CPU clock comes from system/peripheral oscillator which was controlled by H/L bit in PS register. In the normal operation, the system clock comes from high speed system oscillator (OSCH/N/2). N is define by CPUFS register. The low speed operation frequency (OSCL/2) comes from RC oscillator was selected by mask option.

✧ CPUFS (ADDRESS : 219H) : CPU frequency division's register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	--	--	CS1	CS0	0000B
Read/Write	--	--	R/W	R/W	

CS1~CS0: the selector value of CPU division's register

CS1 ~ CS0	CPU frequency	RC=4MHz
0	OSCH/1	4MHz
1	OSCH/2	2MHz
2	OSCH/4	1MHz
3	OSCH/8	500KHz

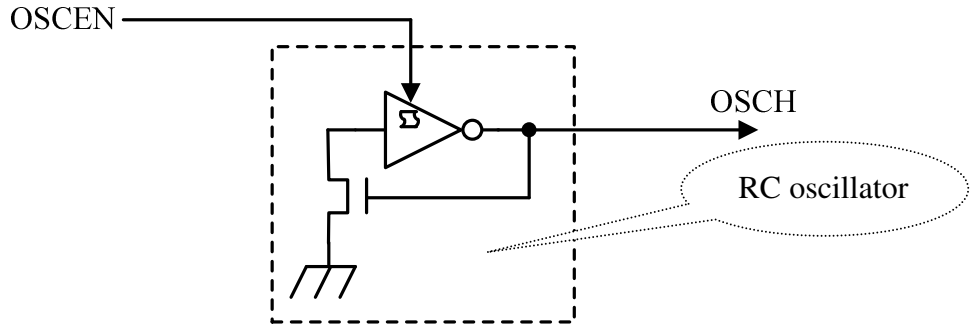


Figure: System High Speed Oscillator

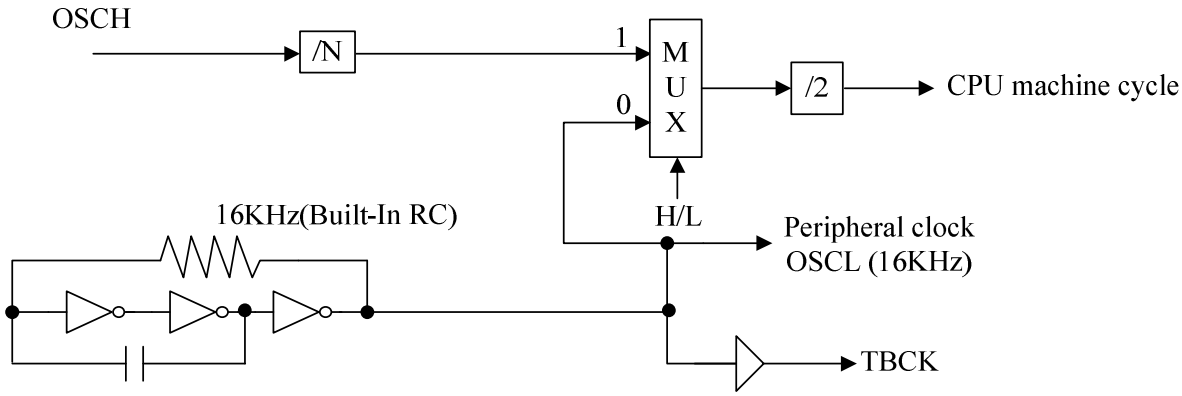


Figure: System Oscillator & CPU Clock Sources

Note:

If oscillator stable time < system OST, CPU will get abnormal.

S-4: Power saving mode (Stop mode & Sleep mode)

The CPU enters stop or sleep mode is operated by writing CPU power saving register (PS). During the power saving mode, CPU holds the internal status of the system. In stop mode, the oscillator clocks will be stopped and system need a warm-up time for the stability of system clock running after wake up.

S-5: MCU System Operation Modes

The MCU has 4 operating modes, including high speed operation, low speed operation, sleep & stop modes. After power on reset, the MCU will go into high speed operation mode automatically. After wake up from stop/sleep mode, the MCU will resume the last operation mode.

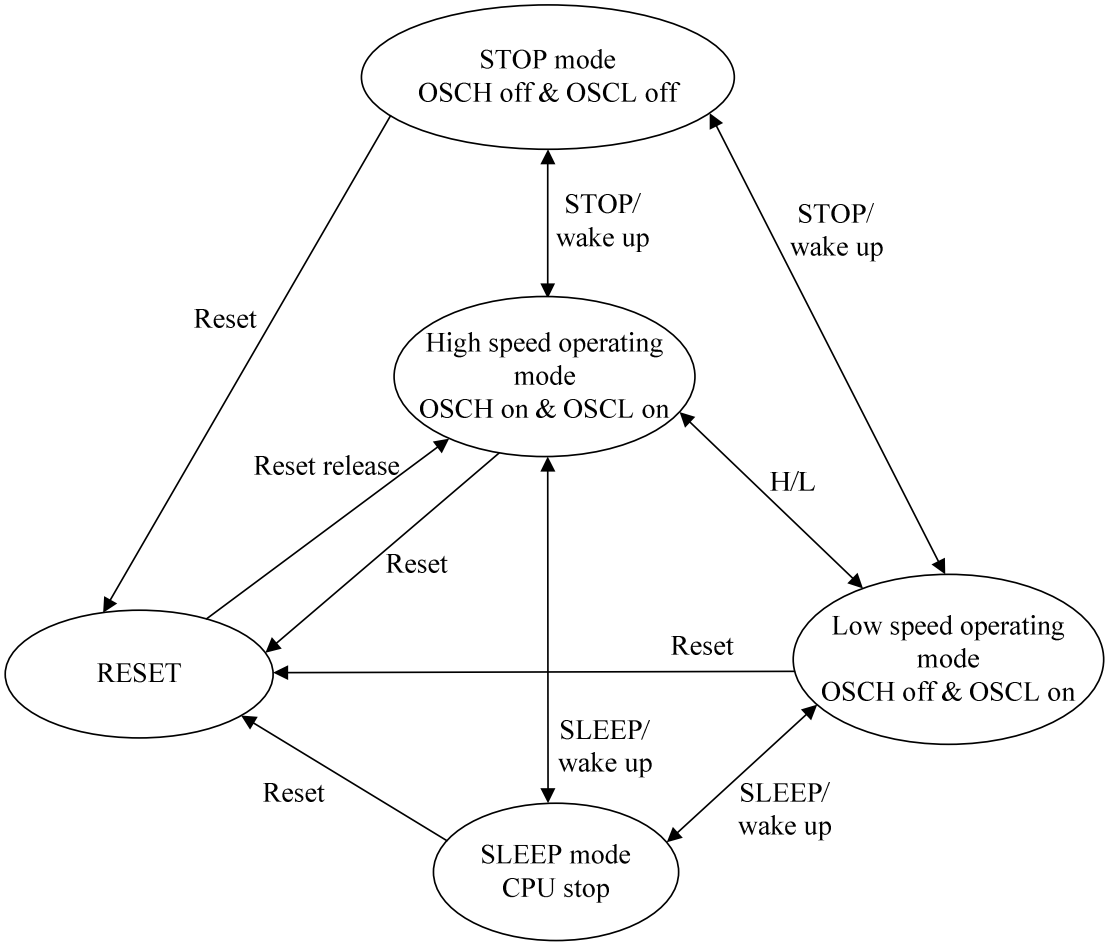


Figure: System Operation State Diagram

* Power saving mode condition & Release

Modes	Stop mode	Sleep mode
High speed oscillator	Stopped	Stopped as H/L=0
High speed oscillator	Stopped	Keep Operating
CPU clock	Stopped	Stopped
CPU internal status	Stop & Retain the status	
Memory, Flag, Register, I/O	Retain the status	
Program counter	Hold the next executed address	
Peripherals: Time base, Timers, Interrupts	Stopped & Retain	Keep Operating
Watch Dog Timer	Disable & cleared	
Release Condition	Reset, external INT, Input wake-up	Reset, external and internal INT sources, Input Wake-up

S-6: Watch Dog Timer (WDT)

The clock of watch dog timer comes from time base overflow (TB1OV). User can use the time up signal to prevent a software malfunction or abnormal sequence from jumping to an unknown memory location causing a system fatal failure. Normally, if the watchdog timer time up signal active that will reset the chip. At the same time, program and hardware can be initialized and resume system under normal operation. The chip also provides 2 steps clear watchdog command as the programmer writes INTF with $F data first that will enable the WDT clear, and then writes the power saving (PS) control register after. Completely finishes the two write steps will clear the watch dog timer. User should well arrange the two command steps for avoiding the dead lock loop.

User should keep in minds that always reset WDT at main program and never clear the WDT in the interrupt routine.

The max period of WDT =(TB1OV cycle time) * 8

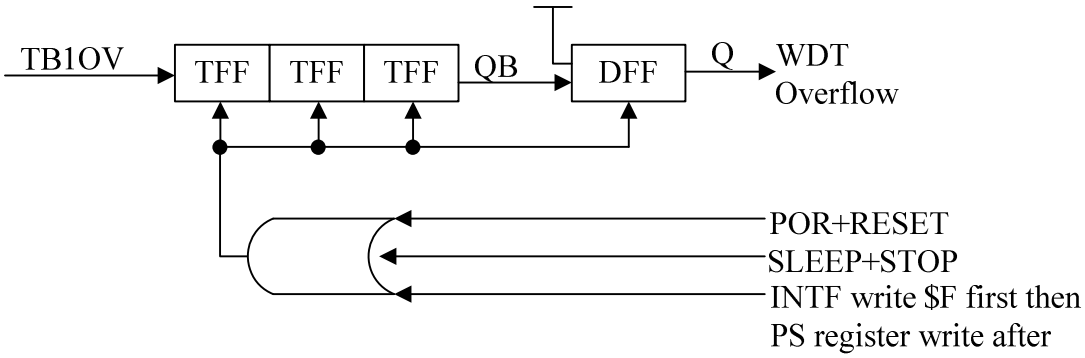


Figure: Watch Dog Timer control circuit

S-7: Low Voltage Reset (LVR)

The low voltage reset (LVR) forces the MCU in reset state during power failure, especially as MCU working in AC power application, preventing from abnormal state is the key issue. The control bit LVREN in power saving control register (PS) is for power saving. The detected voltage locates at 2.2V or 3.0V

S-8: RESET

The chip has four kinds of reset sources: POR (power on reset), External reset, Watch dog timer reset, LVR (low voltage reset). The reset feature will initialize the CPU and peripheral device with default state.

.POR (power on reset)

The chip provides automatic reset function when the power is turned on. The VDD should be below 1.6V and its rising slope (from 0.1VDD up to o.9VDD) needs less than 10ms.

.External Reset (RSTB)

This is one kind of system resetting signal, but only forced externally. When the chip acknowledged the low level from the pin RSTB exceed 1 us, it will generate the reset procedure to reset CPU & all the peripheral back to their initial state (default values).

.Burn out Reset (Program sequence abnormal)

As CPU out of program area, the CPU can detect the abnormal condition and generate a system reset request.

.Watch Dog Timer Reset

The reset signal will generate automatically when the watch dog timer runs overflow. If the watchdog timer is cleared regularly by users' program, no watchdog reset will occur. Unless the MCU is forced into abnormal state, the software controlled procedure is disrupted and causing watch dog timer overflow, then it will generate reset signal to initializes the chip returning to normal operation.

.Low Voltage Reset (LVR)

The LVR function is used to monitor the supply voltage of MCU, it will generate a reset signal (with 4*OSCL de-bounce time) to reset the microcontroller as the VDD power falls below the default setting level V_{LVR}. It can also be enabled or disabled by programming "LVREN" bit in PS register.

✧ RESETF (ADDRESS : 300H) : reset source flag register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	ROMF	BOF	LVRF	WDTF	0000B
Read/Write	R/W	R/W	R/W	R/W	

WDTF: Watch dog timer overflow reset flag (0: no active; 1: active)
LVRF: Low voltage reset flag (0: no active; 1: active)
BOF: Burn out flag (0: no active; 1: active)
ROMF: ROM fail flag (0: no active; 1: active)
(The RESETF is cleared by power on reset and external RESET)

S-9. Power saving control register

✧ PS (ADDRESS : 08H) : Power saving register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	LVREN	H/L	SLEEP	STOP	1100B
Read/write	R/W	R/W	R/W	R/W	

STOP: Into stop mode. (0: inactive; 1: active)
SLEEP: Into sleep mode. (0: inactive; 1: active)
H/L: System clock selection. (1: System clock; 0: peripheral clock)
LVREN: low voltage reset enable,(0:disable, 1:enable)

The SLEEP & STOP bits will be cleared to "0" automatically, when the release conditions occur from reset, interrupt or input wake up.

✧ PSP (ADDRESS : 09H) : Peripheral power saving register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	LDOEN	PFD2EN	PFD1EN	-	0000B
Read/write	R/W	R/W	R/W	-	

PFD1EN: PFD1 output enable (0: disable; 1: enable)

PFD2EN: PFD2 output enable (0: disable; 1: enable)

LDOEN: LDO enable (0: disable; 1: enable)

LDO voltage only supply touchpad circuit. When LDOEN=0, touchpad operate in VDD voltage. When LDOEN=1, touchpad operate in LDO output voltage. LDO output voltage is selected by option.

✧ LDO Flag (ADDRESS : 218H) : LDO falg register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	-	-	-	LDOFail	0000B
Read/write	-	-	-	R/W	

LDOFail: When VDD voltage is small then LDO voltage + 0.1V, LDOFail will be set. This bit can be clear by write 0.

The system oscillator generates the system control timing for CPU core or peripheral devices with fixed control phase, so the waveform of oscillator becomes sensitive to noise, abnormal duty especially fatal for CPU. Any switching of clock source needs oscillation stable time (OST) to make sure the oscillation is stable and synchronized with CPU timing phase. The relative OST for different oscillator with reference value as below table:

OST	From Stop state	oscillating	Unit
System clock(OSCH)	8	8	OSCH clock
RC Peripheral clock(OSCL)	8	8	OSCL RC clock

S-10. Interrupts

The CPU provides only 1 interrupt vector ($001H) and no priority, but can expand to multi-sources. Interrupt source includes external interrupts (INT0,INT1), timer/counter interrupts (TCP1INT), timer/PWM interrupts(TCP2INT), Time base timer interrupt (TBxINT). The interrupt control registers (INTC or INTC1) contain the interrupt control bits to enable and disable corresponding interrupt request and the corresponding interrupt request flags in the (INTF or INTF1) registers. Before finishing the INT service routine, another INT request will keep waiting until program return from interrupt routine.

If the interrupt request needs service, the programmer may set the corresponding INT enable bit to allow interrupt active. The triggered type of external interrupt can be selected in option. When external interrupts are triggered and set the related interrupt request flag (INTFx). The internal timer/counter interrupt is setting the TCP1F to 1, resulting from the timer/counter overflow. The internal timer/PWM interrupt is setting the TCP2F to 1, resulting from the timer/PWM overflow. The time base interrupt TBxINT was provided 2 periodic interrupt request cycles for user operating a periodic routine.

When the corresponding interrupt enable and flag bits is set to 1, the CPU will active the interrupt service routine. Then CPU reads the service flag and check the request priority then proceeds with the relative interrupt service. After CPU writes the corresponding bits to 0 in the INTFx register, the service flag will be cleared to 0(using STX #n,$m instruction). The INTF & INTF1 registers' bit can only write "0" to clear the flag. User writes "1" to Flag bit with no effect.

✧ INTC (ADDRESS : 0AH) : Interrupt control register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	TB2IE	TCP2IE	TCP1IE	TB1IE	0000B
Read/Write	R/W	R/W	R/W	R/W	

TB1IE: Enable time base 1st interrupt. (0: disable; 1: enable)
TCP1IE: Enable interrupt of timer/counter. (0: disable; 1: enable)
TCP2IE: Enable interrupt of timer/PWM. (0: disable; 1: enable)
TB2IE: enable time base 2nd interrupt. (0: disable; 1: enable)

✧ INTF (ADDRESS : 0BH) : Interrupt request flag register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	TB2F	TCP2F	TCP1F	TB1F	0000B
Read/Write	R/W	R/W	R/W	R/W	

TB1F: Time base timer 1st interrupt request flag. (0: inactive; 1: active)
TCP1F: Timer/counter interrupt request flag. (0: inactive; 1: active)
TCP2F: Timer/PWM interrupt request flag. (0: inactive; 1: active)
TB2F: Time base 2nd interrupt request flag. (0: inactive; 1: active)

✧ INTC1 (ADDRESS : 0CH) : Extended interrupt control register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	-	-	INT1IE	INT0IE	0000B
Read/Write	-	-	R/W	R/W	

INT0IE: enable INT0 external interrupt. (0: disable; 1: enable)
INT1IE: enable INT1 external interrupt. (0: disable; 1: enable)

✧ INTF1 (ADDRESS : 0DH): Extended interrupt request flag register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	-	-	INT1F	INT0F	0000B
Read/Write	-	-	R/W	R/W	

INT0F: INT0 external interrupt request flag. (0: inactive; 1: active)
INT1F: INT1 external interrupt request flag. (0: inactive; 1: active)

The trigged type of INT0F and INTF1 is defined in option.

✧ TPINTC (ADDRESS : 1EH) : Touchpad interrupt control register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	TPCTIE	TPCMPIE	-	-	0000B
Read/Write	R/W	R/W	-	-	

TPCMPIE: Capacitor overcharge interrupt enable. (0: disable; 1: enable)
TPCTIE: Duty counter overflow interrupt enable. (0: disable; 1: enable)

✧ TPINTF (ADDRESS : 1FH) : Touchpad request flag register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	TPCTF	TPCMPF	-	-	0000B
Read/Write	R/W	R/W	-	-	

TPCMPF: Capacitor overcharge's flag. (0: inactive; 1: active)
TPCTF: Duty counter overflow flag. (0: inactive; 1: active)

§ Peripheral function description:

P-1: System clock pre-scale

The system clock almost is the most high frequency of MCU. For various peripherals, application needs different clock source divided from system clock. TCPFS register is a selector for choosing suitable frequency (FS).

✧ TCPFS (ADDRESS : 20CH) : System clock pre-scale register[R/W]

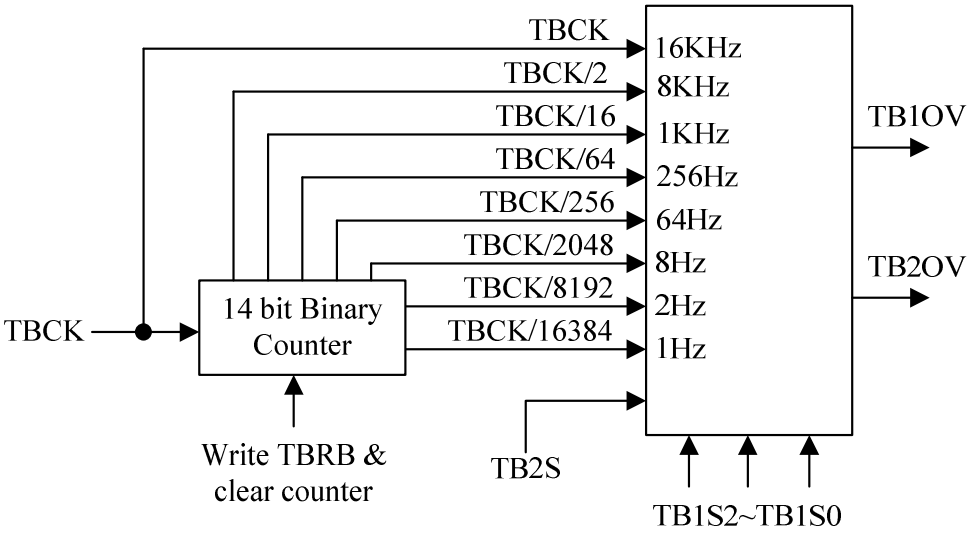
Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	-	FS2	FS1	FS0	0000B
Read/Write	-	R/W	R/W	R/W	

FS2~FS0: the selector value of TCPFS register

FS2 ~ FS0	FS	FS2 ~ FS0	FS
0	OSCH/1	4	OSCH/16
1	OSCH/2	5	OSCH/32
2	OSCH/4	6	OSCH/64
3	OSCH/8	7	OSCH/128

P-2: Time Base Counter

The time base counter has 2 interrupt sources and both of them come from the peripheral internal RC oscillator. The time base 1st overflow output (TB1OV) can cause interrupt and the period is selected by TB1S2~TB1S0 in TBC register. The time base 2nd frequency (TB2OV) also offers two sample frequency options by TB2S bit in the TBC register.



✧ TBC (ADDRESS : 20DH) : Time base control register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	TB2S	TB1S2	TB1S1	TB1S0	1111B
Read/Write	R/W	R/W	R/W	R/W	

TB1S2 ~ TB1S0: Base timer1 overflow frequency selection bits.

TB2S: Base timer2 overflow frequency selection (0: 32Hz; 1:16Hz)

(Every time writing the TBRB will clear the time base counter)

TB2S	Base timer overflow frequency (TB1OV)	TB2OV (OSCL=16K)
0	TBCK/512	32Hz
1	TBCK/1024	16Hz

TB1S2	TB1S1	TB1S0	Base timer overflow frequency (TB1OV)	TB1OV (OSCL=16K)
0	0	0	TBCK	16KHZ
0	0	1	TBCK/2	8KHZ
0	1	0	TBCK/16	1KHZ
0	1	1	TBCK/64	256HZ
1	0	0	TBCK/256	64 HZ
1	0	1	TBCK/2048	8HZ
1	1	0	TBCK/8192	2HZ
1	1	1	TBCK/16384	1HZ

P-3: 8 bits Timer/Counter/PFD (TCP) for TCP1 & 8 bits Timer/PWM/PFD (TCP) for TCP2

.Timer

When TCPx works as a Timer, user needs give the preload data TCPxD for periodic interrupt. After initial setting, user starts the TCPx counting by setting TCPxEN=1, the TCPx cycle period is: Tc = (selected clock cycle) * (TCPxD)

When user writes data to the TCPxD, the data just keep in TCPxL/H register. During the TCPxEN=1 command executed, the TCPxD's complement value will load into counter TCPx as initial value and start the timer function. Necessary TCP1LD=1(just in TCP1), timer run with reload feature as TCPx up counts and reaches the value 0f "FF_H" or 255. At the same time, interrupt request flag TCPxF will set activated, if software enables the corresponding interrupt enable bit, INT hardware will cause MCU interrupt service routine.

.PFD

The PFD Mode includes in timer mode and the output frequency is:

PFDx frequency = (selected clock frequency) / (2) / (TCPxD)

At this time, most users will disable the interrupt feature for tone or melody generation.

.Counter

Counter feature is implemented only by TCP1LD=0, the TCP1D can be zero or not that depends on software needs. User starts & stops the counter by changing the TCP1EN bit value. On the save side, reading the counter value after stopping the count by disable TCP1EN=0, if reading the counter value during value changing that means clock in happening at the same time. The reading of counter value may disrupt for transient state. If 8 bit counter is not enough for counting, user can enable the interrupt and using the data RAM as software counter for extending the counter stage.

.PWM

PWM feature is implemented only by PWM=1, the PWM's duty is define by TCP2D . User can set TPC2EN=1 and enable PWM function.

One 8-bits timer/counters/PFD (TCP) with 4 kind clock sources and preload data buffer can implement as a timer or counter feature , PFD is programmable frequency divider can support sound/melody/carrier generator. The clock sources of TCP1 are selected by TCP1S0 & TCP1S1

two bits of the timer control registers (TCP1C). TCP1OV is the timer or counter overflow signal and the rising edge will set the relative INT flag.

One 8-bits Timer/PWM/PFD (TCP) with 4 kind clock sources and PWM bit can select as a PWM or Timer feature , PFD is programmable frequency divider can support sound/melody/carrier generator, only in Timer mode. The clock sources of TCP2 are selected by TCP2S0 & TCP2S1 two bits of the timer control registers (TCP2C). TCP2OV is the timer or counter overflow signal and the rising edge will set the relative INT flag. If user select Timer function, IOPAD is PFD output. If user select PWM function, IOPAD is PWM output, and user must disable TCP2IE to disable TCP2 interrupt.

✧ TCP1C (ADDRESS : 200H) : Timer/counter/PFD control register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	TCP1LD	TCP1S1	TCP1S0	TCP1EN	0000B
Read/Write	R/W	R/W	R/W	R/W	

TCP1EN: TCP1 counting enabled. (0: disable; 1: enable)
TCP1LD: TCP1 auto-reload enabled. (0: disable; 1: enable)
TCP1S1 & TCP1S0: TCP1 clock source selection bits.

✧ TCP1L (ADDRESS : 201H): TCP1 low nibble data register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	TCP1_3/ TCP1D3	TCP1_2/ TCP1D2	TCP1_1/ TCP1D1	TCP1_0/ TCP1D0	0000B
Read/Write	R/W	R/W	R/W	R/W	

TCP1_3~TCP1_0: reading the counter low nibble data.
TCP1D3~TCP1D0: writing TCP1D low nibble of data buffer.

✧ TCP1H (ADDRESS : 202H) : TCP1 high nibble data register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	TCP1_7/ TCP1D7	TCP1_6/ TCP1D6	TCP1_5/ TCP1D5	TCP1_4/ TCP1D4	0000B
Read/Write	R/W	R/W	R/W	R/W	

TCP1_7~TCP1_4: reading the counter high nibble data.

TCP1D7~TCP1D4: writing TCP1D high nibble of data buffer.

TCP1D	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	TCP1D7	TCP1D6	TCP1D5	TCP1D4	TCP1D3	TCP1D2	TCP1D1	TCP1D0

TCP1D like a 8 bit TCP1 data register. The special R/W function for TCP1 has different Target, AS writing TCP1H/L registers that are updating preload data of the TCP1D. As read TCP1H/L registers that are the brand new TCP1 counter value.

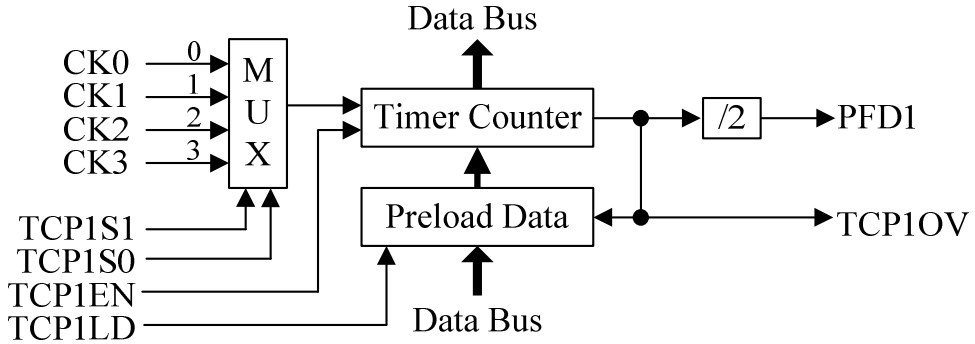


Figure: Timer/Counter/PFD

TCP1S1	**TCP1S0**		**TCP1**
0	0	CK0	FS
0	1	CK1	TCP1I
1	0	CK2	TBCK
1	1	CK3	TB1OV

	PFD Output
TCP1	PFD1

FS: System scaled frequency.

TCP1I: External clock input from PA1.

TBCK: Peripheral clock source, 16KHZ in the RC mode.

TB1OV: Time base 1st overflow output.

PFD1: TCP1 cycle time/2 output signal

TCP1OV: Timer/counter1's overflow output.

✧ TCP2C (ADDRESS : 203H) : Timer/PWM /PFD control register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PWM	TCP2S1	TCP2S0	TCP2EN	0000
Read/Write	R/W	R/W	R/W	R/W	

TCP2EN: TCP2 counting enabled. (0: disable; 1: enable)

PWM: PWM or Timer select. (0: Timer; 1: PWM)

TCP2S1 & TCP2S0: TCP2 clock source selection bits.

✧ TCP2L (ADDRESS : 204H) : TCP2 low nibble data register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	TCP2_3/ TCP2D3	TCP2_2/ TCP2D2	TCP2_1/ TCP2D1	TCP2_0/ TCP2D0	0000
Read/Write	R/W	R/W	R/W	R/W	

TCP2_3~TCP2_0: reading the counter low nibble data.

TCP2D3~TCP2D0: writing TCP2D low nibble of data buffer.

✧ TCP2H (ADDRESS : 205H) : TCP2 high nibble data register[R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	TCP2_7/ TCP2D7	TCP2_6/ TCP2D6	TCP2_5/ TCP2D5	TCP2_4/ TCP2D4	0000
Read/Write	R/W	R/W	R/W	R/W	

TCP2_7~TCP2_4: reading the counter high nibble data.

TCP2D7~TCP2D4: writing TCP2D high nibble of data buffer.

TCP2D	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	TCP2D7	TCP2D6	TCP2D5	TCP2D4	TCP2D3	TCP2D2	TCP2D1	TCP2D0

TCP2D like a 8 bit TCP2 data register. The special R/W function for TCP2 has different Target, AS writing TCP2H/L registers that are updating preload data of the TCP2D or PWM duty select register. As read TCP2H/L registers that are the brand new TCP2 counter value.

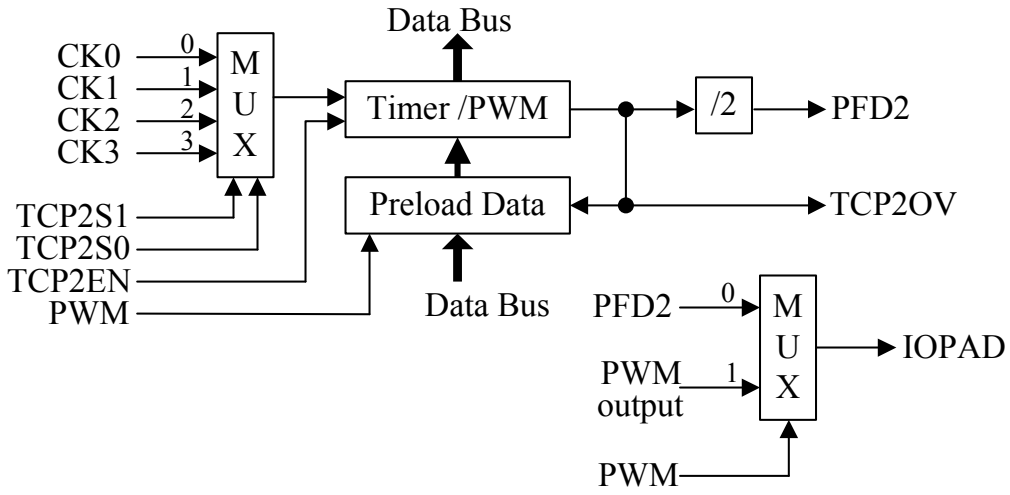


Figure: Timer/PWM /PFD

TCP2S1	TCP2S0		Timer	PWM
0	0	CK0	FS	FS
0	1	CK1	TCP2I	OSCH
1	0	CK2	TBCK	TBCK
1	1	CK3	TCP1OV	TB1OV

	PFD Output
TCP2	PFD2

FS: System scaled frequency.

TCP2I: External clock input from PB1.

TBCK: Peripheral clock source, 16KHZ in the RC mode.

TB1OV: Time base 1st overflow output.

OSCH: High speed system oscillator

TCP1OV: Timer/counter1's overflow output.

PFD2: TCP2 cycle time/2 output signal

TCP2OV: Timer/PWM's overflow output.

TCP2D7~TCP2D0	PWM duty
0	0/256
1	1/256
2	2/256
.....	.....
254	254/256
255	255/256

Figure:PWM duty define

. I/O PAD Cell Structure & Function Description

.. Input Port

The input port can mask option with pull high resistor and input data can read by port reading command. As mask option with pull-up resister then a wake-up function also offers the system wake up feature for keys or special external triggers.

Input Data	Pull-high	Read Data	Wake-up
0	R	0	Active
0	No	0	Inhibited
1	R	1	Non-active
1	No	1	Inhibited
Floating	R	1	Non-active
Floating	No	?	Inhibited

R: pull-up resistor

X: don't care the value

?: unknown

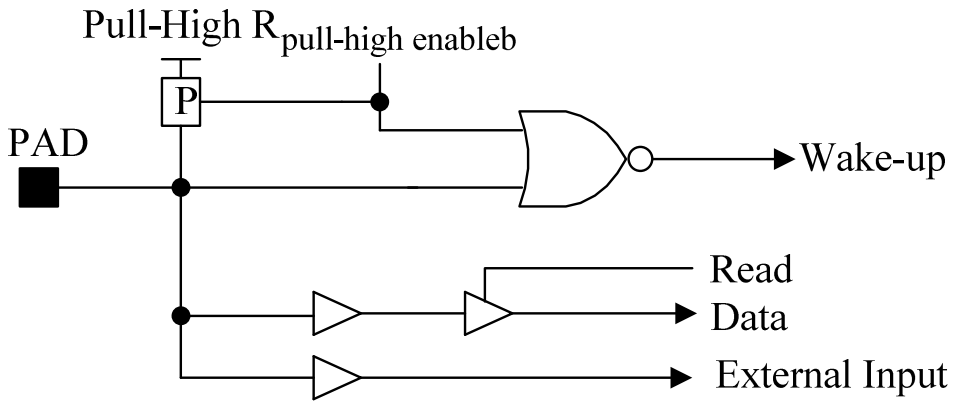


Figure IO-E: Input Port

.. I/O Port with external input

The input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. Software can performs a configuration (data=0, changing the control 0 or 1) for open drain type that specifies suitable for key scan application. An additional feature supports the interrupt input triggers and Timer external clock sources.

I/O control Data	Output data	Pull-up R	Wake-up feature	External inputs
0	X	No	No	No
1	0	No	No	Enable
1	1	Enable	Enable	Enable

X: don't care the value

I/O control Data	MODE	PAD
0	Output mode	Output Register data
1	Input mode	Input data

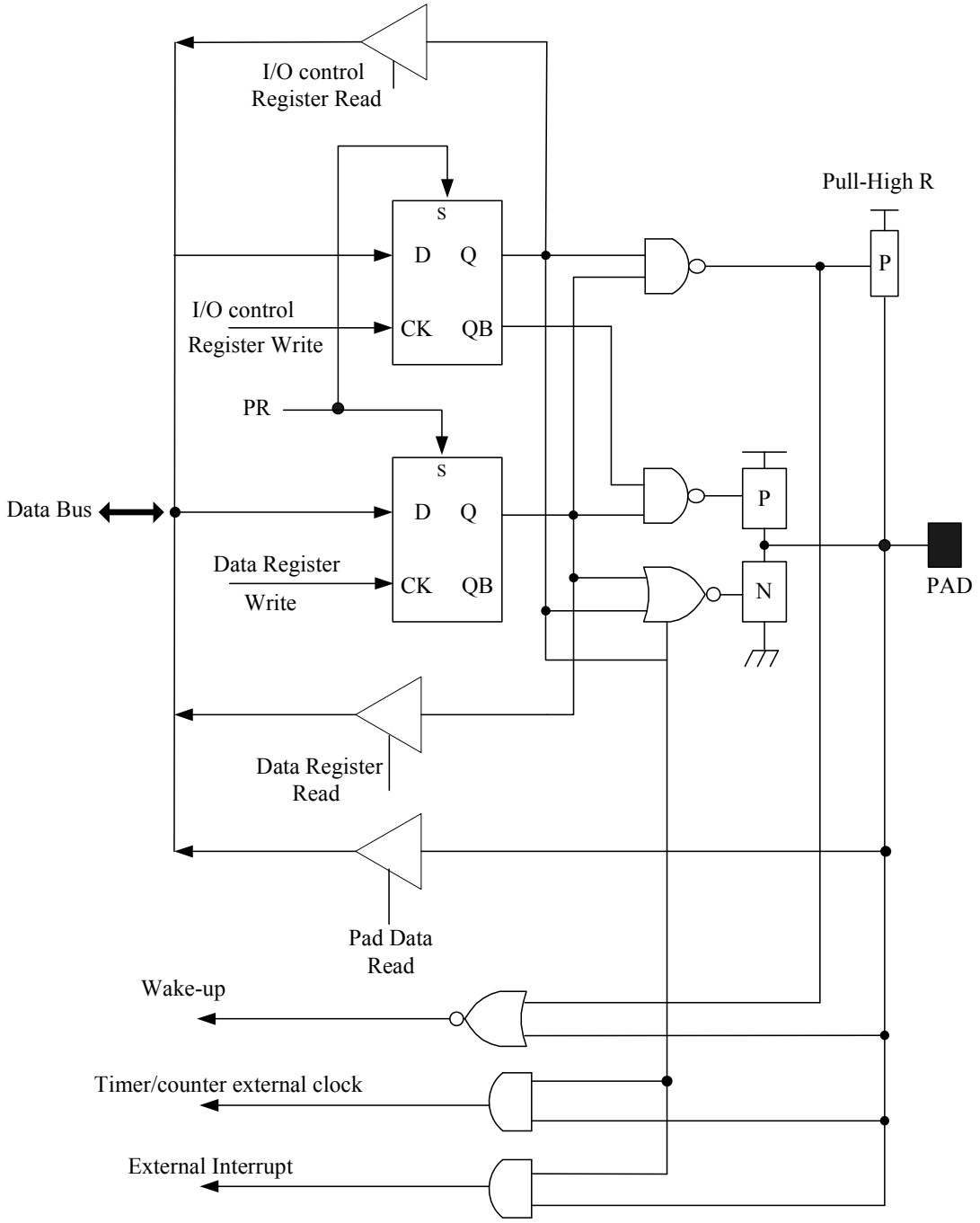


Figure IO-A: Standard IO Port with wake-up/interrupt/timer clock inputs

.. I/O port with internal output

The standard input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. If enable internal output by mask option, the internal output will control by output data (on/off) and outputs to PAD. Internal output refers to the internal buzzer, PFD or PWM output, etc.

I/O control Data	Output data	Pull-up	Wake-up
0	X	No	No
1	0	No	No
1	1	Enable	Enable

X: don't care the value

I/O control Data	Internal output	PAD
0	enable	Output internal data
0	disable	Output Register data
1	X	PAD input data

X: don't care the value

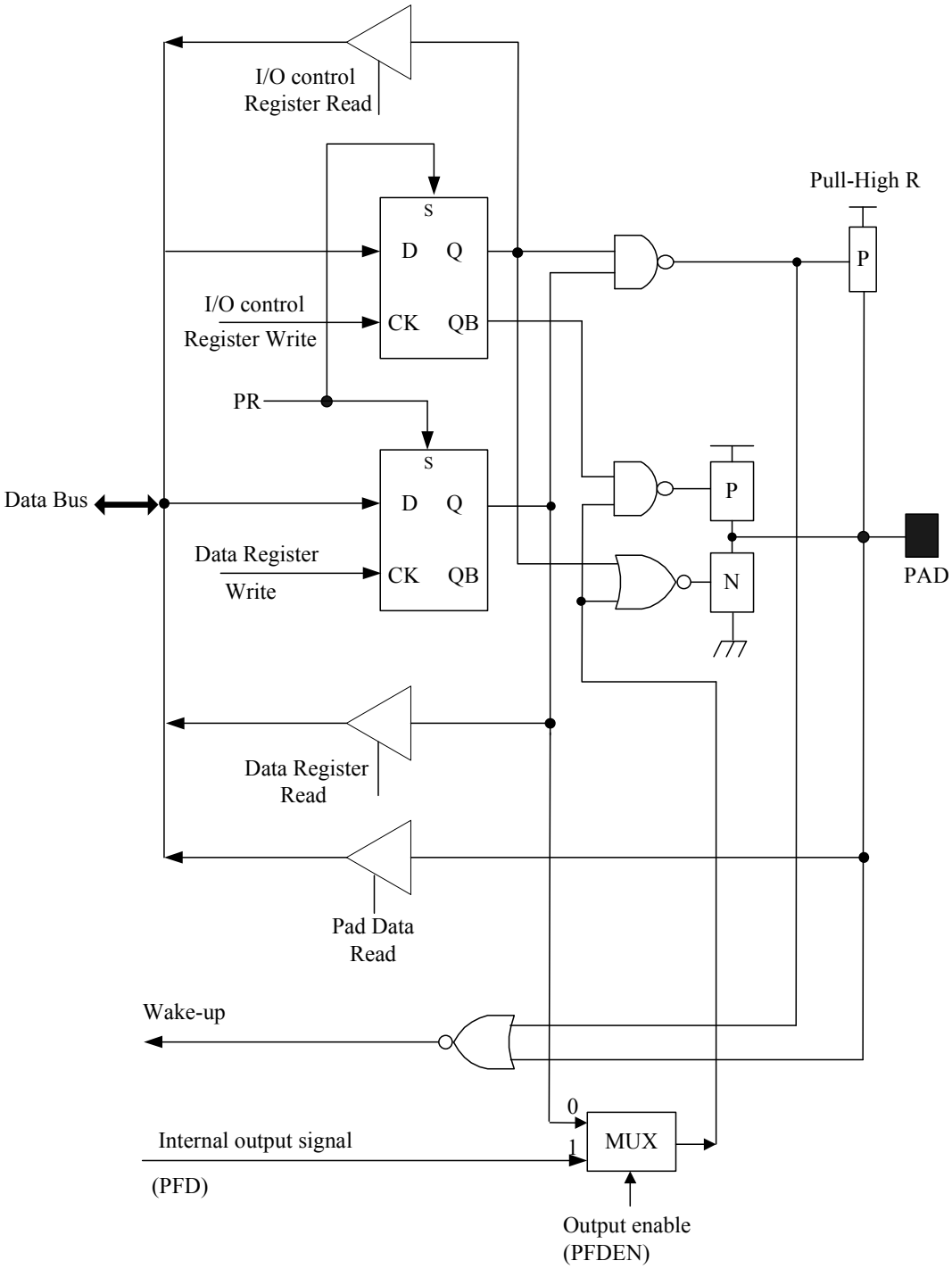


Figure IO-B: Standard I/O Port with internal output signal

.. Standard I/O Port

The standard input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. Software can performs a configuration (data=0, changing the control 0 or 1) for open drain type that specifies suitable for key scan application.

I/O control Data	Output data	Pull-up	Wake-up
0	X	No	No
1	0	No	No
1	1	Enable	Enable

X: don't care the value

I/O control Data	MODE	PAD
0	Output mode	Output Register data
1	Input mode	Input data

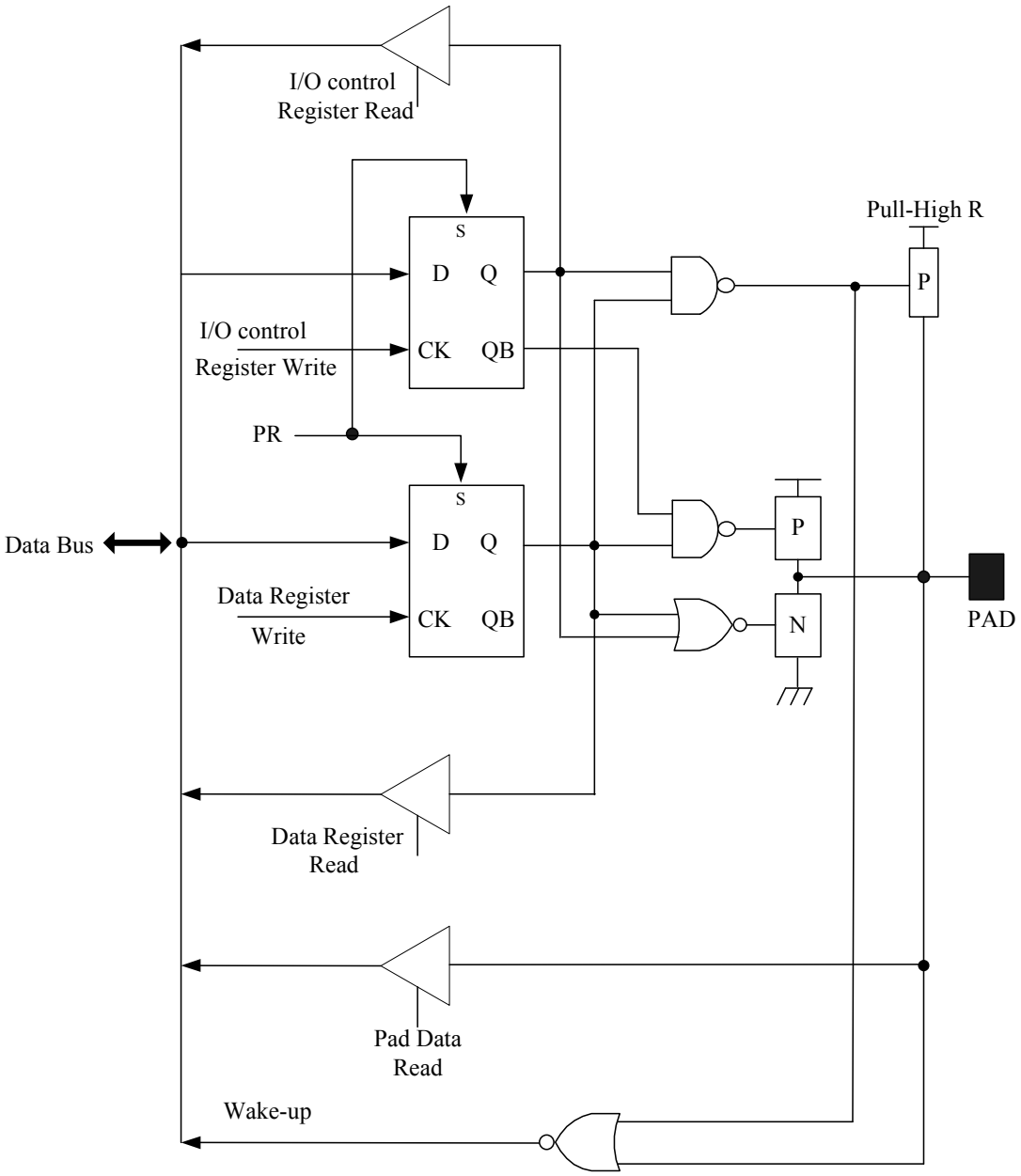


Figure IO-C: Standard I/O Port

.. I/O port with internal output & external input

The standard input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. If enable internal output by mask option, the internal output will control by output data (on/off) and outputs to PAD. Internal output refers to the internal buzzer, PFD or PWM output, etc.

I/O control Data	Output data	Pull-up	Wake-up
0	X	No	No
1	0	No	No
1	1	Enable	Enable

X: don't care the value

I/O control Data	Internal output	PAD
0	enable	Output internal data
0	disable	Output Register data
1	X	PAD input data

X: don't care the value

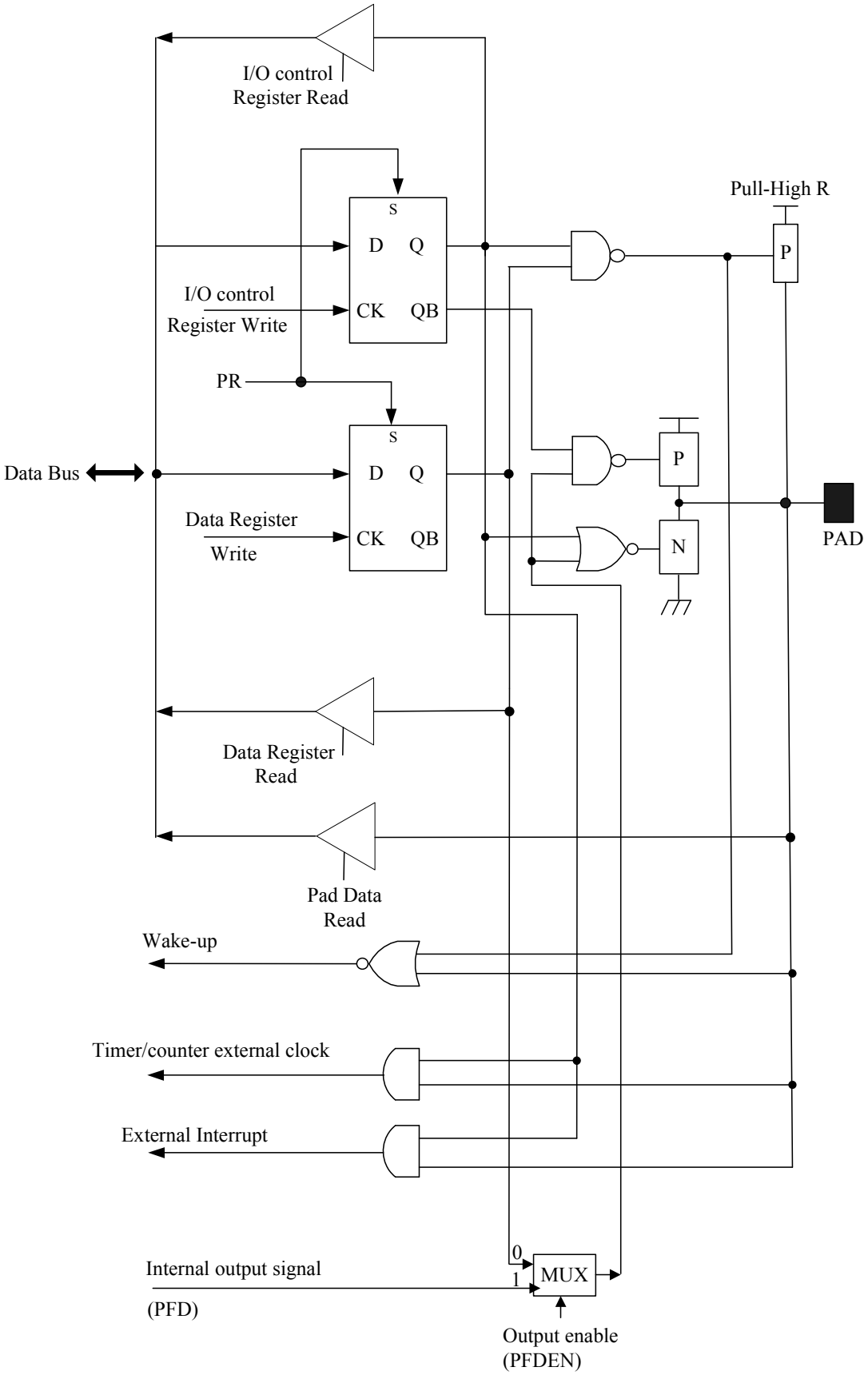


Figure IO-D: Standard I/O Port with internal output signal & external input

I/O Pad Cells

The main features of pad cell are including ESD/EFT protection and general I/O access. A general I/O pad cell can be configured as input with or without pull-up resistor, or working as a CMOS or NMOS output driver. The input pad cell must have pull-up resistor for avoiding a floating state when user doesn't care or not be used. For concerning the standby current, user can use data register or I/O control register to fit the application.

. I/O File Register

✧ PAC (ADDRESS : 12H) : Port A I/O control register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PAC3	PAC2	PAC1	PAC0	1111B
Read/Write	R/W	R/W	R/W	R/W	

PAC3~PAC0: port A' I/O control register.

✧ PA (ADDRESS : 13H) : Port A data register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PA3	PA2	PA1	PA0	1111B
Read/Write	R/W	R/W	R/W	R/W	

PA3~PA0: port A' data register.

✧ PBC (ADDRESS : 14H) : Port B I/O control register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PBC3	PBC2	PBC1	PBC0	1111B
Read/Write	R/W	R/W	R/W	R/W	

PBC3~PBC0: port B I/O control register.

✧ PB (ADDRESS : 15H) : Port B data register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PB3	PB2	PB1	PB0	1111B
Read/Write	R/W	R/W	R/W	R/W	

PB3~PB0: port B data register.

✧ PCC (ADDRESS : 16H) : Port C I/O control register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PCC3	PCC2	PCC1	PCC0	1111B
Read/Write	R/W	R/W	R/W	R/W	

PCC3~PCC0: port C I/O control register.

PC0 is input pin, PCC0 and PC0 remain for pull-up control.

✧ PC (ADDRESS : 17H) : Port C data register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PC3	PC2	PC1	PC0	1111B
Read/Write	R/W	R/W	R/W	R/W	

PC3~PC0: port C data register.

✧ PDC (ADDRESS : 18H) : Port D I/O control register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PDC3	PDC2	PDC1	PDC0	1111B
Read/Write	R/W	R/W	R/W	R/W	

PDC3~PDC0: port D I/O control register.

✧ PD (ADDRESS : 19H) : Port D data register [R/W]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PD3	PD2	PD1	PD0	1111B
Read/Write	R/W	R/W	R/W	R/W	

PD3~PD0: port D data register.

✧ PAI (ADDRESS : 206H) : Port A pad data reading address [R]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PAI3	PAI2	PAI1	PAI0	----B
Read/Write	R	R	R	R	

PAI3~PAI0: port A' pad data

✧ PBI (ADDRESS : 207H) : Port B pad data reading address [R]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PBI3	PBI2	PBI1	PBI0	----B
Read/Write	R	R	R	R	

PBI3~PBI0: port B' pad data

✧ PCI (ADDRESS : 208H): Port C pad data reading address [R]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PCI3	PCI2	PCI1	PCI0	----B
Read/Write	R	R	R	R	

PCI3~PCI0: port C' pad data

✧ PDI (ADDRESS : 209H) : Port D pad data reading address [R]

Register	Bit3	Bit2	Bit1	Bit0	Default Value
Bit Name	PDI3	PDI2	PDI1	PDI0	----B
Read/Write	R	R	R	R	

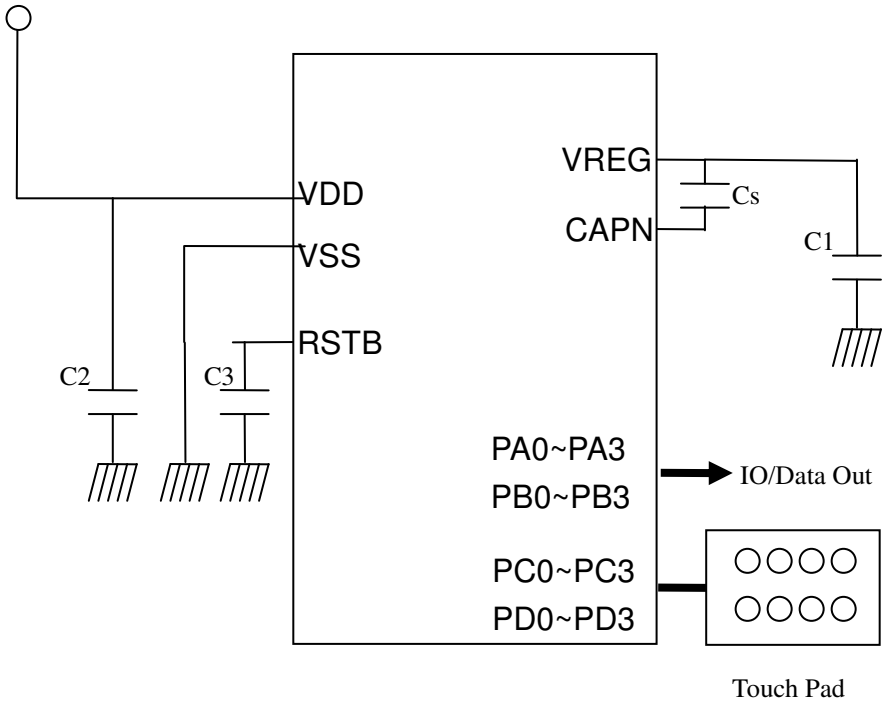
PDI3~PDI0: port D' pad data

§ Mask Option Table:

The following table shows the mask option in this chip. All the mask options must be defined clearly and ensure to meet user's proper function.

No.	Mask Option	Function Descriptions	
+1	LVR output Voltage select	0	2.2V
		1	3.0V
+1	PSR select	0	Low PSR
		1	High PSR
+2	PC3 special function select	00	disable
		01	PWM/PFD2
		10	PFD1
		11	INT0
+2	PD0 special function select	00	disable
		01	PWM/PFD2
		10	PFD1
		11	INT1
+2	INT0F trigger type INT0S1,INT0S0	00	Low level trigger
		01	Falling edge trigger
		10	Rising edge trigger
		11	Dual edge trigger
+2	INT1F trigger type INT1S1,INT1S0	00	Low level trigger
		01	Falling edge trigger
		10	Rising edge trigger
		11	Dual edge trigger
+1	LDO output Voltage select	0	2.7V
		1	4.2V
+1	LVREN select	0	LVREN disable
		1	LVREN enable

§ Application Circuit



§ REVISION HISTORY：

2012/02/08：(Ver. 3.0)

2018/10/04：(Ver. 3.1) Modify Page 5 Top=-40~+85