# TTP252 Target Spec.

## § PATENTED

1. PATENT：『電流源控制及補償觸控電容感測方法及其裝置』
   PAT NO. I339356 (Taiwan)
   PAT NO. ZL 2007 1 0202087. 0 (CHINA)
2. PATENT：『具環境變化校正的電容式觸控感測裝置』
   PAT NO. M383780 (Taiwan)
   PAT NO. ZL 2010 2 0141537. 7 (CHINA)
3. PATENT：『省電型多鍵觸摸開關感測裝置』
   PAT NO. M375250 (Taiwan)
   PAT NO. ZL 2010 2 0302392. 4 (CHINA)

## § General Description:

TTP252 MCU is an easy-used 4-bit CPU base microcontroller. It contains 1984-word ROM、96-nibble RAM、timer/Counter、timer/PWM、interrupt service 、IO control hardware、LVR、touch pad and LDO feature for specified applications. The device is also suitable for diverse simple applications in control appliance and consumer product.

## § Features:

1. Tontek RISC 4-bit CPU core
2. Total 26 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
4. advance CMOS process
5. Working memory with 1984*16 program ROM and 96*4 SRAM
6. 2-level stacks
7. Operating voltage: 2.0V~5.5V
8. System operating frequency: (at VDD=5V )
   . High speed system oscillator (OSCH):
   - ✧ Built-in RC oscillator: 4MHz(typical)

   .Low speed peripheral oscillator (OSCL):
   - ✧ Built-in RC oscillator: 16KHz(typical)
9. Offer 8 IO+8 touch pad or 16 general programmable I/O
   - ✧ IO port built-in key wake-up feature enable by software setting
   - ✧ Providing external interrupt inputs and Timer clock inputs
   - ✧ Offering internal signal outputs, like buzzer(PFD)
10. One 8-bit auto-reload timer/counter & one 8-bit timer/PWM & one time

base counter

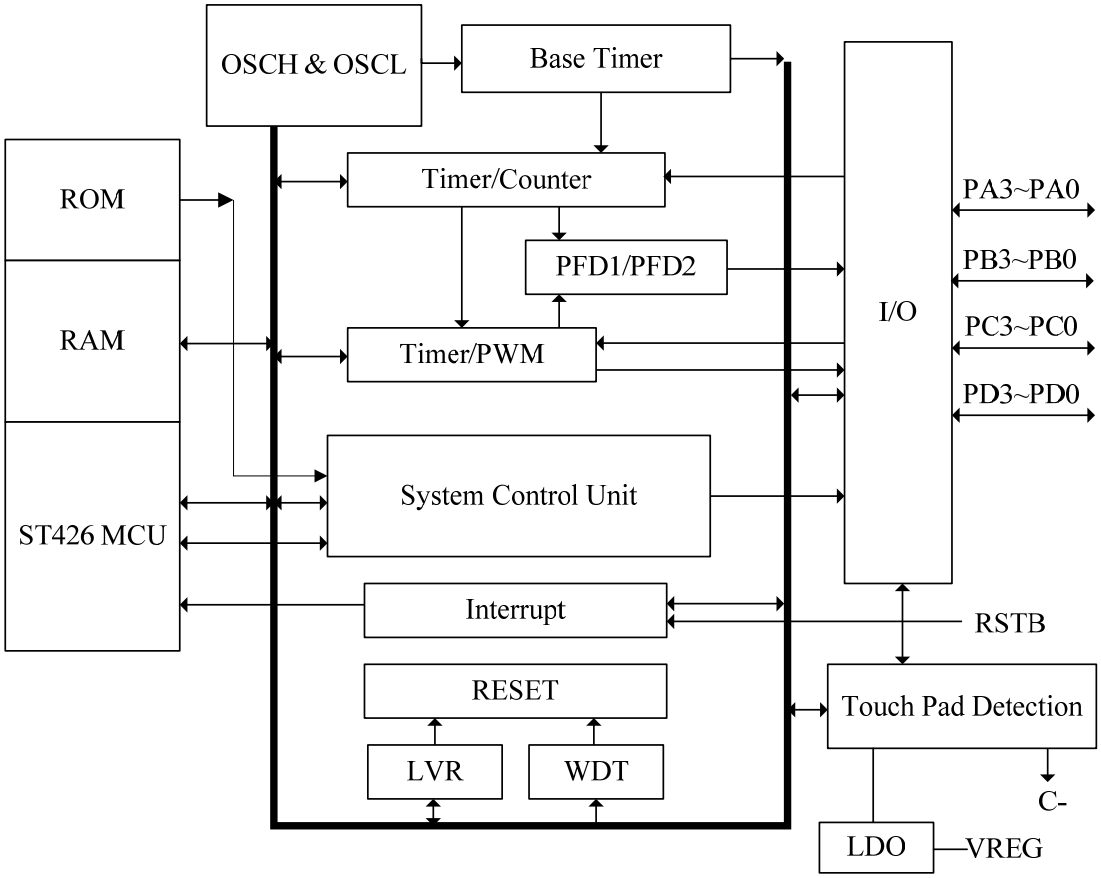
- ✧ 4 timer clock sources(internal & external) selected by software
- ✧ Timer provides the PFD feature for Buzzer output driver
- ✧ Time base offers 2 various period interrupt request

11. MCU system protection and power saving controlled mode:
    - ✧ Built-in watch dog timer (WDT) circuit
    - ✧ ROM code error detection
    - ✧ Out of user program's range detection
    - ✧ Providing high/low system operating speed、sleep、stop mode for power saving control
    - ✧ Built-in low voltage reset (LVR) function
12. 8 pins with touch pad detection
13. LDO voltage can select 2.7V or 4.2V output by option.
14. LVR voltage can select 2.2V or 3.0V by option.
15. Provides 8 interrupt sources
    - ✧ External: INT0 , INT1 shared with IO pad
    - ✧ Internal: Timer/counter, Timer/PWM, two Time base timer
    - ✧ Two touchpad's interrupt
16. Provide package types
    - ✧ DIP/SOP 8 pins, DIP/SOP/SSOP/QFN 16/20/24 pins, TSSOP 20pins
    - ✧ Dice available

## § Applications:

1. Household electric appliances
2. Consumer products
3. Measurement controller

## § Block Diagram:



## § Pin Description:

| Pin Name | Share Pin | I/O | Pin no. | Mask Option | Pin Description |
|---|---|---|---|---|---|
| $V_{DD}$ | - | Power | +1 | - | Positive power supply |
| $V_{SS}$ | - | Power | +1 | - | Negative power supply, ground |
| RSTB | - | I | +1 | - | External reset input, active low, 50kΩ pull-up( $V_{DD}$ =5v) |
| PA0(INT0)<br>PA1(TCP1I)<br>PA2(PFD1)<br>PA3(PFD2/PWM) | | IO<br>IO<br>IO<br>IO | +4 | - | I/O port with external interrupt input (PA0). PA1 is used as clock inputs of timer/counter1. PA2 is shared with internal PFD1 output. PA3 is shared with internal PFD2 or PWM output. |
| PB0<br>PB1(TCP2I)<br>PB2<br>PB3 | - | IO<br>IO<br>IO<br>IO | +4 | - | I/O port with internal signal output. PB1 is used as clock inputs of timer/PWM . |
| PC0(VPP)<br>PC1<br>PC2(INT1)<br>PC3(PWM/PFD2/PFD1/INT0) | TP0<br>TP1<br>TP2<br>TP3 | I<br>IO/I<br>IO/I<br>IO/I | +4 | PC/TP | IO port or touch pad input. PC2 is shared with external interrupt input. PC3 is shared with external interrupt input and PFD1/PFD2/PWM output. |
| PD0(PWM/PFD2/PFD1/INT1)<br>PD1<br>PD2<br>PD3 | TP4<br>TP5<br>TP6<br>TP7 | IO/I<br>IO/I<br>IO/I<br>IO/I | +4 | PD/TP | IO port or touch pad input. PD0 is shared with external interrupt input and PFD1/PFD2/PWM output. |
| C- | - | O | +1 | - | Touch signal output with pull up R |
| VREG | - | Power | +1 | - | LDO output |
| | | | 21 | | |

* If PC3 select INT0 option, and PA0's INT0 will be disable. If PC3's option don't select INT0 , and PA0 have INT0 function.
* If PD0 select INT1 option, and PC2's INT1 will be disable. If PD0's option don't select INT1 , and PC2 have INT1 function.
* If PC3 or PD0 select PFD1, it will disable PA2's PFD1 function. PC3's PFD1 function and PD0's PFD1 function can be enable in same time.
* If PC3 or PD0 select PWM/PFD2, it will disable PA3's PWM/PFD2 function. PC3's PWM/PFD2 function and PD0's PWM/PFD2 function can be enable at same time.

## § IO Cell type Description:

| Pin Name | I/O Type | Description |
|---|---|---|
| PA0~PA1 | Figure IO-A | STD IO with external input |
| PA2~PA3 | Figure IO-B | STD IO with internal output |
| PB0 | Figure IO-C | STD IO |
| PB1 | Figure IO-A | STD IO with external input |
| PB2~PB3 | Figure IO-C | STD IO |
| PC0 | Figure IO-E | Input Port |
| PC1 | Figure IO-C | STD IO |
| PC2 | Figure IO-A | STD IO with external input |
| PC3,PD0 | Figure IO-D | STD IO with internal output & external input |
| PD0~PD3 | Figure IO-A | STD IO with external input |

## § Absolute Maximum ratings:

| ITEM | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Operating Temperature | Top | -40℃ ~ +85℃ | ℃ |
| Storage Temperature | Tst | -50℃ ~ +125℃ | ℃ |
| Supply Voltage | VDD | VSS-0.3 ~ VSS+6.0 | V |
| OTP Supply Voltage | VPP | VSS-0.3 ~ VSS+12.5 | V |
| Input Voltage | Vin | VSS -0.3 ~ VDD+0.3 | V |
| Human Body Mode | ESD | >=5 | KV |

Note: VSS symbolizes for system ground

## § DC Characteristics: (Test condition at room temperature=25°C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | $F_{OSCH}$=4MHz<br>(LVR OFF)<br>(LVR ON) | 2.0<br>2.0<br>2.2 | -<br>-<br>- | 5.5<br>5.5<br>5.5 | V |
| Operating Current (Normal Mode CPU working, I/O no load ) | $I_{nd1}$ | VDD=5.0V, no load, $F_{OSCH}$=4MHz, | - | 1.5 | 2.0 | mA |
| | $I_{nd2}$ | VDD=5.0V, no load, $F_{OSCL}$ on | - | 30 | 50 | uA |
| Operating Current (Sleep Mode, CPU stop, I/O no load) | $I_{sd1}$ | VDD=5.0V, no load, $F_{OSCH}$=4MHz, | - | 1.5 | 2.0 | mA |
| | $I_{sd2}$ | VDD=3.0V, no load, $F_{OSCL}$ on | - | 5 | 10 | uA |
| Standby Current | Istb | I/O no load, $F_{OSCH}$ & $F_{OSCL}$ stop | - | - | 1.0 | uA |
| Input Ports | $V_{IL}$ | Input Low Voltage | 0 | - | 0.2 | $V_{DD}$ |
| Input Ports | $V_{IH}$ | Input High Voltage | 0.8 | - | 1.0 | $V_{DD}$ |
| RSTB & INT | $V_{IL}$ | Input Low Voltage | 0 | - | 0.3 | $V_{DD}$ |
| RSTB & INT | $V_{IH}$ | Input High Voltage | 0.7 | - | 1.0 | $V_{DD}$ |
| Output port Sink Current | $I_{OL}$ | VDD=5.0V, $V_{OL}$=0.6V | - | 8 | - | mA |
| Output Port Source Current | $I_{OH}$ | VDD=5V, $V_{OH}$=VDD-0.7V | - | -4 | - | mA |
| I/O Port Pull-High Resistor | $R_{PH}$ | VDD=5.0V | 100 | 150 | 200 | KΩ |
| RSTB Pull-High Resistor | $R_{PH}$ | VDD=5.0V | 30 | 50 | 80 | KΩ |
| Low Voltage Reset (LVR) | $V_{LVR1}$ | - | 2.0 | 2.2 | 2.4 | V |
| | $V_{LVR2}$ | - | 2.7 | 3.0 | 3.3 | V |

## § AC Characteristics:

| Parameter | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| External Reset | Low active pulse width $t_{RES}$ | | 2 | - | - | CPU clock |
| Interrupt input | Low active pulse width $t_{INT}$ | | 2 | - | - | |
| Wake up input | Low active pulse width $t_{wkup}$, Application de-bounce should be manipulated by user' software | | 2 | - | - | OSCL |
| System Oscillator Frequency | $F_{OSCH}$ (Built-in RC) | VDD=5.0V | - | 4M | - | Hz |
| Peripheral Oscillator Frequency | Built-in $F_{OSCL}$(RC) | VDD=2.0~5.0V | 12K | **16K** | 21K | Hz |
| Startup Period of Oscillators | $T_{OSCH}$ (Built-in RC) | wake-up from off mode | 8 | - | - | $F_{OSCH}$ |
| | $T_{OSCL}$ (Built-in RC) | Wake-up from off mode | 8 | - | - | $F_{OSCL}$ |
| Stable Time Of System Clock Switching | $T_{OSCH}$ ( Built-in RC) | OSCL→OSCH & OSCH off | 8 | - | - | $F_{OSCH}$ |
| | (If H/L=0 then OSCH stop) | | | | | |
| | $T_{OSCL}$ ( Built-in RC) | OSCH→OSCL & OSCL on | 8 | - | - | $F_{OSCL}$ |
| Timer/Counter input clock frequency | Input frequency rating, no de-bounce circuit built-in ,at VDD=5V | | DC | - | 4M | Hz |
| System Stable Time after Power up | After power up, the system needs to initialize the configured state and OST. | | - | - | 40 | ms |

## § Memory Map:

| ROM ADDRESS | RAM ADDRESS | Function Block |
|---|---|---|
| $000_H$~$7BF_H$ | - | Program ROM [1984*16] |
| - | $000_H$ ~$007_H$ | File Registers |
| - | $008_H$~$01F_H$ | Peripheral registers (I) |
| - | $020_H$~$07F_H$ | Working RAM [96*4] |
| - | $200_H$~$30F_H$ | Peripheral registers (II) |

## § Interrupt Vectors:

| Interrupt Vectors | Function Description |
|---|---|
| **$000** | hardware RESET |
| **$001** | Hardware IRQ |

## § File registers:

| Address | Symbol | R/W | Default | Description |
|---|---|---|---|---|
| $000_H$ | (DP1) | R/W | - | Indirect addressing register |
| $001_H$ | ACC | R/W | - | Accumulator & Read Table 1st data |
| $002_H$ | TB1 | R/W | - | Read Table 2nd data |
| $003_H$ | TB2 | R/W | - | Read Table 3rd data |
| $004_H$ | TB3 | R/W | - | Read Table 4th data |
| $005_H$ | DPL | R/W | - | Data Pointer low nibble |
| $006_H$ | DPM | R/W | - | Data Pointer middle nibble |
| $007_H$ | DPH | R/W | - | Data Pointer high nibble |

## § Peripheral registers: Interrupt request flag register

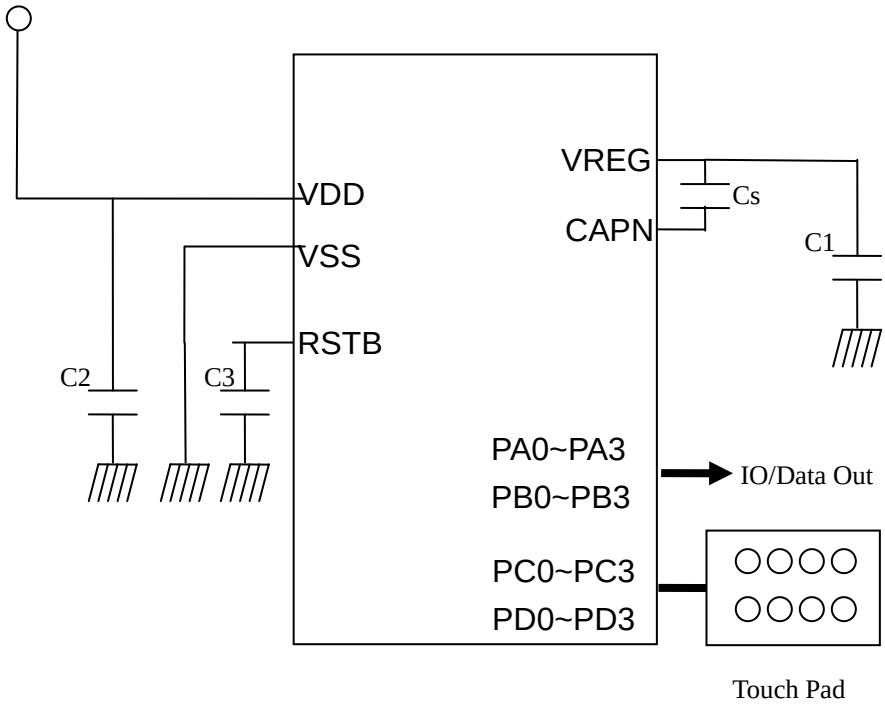
| Address | Symbol | R/W | Default | Description |
|---|---|---|---|---|
| $008_H$ | PS | R/W | 1100 | CPU power saving control register |
| $009_H$ | PSP | R/W | 0000 | Peripheral power saving control register |
| $00A_H$ | INTC | R/W | 0000 | Interrupt enable control register |
| $00B_H$ | INTF | R/W | 0000 | Interrupt request flag register |
| $00C_H$ | INTC1 | R/W | 0000 | Extended interrupt enable register |
| $00D_H$ | INTF1 | R/W | 0000 | Extended interrupt request flag register |
| $00E_H$ | - | - | - | - |
| $00F_H$ | - | - | - | - |
| $010_H$ | - | - | - | - |
| $011_H$ | - | - | - | - |
| $012_H$ | PAC | R/W | 1111 | I/O port A control register |
| $013_H$ | PA | R/W | 1111 | I/O port A data register |
| $014_H$ | PBC | R/W | 1111 | I/O port B control register |
| $015_H$ | PB | R/W | 1111 | I/O port B data register |
| $016_H$ | PCC | R/W | 1111 | I/O port C control register |
| $017_H$ | PC | R/W | 1111 | I/O port C data register |
| $018_H$ | PDC | R/W | 1111 | I/O port D control register |
| $019_H$ | PD | R/W | 1111 | I/O port D data register |
| $01A_H$ | | | | |
| $01B_H$ | - | - | - | - |
| $01C_H$ | - | - | - | - |
| $01D_H$ | - | - | - | - |
| $01E_H$ | | | | |
| $01F_H$ | | | | |

| | | | | |
|---|---|---|---|---|
| $200_H$ | TCP1C | R/W | 0000 | Timer/counter 1 control register |
| $201_H$ | TCP1L | R/W | xxxx | Timer/counter 1 data low register |
| $202_H$ | TCP1H | R/W | xxxx | Timer/counter 1 data high register |
| $203_H$ | TCP2C | R/W | 0000 | Timer/counter 2 control register |
| $204_H$ | TCP2L | R/W | xxxx | Timer/counter 2 data low register |
| $205_H$ | TCP2H | R/W | xxxx | Timer/counter 2 data high register |
| $206_H$ | PAI | R | ---- | Port A pad data reading address |
| $207_H$ | PBI | R | ---- | Port B pad data reading address |
| $208_H$ | PCI | R | ---- | Port C pad data reading address |
| $209_H$ | PDI | R | ---- | Port D pad data reading address |
| $20A_H$ | - | - | - | - |
| $20B_H$ | - | - | - | - |
| $20C_H$ | TCPFS | R/W | 0000 | TCP clock source FS pre-scale register |
| $20D_H$ | TBC | R/W | 1111 | Time base control register |
| $20E_H$ | | | | |
| $20F_H$ | | | | |
| $210_H$ | | | | |
| $211_H$ | | | | |
| $212_H$ | | | | |
| $213_H$ | | | | |
| $214_H$ | - | - | - | - |
| $215_H$ | - | - | - | - |
| $216_H$ | - | - | - | - |
| $217_H$ | - | - | - | - |
| $218_H$ | LDO flag | R/W | 0000 | LDO fail flag address |
| $219_H$ | CPUFS | R/W | 0000 | CPU freq. select. |
| $21A_H$ | - | - | - | - |
| $300_H$ | RESETF | R/W | 0000 | Reset flag |
| $301_H$ | TBRB | W | xxxx | Time base counter clear address |
| $302_H$ | MRO | W | xxxx | Reserved for testing |

Note: a. Default means initial value after power on or reset.

b. R is “read” only, W is “write” only, R/W is both of “read” & “write”.

## § Application Circuit



# § REVISION HISTORY：

2012/02/08：(Ver. 3.0)

2018/10/04：(Ver. 3.1) Modify Page 5 Top=-40~+85