TTP255 Target Spec.

§ General Description:

TTP255 MCU is an easy-used 4-bit CPU base microcontroller. It contains 4K-word ROM、384-nibble RAM、timer/Counter、interrupt service 、IO control hardware、touch pad feature、LDO and TT-BUS for specified applications. The device is also suitable for diverse applications in control appliance and consumer product.

§ Features:

1. Tontek Dual RISC 4-bit CPU cores
2. Total 26 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
4. advance CMOS process
5. Working memory with 4K*16 program ROM and 256*4 SRAM
6. 4-level stacks for CPUA (+4 stacks for CPUB)
7. Operating voltage: 2.0V~5.5V
8. System operating frequency: (at VDD=5V)
   . High speed system oscillator (OSCH):
   - ✧ Resonator mode: 400KHz~8MHz
   - ✧ RC mode: 150KHz~4MHz
   - ✧ Built-in RC oscillator: 4MHz(typical at 5V)
   - ✧ External clock mode: DC~8MHz

   .Low speed peripheral oscillator (OSCL):
   - ✧ Built-in RC oscillator: 16KHz(typical)
9. Offer 8~20 general programmable I/O or input pins
   - ✧ Built-in key wake-up feature enable by software setting
   - ✧ Providing external interrupt inputs and Timer clock inputs
   - ✧ Offering internal signal outputs, like buzzer(PFD)
10. Two 8-bit auto-reload timer/counter & one time base counter
    - ✧ 4 timer clock sources(internal & external) selected by software
    - ✧ Timer provides the PFD feature for Buzzer output driver
    - ✧ Time base offers 2 various period interrupt request
11. MCU system protection and power saving controlled mode:
    - ✧ Built-in watch dog timer (WDT) circuit
    - ✧ Providing high/low system operating speed、sleep、stop mode

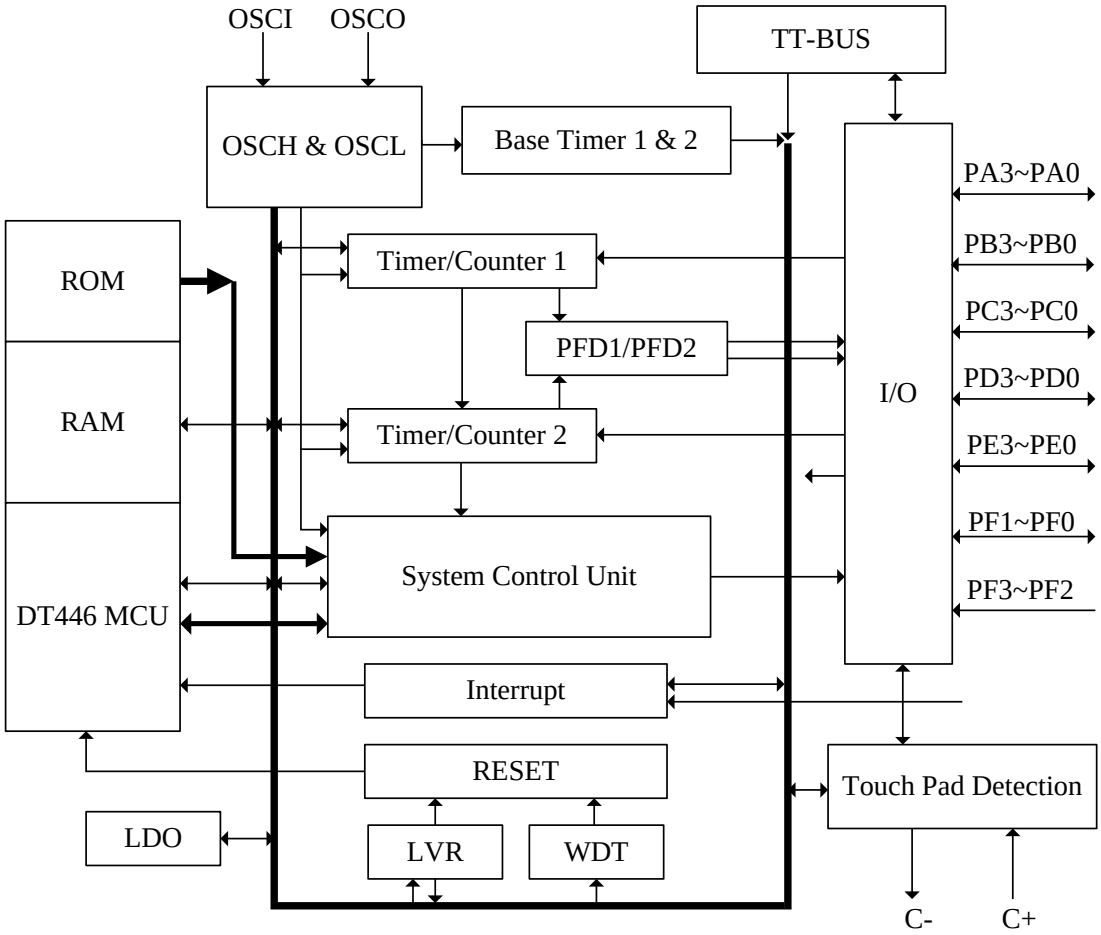
for power saving control
- ✧ Built-in low voltage reset (LVR) function

12. 16 Touch pads detection features
13. Provides 13 interrupt sources
    - ✧ External: INT0 & INT1 shared with IO pad
    - ✧ Internal: Timer/counter 1/2, IIC & Time base timer
    - ✧ Software interrupt request for CPU A & B
    - ✧ Touch pad detect and Touch pad detect overflow interrupt
14. Provide LDO to avoid Power noise
    - ✧ Select 2.7V or 3.3V output by option
15. Provide two wire serial interface (TT-BUS)
16. Provide package types
    - ✧ QFN 32 pin, SKDIP/SOP 28 pin ,
      SKDIP/SOP/SSOP/TSSOP 24 pin,
      SKDIP/SOP/SSOP/TSSOP 20 pin,
      SKDIP/SSOP 16 pin
    - ✧ Dice available

§ Applications:

1. Household electric appliances
2. Consumer products
3. Measurement controller

§ Block Diagram:



§ Pin Description:

Pin Name	Share Pin	I/O	Pin no.	Mask Option	Pin Description
RSTB		I	+1		External reset input, active low 50kΩ pull-up(5v)
V_{DD}		Power	+1		Positive power supply
OSCI OSCO	RCOSC/PF2 RCOSC4/PF3	I/I O/I	+2	RC/Crystal /Port F	Crystal/resonator/RC oscillator terminals or PF2~PF3 Input port
PA0 PA1(TCP1I) PA2 PA3	INT0/VPP	IO IO IO IO	+4		I/O port with external interrupt input (PA0). PA1 used as clock inputs of timer/counter 1.
PB0(PFD1) PB1(PFD2) PB2(pfd1b) PB3(pfd2b)	INT1/SCL SDA TP12 TP13	IO IO IO IO	+4	PB/TP PB/TP	I/O port with external interrupt input (PB0). I/O port with internal signal output
V_{SS}		Power	+1		Negative power supply, ground
PC0~PC3	TP0~TP3	IO/I	+4	PC/TP	IO port or touch pad input
PD0~PD3	TP4~TP7	IO/I	+4	PD/TP	IO port or touch pad input
C+		I	+1		Touch sensor input
C-		O	+1		Touch signal output with pull up R
PE0~PE3	TP8~TP11	IO/I	+4	PE/TP	IO port or touch pad input
PF0~PF1	TP14~TP15	IO/I	+2	PF/TP	IO port or touch pad input

§ IO Cell type Description:

Pin Name	I/O Type	Description
PA0~PA3	Figure IO-A	STD IO with external input
PB0~PB3	Figure IO-B	STD IO with internal output
PC0~PC3	Figure IO-A	STD IO with external input
PD0~PD3	Figure IO-A	STD IO with external input
PE0~PE3	Figure IO-A	STD IO with external input
PF0~PF3	Figure IO-A	STD IO with external input

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-40℃ ~ +85℃	℃
Storage Temperature	Tst	-50℃ ~ +125℃	℃
Supply Voltage	VDD	VSS-0.3 ~ VSS+6.0	V
OTP Supply Voltage	VPP	VSS-0.3 ~ VSS+12.5	V
Input Voltage	Vin	VSS -0.3 ~ VDD+0.3	V
Human Body Mode	ESD	>5	KV
Note: VSS symbolizes for system ground			

§ DC and AC Characteristics

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	F_{OSCH}=1MHz (LVR OFF) (LVR ON)	2.0 2.0 2.2	- - -	5.5 5.5 5.5	V
Operating Current (Normal Mode, CPU working, I/O no load , LVR off)	I_{nd1}	VDD=5.0V, no load, F_{OSCH}=8MHz,	-			mA
	I_{nd2}	VDD=5.0V, no load, F_{OSCH}=4MHz(RC)	-	3.5	-	
	I_{nd3}	VDD=5.0V, no load, F_{OSCL} on	-	30	50	uA
Operating Current (Sleep Mode, CPU stop, I/O no load, LVR off)	I_{sd1}	VDD=5.0V, no load, F_{OSCH}=8MHz,	-			uA
	I_{sd2}	VDD=5.0V, no load, F_{OSCH}=4MHz(RC),	-	600	-	
	I_{sd3}	VDD=3.0V, no load, F_{OSCL} on	-	5	10	uA
Standby Current	Istb	I/O no load, F_{OSCH} & F_{OSCL} stop	-	-	1.0	uA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
RESET & INT	V_{IL}	Input Low Voltage	0	-	0.3	VDD
RESET & INT	V_{IH}	Input High Voltage	0.7	-	1.0	VDD
Output port Sink Current	I_{OL}	VDD=5.0V, VOL=0.6V	-	8	-	mA
Output Port Source Current	I_{OH}	VDD=5V, VOH=VDD-0.7V	-	-4	-	mA
I/O Port Pull-High Resistor	R_{PH}	VDD=5.0V	100	150	200	KΩ
RESET Pull-High Resistor	R_{PH}	VDD=5.0V	30	50	80	KΩ
Low Voltage Reset (LVR)	V_{LVR1}	LVRC = 1	2.7	3.0	3.3	V
	V_{LVR2}	LVRC = 0	2.0	2.2	2.4	V
Oscillator Start up voltage	$\mathbf{V_{ST}}$	F_{OSC}=4MHz	-	1.8	-	V
Oscillator Sustain voltage	$\mathbf{V_{SU}}$	F_{OSC}=4MHz	-	1.7	-	V

§ AC Characteristics:

Parameter	Test Condition		Min	Typ.	Max	Unit
External Reset	Low active pulse width t_{RES}		2	-	-	
Interrupt input	Low active pulse width t_{INT}		2	-	-	
Wake up input	Low active pulse width t_{wkup}, Application de-bounce should be manipulated by user' software		2	-	-	OSCL
System Oscillator Frequency	F_{OSCH}(Crystal)	VDD=5.0V	400K	-	8M	Hz
	F_{OSCH}(Crystal)	VDD=3.0V	400K	-	4M	
	F_{OSCH}(RC)	VDD=5.0V	150K	-	4M	
	F_{OSCH}(RC)	VDD=3.0V	150K	-	1M	
Peripheral Oscillator Frequency	Built-in F_{OSCL}(RC)	VDD=2.0~5.0V	10K	16K	22K	Hz
Startup Period of Oscillators	T_{OSCH} (Crystal)	wake-up from off mode	-	-	4	F_{OSCH}
	T_{OSCH} (RC)		4	-	-	F_{OSCL}
	T_{OSCL} (RC)	Wake-up from off mode	4	-	-	F_{OSCL}
Stable Time of System Clock Switching	T_{OSCH} (Crystal)	OSCL→OSCH & OSCH off	-	-	4	F_{OSCH}
	T_{OSCH} (RC)		4	-	-	F_{OSCL}
	(If H/L=0 then OSCH stop)					
	T_{OSCL} (Crystal)	OSCH→OSCL & OSCL on	2	-	-	F_{OSCL}
	T_{OSCL} (RC)		2	-	-	F_{OSCL}
Timer/Counter input clock frequency	Input frequency rating, no de-bounce circuit built-in ,at VDD=5V		DC	-	8M	Hz
System Stable time after Power up	After power up, the system needs to initialize the configured state and OST.		-	-	40	ms

§ Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~FFF_H		Program ROM [4K*16]
	000_H~007_H	File Registers
	008_H~$01F_H$	Peripheral registers (I)
	020_H~$19F_H$	Working RAM [384*4]
	200_H~301_H	Peripheral registers (II)

§ Interrupt Vectors:

Interrupt Vectors	Function Description
$000	CPU A hardware RESETB
$001	CPU A INT hardware IRQB /Soft IRQB
$002	CPU B hardware RESETB
$003	CPU B INT hardware IRQB /Soft IRQB

§ File registers:

Address	Symbol	R/W	Default	Description
000_H	(DP1)	R/W	-	Indirect addressing register
001_H	ACC	R/W	-	Accumulator & Read Table 1st data
002_H	TB1	R/W	-	Read Table 2nd data
003_H	TB2	R/W	-	Read Table 3rd data
004_H	TB3	R/W	-	Read Table 4th data
005_H	DPL	R/W	-	Data Pointer low nibble
006_H	DPM	R/W	-	Data Pointer middle nibble
007_H	DPH	R/W	-	Data Pointer high nibble

§ Peripheral registers:

Address	Symbol	R/W	Default	Description
008_H	PS	R/W	1100	CPU power saving control register
009_H	PSP	R/W	0000	Peripheral power saving control register
$00A_H$	INTAC	R/W	0000	Interrupt enable control register for CPU A
$00B_H$	INTAF	R/W	0000	Interrupt request flag register
$00C_H$	INTBC	R/W	0000	Interrupt enable control register for CPU B
$00D_H$	INTBF	R/W	0000	Interrupt request flag register
$00E_H$	INTAC1	R/W	0000	Extended interrupt enable register for CPU A
$00F_H$	INTBC1	R/W	0000	Extended interrupt enable register for CPU B
010_H	INTF1	R/W	0000	Extended interrupt request flag1 register
011_H	INTF2	R/W	0000	Extended interrupt request flag2 register
012_H	PAC	R/W	1111	I/O port A control register
013_H	PA	R/W	1111	I/O port A data register
014_H	PBC	R/W	1111	I/O port B control register
015_H	PB	R/W	1111	I/O port B data register
016_H	PCC	R/W	1111	I/O port C control register
017_H	PC	R/W	1111	I/O port C data register
018_H	PDC	R/W	1111	I/O port D control register
019_H	PD	R/W	1111	I/O port D data register
$01A_H$	PEC	R/W	1111	I/O port E control register
$01B_H$	PE	R/W	1111	I/O port E data register
$01C_H$	PFC	R/W	--11	I/O port F control register
$01D_H$	PF	R/W	--11	I/O port F data register
$01E_H$	TPINTC	R/W	0000	Touch pad interrupt enable register
$01F_H$	TPINTF	R/W	0000	Touch pad interrupt request flag register
200_H	TCP1C	R/W	0000	TCP1 Timer/counter A control register
201_H	TCP1L	W/R	0000	TCP1 Timer/counter A data low register
202_H	TCP1H	R/W	0000	TCP1 Timer/counter A data high register
203_H	TCP2C	R/W	0000	TCP2 Timer/counter A control register
204_H	TCP2L	R/W	0000	TCP2 Timer/counter A data low register
205_H	TPC2H	R/W	0000	TCP2 Timer/counter A data high register
206_H	PAI	R	----	Port A pad data reading address

207_H	PBI	R	----	Port B pad data reading address
208_H	PCI	R	----	Port C pad data reading address
209_H	PDI	R	----	Port D pad data reading address
$20A_H$	PEI	R	----	Port E pad data reading address
$20B_H$	PFI	R	----	Port F pad data reading address
$20C_H$	TCPFS	R/W	0000	TCP clock source FS pre-scale register
$20D_H$	TB1C	R/W	1111	Time base1 control register
$20E_H$	TB2C	R/W	1111	Time base2 control register
$20F_H$	---	---	---	---
210_H	---	---	---	---
211_H	---	---	---	---
212_H	---	---	---	---
213_H	---	---	---	---
214_H	---	---	---	---
215_H	---	---	---	---
216_H	---	---	---	---
217_H	---	---	---	---
218_H	LDOFLAG	R/W	---0	LDO flag register
230_H	TTADRL	R/W	000-	IIC Low Address register
231_H	TTADRH	R/W	0000	IIC High Address register
232_H	TTCTR1	R/W	1---	IIC Control 1 register
233_H	TTCTR2	R/W	00-0	IIC Control 2 register
234_H	TTSR1	R/W	-001	IIC Status 1 register
235_H	TTSR2	R/W	000-	IIC Status 2 register
236_H	TTDRL	R/W	0000	IIC Low Data register
237_H	TTDRH	R/W	0000	IIC High Data register
---	---	---	---	---
300_H	RESETF	R/W	0000	Reset flag
301_H	TBRB	W	---	Time base counter clear address

Note: a. Default means initial value after power on or reset.
b. R is “read” only, W is “write” only, R/W is both of “read” & “write”.

§ System function description:

S-1: System Oscillators

The high speed oscillator can be operated in 3 different oscillator modes; resonator mode, RC mode & external clock mode. The oscillator mode can be defined by mask option.

✧ Resonator/crystal mode (400K Hz~8M Hz oscillator)

A 400K Hz~8M Hz crystal across OSCI and OSCO pads, capacitors are connected between OSCI/OSCO pads and ground (VSS).

✧ RC mode (150KHz~4MHz oscillator, built-in mode fixed 4MHz)

The external resistor connected OSCI and the other end ground to VSS. The recommend value of R_{ext} between 60KΩ and 500KΩ, if used R_{ext} value too low (under 2KΩ), the oscillator will become unstable or stop. On the other hand, if used R_{ext} value too high (over 1MΩ), the oscillator will easily be interfered by external radiation. OSCH/4 output signal is the internal oscillating RC clock divided by 4 and keeps at high level during system reset.

✧ External clock mode (DC~8MHz)

The oscillator supports the external clock direct input (OSCI). For the clock source directly drives the crystal oscillator input, so it needs the same wake up time (OST) as crystal mode from power on or power saving mode.

S-2: Peripheral Oscillators

The low speed oscillator was built-in an internal RC oscillator that is for low power consumption consideration and fixed peripheral device timing control. The peripheral oscillator provides three models for user's selection, but the target peripheral oscillator frequency is set about 16 KHz. The external R mode is just for micro-adjustment for more accurate 16 KHz frequency.

✧ Built-in RC oscillator and the frequency range between 12 KHz ~ 22 KHz.

S-3: CPU clock

The CPU clock comes from system/peripheral oscillator which was controlled by H/L bit in PS register. In the normal operation, the system clock comes from high speed system oscillator (OSCH/2). The low speed operation frequency (OSCL/2) comes from RC oscillator was selected by mask option.

Crystal oscillator/
External clock

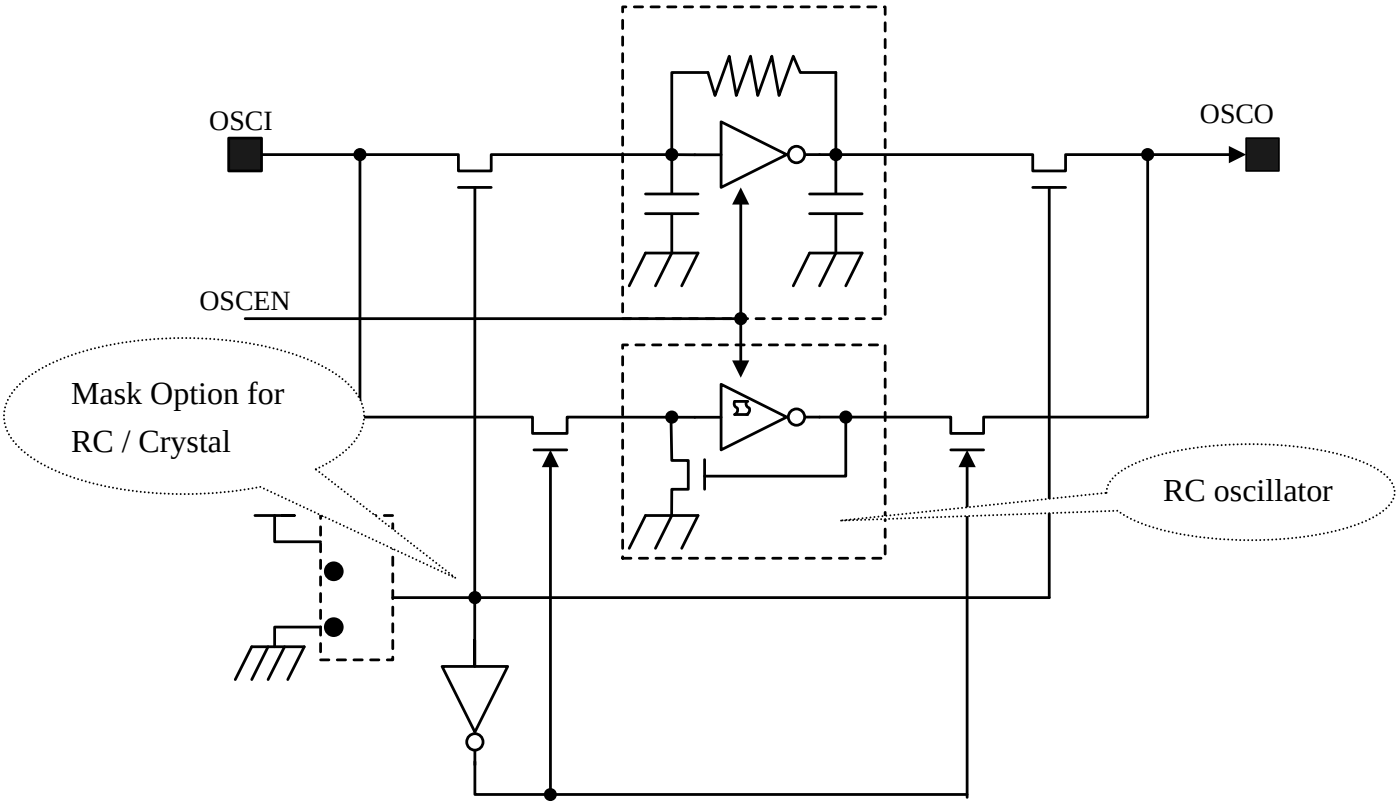


Figure: System High Speed Oscillator

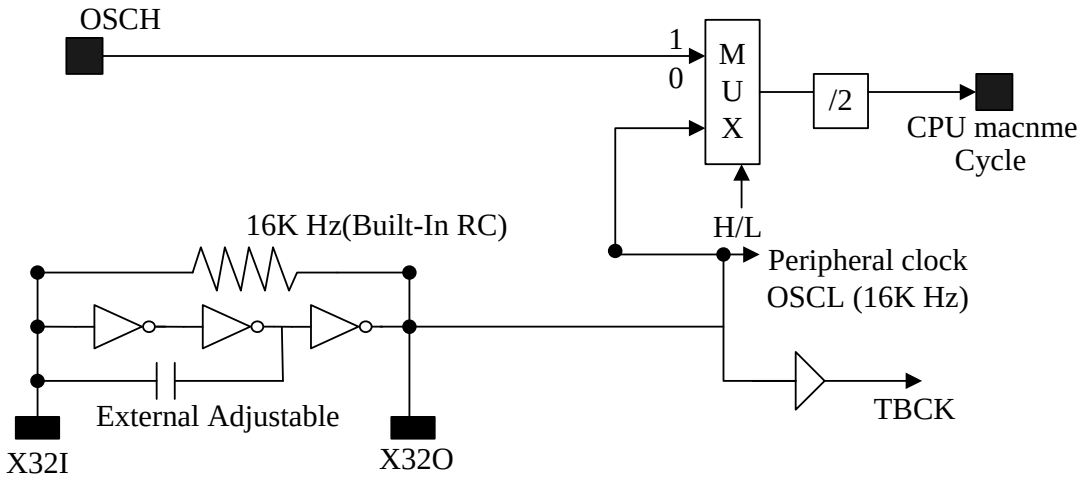


Figure: System Oscillator & CPU Clock Sources

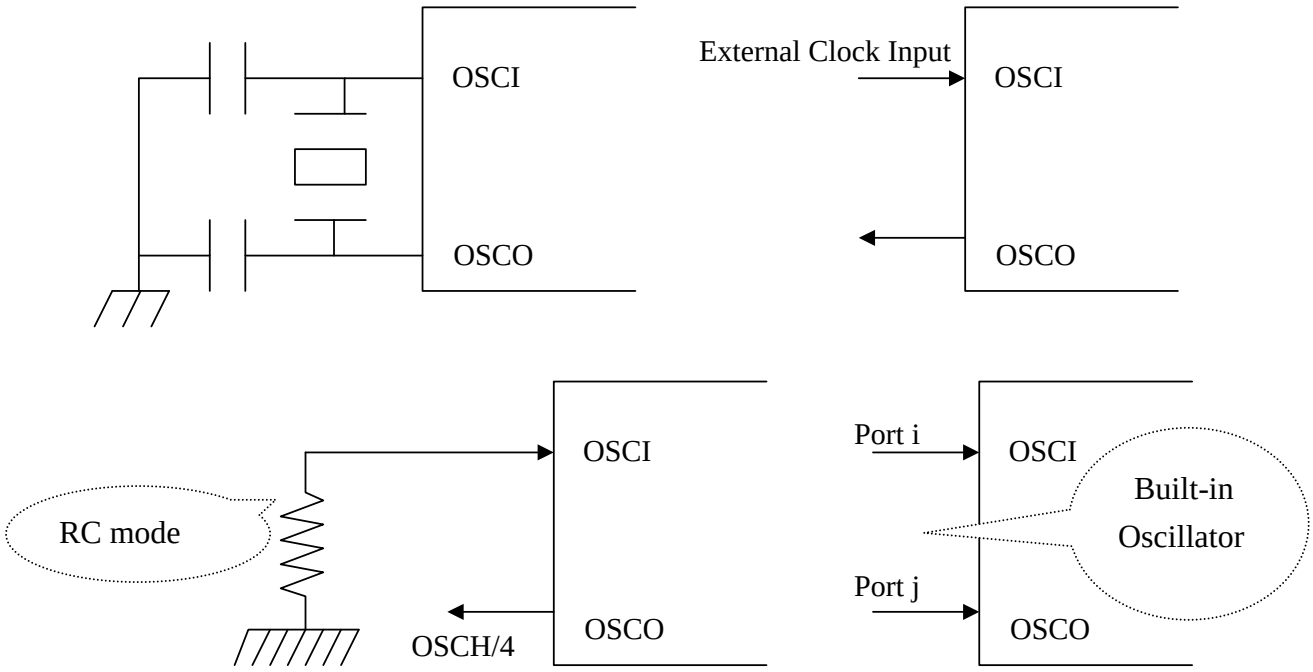


Figure: High Speed System Oscillator (OSCH)

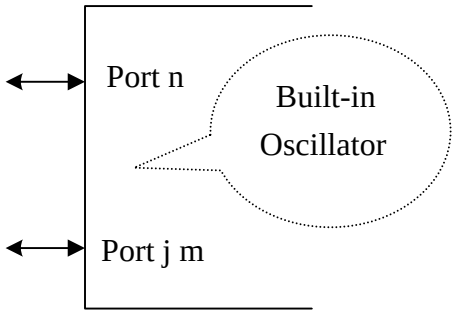
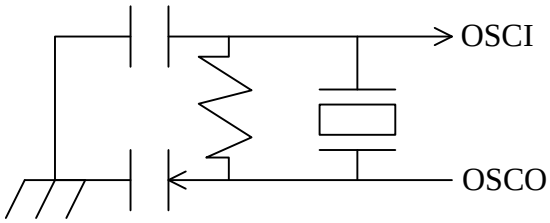


Figure: Low Speed Oscillator (OSCL)

A reference value of external components in crystal or resonator oscillator list in below table. OST0 is resonator or crystal oscillator stable time.



Resonator	Capacitor	Resister	5V OST0	3V OST0
< 1 M Hz	100pF	800kΩ	<8ms	<2ms
	20pF	-	<35ms	<20ms
	-	-	<200ms	<30ms
1 MHz	20pF	700KΩ	<25ms	<10ms
	-	-	<150ms	<15ms
2 MHz	20pF	600KΩ	<5ms	<3ms
	-	-	<10ms	<5ms
2 MHz<OSC<=4 MHz	10pF	500KΩ	<2ms	<1ms
	-	-	<5ms	<2ms
< 4 MHz	10pF	400KΩ	<1ms	<0.5ms
	-	-	<2ms	<1ms

Crystal	Capacitor	Resister	5V OST0	3V OST0
1 MHz	20pF	700KΩ	<25ms	<10ms
	-	-	<150ms	<15ms
2 MHz	20pF	600KΩ	<5ms	<3ms
	-	-	<10ms	<5ms
2MHz<OSC	10pF	500KΩ	<2ms	<1ms
	-	-	<5ms	<2ms

Note:

0. Built-in crystal or resonator oscillator feedback resister is about 600KΩ.
1. Different component value causes differed oscillator stable time.
2. If oscillator stable time < system OST, CPU will get abnormal.

S-4: Power saving mode (Stop mode & Sleep mode)

The CPU enters stop or sleep mode is operated by writing CPU power saving register (PS). During the power saving mode, CPU holds the internal status of the system. In stop mode, the oscillator clocks will be stopped and system need a warm-up time for the stability of system clock running after wake up.

S-5: MCU System Operation Modes

The MCU has 4 operating modes, including high speed operation, low speed operation, sleep & stop modes. After power on reset, the MCU will go into high speed operation mode automatically. After wake up from stop/sleep mode, the MCU will resume the last operation mode.

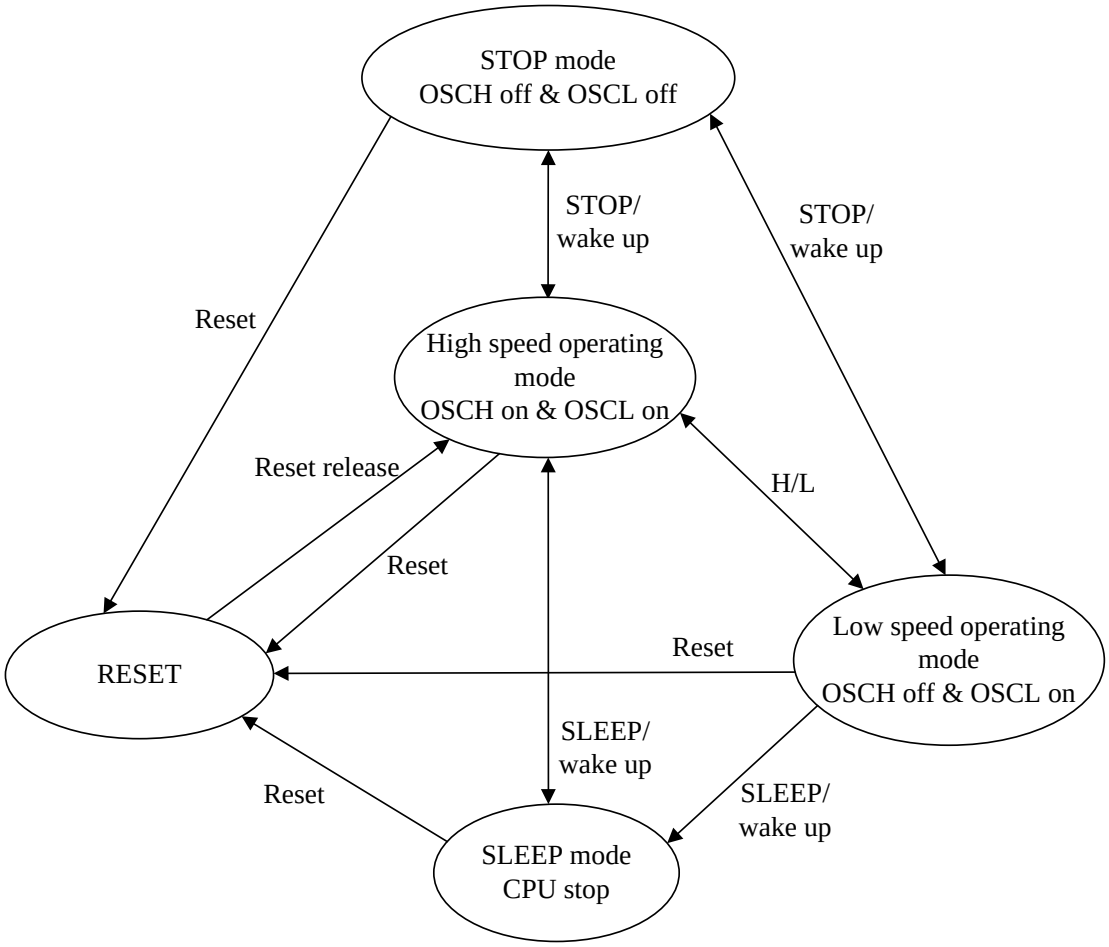


Figure: System Operation State Diagram

* Power saving mode condition & Release

Modes	Stop mode	Sleep mode
High speed oscillator	Stopped	Stopped as H/L=0
High speed oscillator	Stopped	Keep Operating
CPU clock	Stopped	Stopped
CPU internal status	Stop & Retain the status	
Memory, Flag, Register, I/O	Retain the status	
Program counter	Hold the next executed address	
Peripherals: Time base, Timers, Interrupts	Stopped & Retain (Vref off)	Keep Operating
Watch Dog Timer	Disable & cleared	
Release Condition	Reset, external INT, Input wake-up	Reset, external and internal INT sources, Input Wake-up

S-6: Watch Dog Timer (WDT)

The clock of watch dog timer comes from time base overflow (TB1_1OV). If time base frequency select 8KHz or 1KHz, watch dog timer's clock is switch to 64Hz. User can use the time up signal to prevent a software malfunction or abnormal sequence from jumping to an unknown memory location causing a system fatal failure. Normally, if the watchdog timer time up signal active that will reset the chip. At the same time, program and hardware can be initialized and resume system under normal operation. The chip also provides 2 steps clear watchdog command as the programmer writes INTAF with $F data first that will enable the WDT clear, and then writes the power saving (PS) control register after. Completely finishes the two write & read steps will clear the watch dog timer. User should well arrange the two command steps for avoiding the dead lock loop.

User should keep in minds that always reset WDT at main program and never clear the WDT in the interrupt routine.

The max period of WDT =(TB1_1OV cycle time) * 7

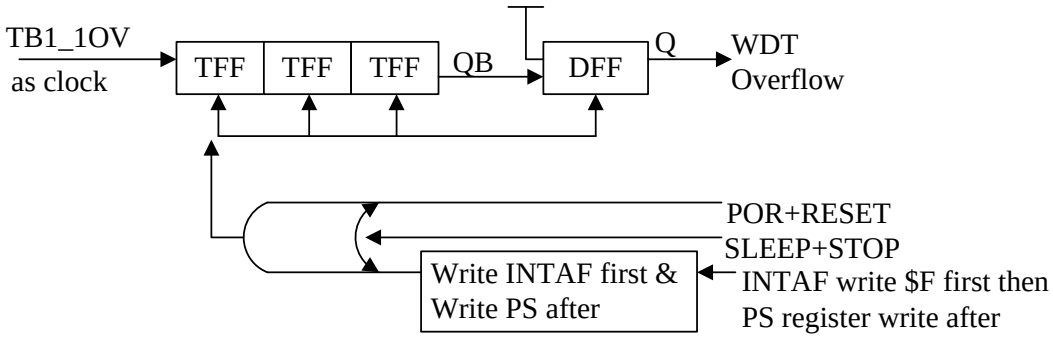


Figure: Watch Dog Timer control circuit

S-7: Low Voltage Reset (LVR)

a. **Low Voltage Reset (LVR)**

The low voltage reset (LVR) forces the MCU in reset state during power failure, especially as MCU working in AC power application, preventing from abnormal state is the key issue. The control bit LVREN in power saving control register (PS) is for power saving. The detected voltage locates at 2.2V or 3.0V

S-8: RESET

The chip has four kinds of reset sources: POR (power on reset), External reset, Watch dog timer reset, LVR (low voltage reset). Reset will initialize the CPU and peripheral device with default state.

.POR (power on reset)

The chip provides automatic reset function when the power is turned on. The VDD should be below 1.6V and its rising slope (from 0.1VDD up to o.9VDD) needs less than 10ms.

.External Reset (RSTB)

This is one kind of system resetting signal, but only forced externally. When the chip acknowledged the low level from the pin RSTB exceed 1 us, it will generate the reset procedure to reset CPU & all the peripheral back to their initial state (default values).

.Burn out Reset (Program sequence abnormal)

As CPU out of program area, the CPU can detect the abnormal condition and generate a system reset request.

.Watch Dog Timer Reset

The reset signal will generate automatically when the watchdog timer runs overflow. If the watchdog timer is cleared regularly by users' program, no watchdog reset will occur. Unless the MCU is forced into abnormal state, the software controlled procedure is disrupted and causing watch dog timer overflow, then it will generate reset signal to initializes the chip returning to normal operation.

.Low Voltage Reset (LVR)

The LVR function is used to monitor the supply voltage of MCU, it will generate a reset signal (with 4*OSCL de-bounce time but no de-bounce in stop mode) to reset the microcontroller as the VDD power falls below the default setting level V_{LVR}. It can also be enabled or disabled by programming "LVREN" bit in PS register.

✧ RESETF: Reset source flag register[R/W], power on value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	ROMF	BOF	LVRF	WDTF
Read/Write	RW	R/W	R/W	R/W

WDTF: Watch dog timer overflow reset flag (0: no active; 1: active)

LVRF: Low voltage reset flag (0: no active; 1: active)

BOF: Burn out flag(0: no active; 1: active)

ROMF: ROM fail flag(0: no active; 1: active)

(The RESETF is cleared by system reset only)

S-9. Power saving control register

✧ PS: Power saving register[R/W] , default [1100]

PS register	Bit3	Bit2	Bit1	Bit0
Bit Name	LVREN	H/L	CPUA SLP	STOP
Read/write	R/W	R/W	R/W	R/W

STOP: Into stop mode. (0: inactive; 1: active)

CPUA SLP: CPUA Into sleep mode. (0: inactive; 1: active)

H/L: System clock selection. (1: System clock; 0: peripheral clock)

LVREN: low voltage reset enable,(0:disable, 1:enable)

As writing PS register system also clear watch dog timer counter.

The SLEEP & STOP bits will be cleared to "0" automatically, when the release conditions occur from reset, interrupt or input wake up.

✧ PSP: Peripheral power saving register[R/W] , default [0000]

PSP register	Bit3	Bit2	Bit1	Bit0
Bit Name	LDOEN	PFD2EN	PFD1EN	CPUB SLP
Read/write	R/W	R/W	R/W	R/W

PFD1EN: PFD1 & PFD1B output enable (0: disable; 1: enable)

PFD2EN: PFD2 & PFD2B output enable (0: disable; 1: enable)

CPUB SLP: CPUB sleep mode (0: inactive; 1: active)

LDOEN: LDO enable (0: inactive; 1: active)

The system oscillator generates the system control timing for CPU core or peripheral devices with fixed control phase, so the waveform of oscillator becomes sensitive to noise, abnormal duty especially fatal for CPU. Any switching of clock source needs oscillation stable time (OST) to make sure the oscillation is stable and synchronized with CPU timing phase. The relative OST for different oscillator with reference value as below table:

S-10. Interrupts

The dual CPU provides 2 interrupt vector ($001H & $003H) and no priority, but can expand to multi-sources. Interrupt source includes external interrupts (INxTx), timer/counter interrupts (TCPxINT), Time base timer interrupt (TBxINT) or other peripheral device interrupt request (PERINT). The interrupt control registers (INTxC or INTxCx) contain the interrupt control bits to enable and disable corresponding interrupt request and the corresponding interrupt request flags in the (INTxF or INTxFx) registers. Before finishing the INT service routine, another INT request will keep waiting until program return from interrupt routine.

OST		From Stop state	oscillating	Unit
System clock (OSCH)	RC	4	4	OSCH clock
	Crystal / Resonator	4	4	
Peripheral clock(OSCL)	RC	4	4	OSCL clock

✧ INTAC: Interrupt control register for CPUA [R/W], default [0000]

INTC	Bit3	Bit2	Bit1	Bit0
Bit Name	TB1_2-IEA	TCP2-IEA	TCP1-IEA	TB1_1-IEA
Read/Write	R/W	R/W	R/W	R/W

TB1_1-IEA：Enable time base1 1st interrupt. (0: disable; 1: enable)

TCP1-IEA: Enable interrupt of timer/counter 1. (0: disable; 1: enable)

TCP2-IEA: Enable interrupt of timer/counter 2. (0: disable; 1: enable)

TB1_2-IEA: Enable time base1 2nd interrupt. (0: disable; 1: enable)

✧ INTBC: Interrupt control register for CPUB [R/W], default [0000]

INTC	Bit3	Bit2	Bit1	Bit0
Bit Name	TB2_2-IEB	TCP2-IEB	TCP1-IEB	TB2_1-IEB
Read/Write	R/W	R/W	R/W	R/W

TB2_1-IEB: Enable time base2 1st interrupt. (0: disable; 1: enable)

TCP1-IEB: Enable interrupt of timer/counter 1. (0: disable; 1: enable)

TCP2-IEB: Enable interrupt of timer/counter 2. (0: disable; 1: enable)

TB2_2-IEB: Enable time base2 2nd interrupt. (0: disable; 1: enable)

✧ INTAF: Interrupt request flag register for CPUA[R/W], default [0000]

INTF	Bit3	Bit2	Bit1	Bit0
Bit Name	TB1_2F	TCP2F	TCP1F	TB1_1F
Read/Write	R/W	R/W	R/W	R/W

TB1_1F: Time base1 1st interrupt request flag. (0: inactive; 1: active)

TCP1F: Timer/counter1 interrupt request flag. (0: inactive; 1: active)

TCP2F: Timer/counter2 interrupt request flag. (0: inactive; 1: active)

TB1_2F: Time base2 2nd interrupt request flag. (0: inactive; 1: active)

✧ INTBF: Interrupt request flag register for CPUB[R/W], default [0000]

INTF	Bit3	Bit2	Bit1	Bit0
Bit Name	TB2_2F	TCP2F	TCP1F	TB2_1F
Read/Write	R/W	R/W	R/W	R/W

TB2_1F: Time base2 1st interrupt request flag. (0: inactive; 1: active)

TCP1F: Timer/counter1 interrupt request flag. (0: inactive; 1: active)

TCP2F: Timer/counter2 interrupt request flag. (0: inactive; 1: active)

TB2_2F: Time base2 2nd interrupt request flag. (0: inactive; 1: active)

✧ INTAC1: Extended interrupt control register for CPUA [R/W], default [0000]

INTC1	Bit3	Bit2	Bit1	Bit0
Bit Name	CPUF2-IEA	CPUF1-IEA	INT1F-IEA	INT0F-IEA
Read/Write	R/W	R/W	R/W	R/W

INT0F-IEA：INT0 external interrupt request enable. (0: disable; 1: enable)

INT1F-IEA：INT1 external interrupt request enable. (0: disable; 1: enable)

CPUF1-IEA：Software interrupt1 request enable. (0: disable; 1: enable)

CPUF2-IEA：Software interrupt2 request enable. (0: disable; 1: enable)

✧ INTBC1: Extended interrupt control register for CPUB [R/W], default value [0000]

INTC1	Bit3	Bit2	Bit1	Bit0
Bit Name	CPUF2-IEB	CPUF1-IEB	INT1F-IEB	INT0F-IEB
Read/Write	R/W	R/W	R/W	R/W

INT0F-IEB：INT0 external interrupt request enable. (0: disable; 1: enable)

INT1F-IEB：INT1 external interrupt request enable. (0: disable; 1: enable)

CPUF1-IEB：Software interrupt1 request enable. (0: disable; 1: enable)

CPUF2-IEB：Software interrupt2 request enable. (0: disable; 1: enable)

✧ INTF1: Interrupt request1 flag register [R/W], default value [--00]

INTF1	Bit3	Bit2	Bit1	Bit0
Bit Name	---	---	INT1F	INT0F
Read/Write	---	---	R/W(0)	R/W(0)

INT0F: INT0 external interrupt request flag. (0: inactive; 1: active)

INT1F: INT1 external interrupt request flag. (0: inactive; 1: active)

✧ INTF2: Interrupt request2 flag register [R/W], default value [00--]

INTF2	Bit3	Bit2	Bit1	Bit0
Bit Name	CPUF2	CPUF1	---	---
Read/Write	R/W	R/W	---	---

CPUF1,2: software interrupt request flag. (0: inactive; 1: active)

CPUF1 & CPUF2 for software set/clear so read & write (both of 0 & 1).

INT0F & INT1F with mask option for trigger type

INTS1 INTS0	Trigger type
00	Low active
01	Falling edge
10	Rising edge
11	Dual edge trigger

If the interrupt request needs service, the programmer may set the corresponding INT enable bit to allow interrupt active. External interrupts are triggered by falling edge trigger and set the related interrupt request flag (INTxF). The internal timer/counter interrupt is setting the TCPxF to 1, resulting from the timer/counter overflow. The time base interrupt TBxINT was provided 2 periodic interrupt request cycles for user operating a periodic routine.

When the corresponding interrupt enable and flag bits is set to 1, the CPU will active the interrupt service routine. Then CPU reads the service flag and check the request priority then proceeds with the relative interrupt service. After CPU writes the corresponding bits to 0 in the INTxF register, the service flag will be cleared to 0(using STX #n,$m instruction). The INTF & INTF1 registers' bit can only write "0" to clear the flag. User writes "1" to Flag bit with no effect.

✧ TPINTC :Touch pad interrupt enable register [R/W], default value [00--]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTIE	TPCMPIE	---	---
Read/Write	R/W	R/W	---	---

TPCTIE: Duty counter overflow interrupt enable.

TPCMPIE: Capacitor overcharge interrupt enable.

✧ TPINTF :Touch pad interrupt request register [R/W], default value [00--]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TPCTF	TPCMPF	---	---
Read/Write	R/W	R/W	---	---

TPCTIE: Duty counter overflow interrupt enable.

TPCMPIE: Capacitor overcharge interrupt enable.

§ Peripheral function description:

P-1: System clock pre-scale

The system clock almost is the most high frequency of MCU. For various peripherals, application needs different clock source divided from system clock. TCPFS register is a selector for choosing suitable frequency (FS).

✧ TCPFS: System clock pre-scale register[R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	FS2	FS1	FS0
Read/Write	-	R/W	R/W	R/W

FS2~FS0: the selector value of TCPFS register

FS2 ~ FS0	FS	FS2 ~ FS0	FS
0	OSCH/1	4	OSCH/16
1	OSCH/2	5	OSCH/32
2	OSCH/4	6	OSCH/64
3	OSCH/8	7	OSCH/128

P-2: Time Base Counter

The time base counter has 2 interrupt sources and both of them come from the peripheral internal RC oscillator or external RTC optioned by mask option. The time base1 & 2 1st overflow output (TB1_1OV &TB2_1OV) can cause interrupt and the period is selected by TB1_1S2~TB1_1S0 in TB1C register and TB2_1S2~TB2_1S0 in TB2C register. The time base1 & 2 2nd frequency (TB1_2OV &TB2_2OV) also offers two sample frequency options by TB1_2S bit in the TB1C register & TB2_2S bit in the TB2C register.

✧ TB1C: Time base1 control register[R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TB1_2S	TB1_1S2	TB1_1S1	TB1_1S0
Read/Write	R/W	R/W	R/W	R/W

TB1_1S2 ~ TB1_1S0: Base timer1 1st overflow frequency selection bits.

TB1_2S: Base timer1 2nd overflow frequency select bit. (0: 256Hz; 1:64Hz)

(Every time writing the TBCC will clear the time base counter)

TB1_2S	TB1_2OV
0	256Hz (TBCK/64)
1	64Hz (TBCK/256)

TB1_1S2	TB1_1S1	TB1_1S0	**Base timer overflow frequency (TB1OV)**	TBCK = 16K **TB1_1OV**
0	0	0	TBCK/2	8K HZ
0	0	1	TBCK/16	1K HZ
0	1	0	TBCK/256	64 HZ
0	1	1	TBCK/512	32 HZ
1	0	0	TBCK/1024	16 HZ
1	0	1	TBCK/2048	8 HZ
1	1	0	TBCK/8192	2 HZ
1	1	1	TBCK/16384	1 HZ

✧ TB2C: Time base2 control register for CPUB[R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TB2_2S	TB2_1S2	TB2_1S1	TB2_1S0
Read/Write	R/W	R/W	R/W	R/W

TB2_1BS2 ~ TB2_1BS0: Base timer2 1st overflow frequency selection bits.

TB2_2BS: Base timer2 2nd overflow frequency select bit. (0: 256Hz; 1:64Hz)

TB2_2S	TB2_2OV
0	256Hz (TBCK/64)
1	64Hz (TBCK/256)

TB2_1S2	TB2_1S1	TB2_1S0	**Base timer overflow frequency (TB1OV)**	TBCK = 16K **TB2_1OV**
0	0	0	TBCK/2	8K HZ
0	0	1	TBCK/16	1K HZ
0	1	0	TBCK/256	64 HZ
0	1	1	TBCK/512	32 HZ
1	0	0	TBCK/1024	16 HZ
1	0	1	TBCK/2048	8 HZ
1	1	0	TBCK/8192	2 HZ
1	1	1	TBCK/16384	1 HZ

P-3: 8 bits Timer/Counter/PFD (TCP) for TCP1, 2

One 8-bits timer/counters/PFD (TCP) with 4 kind clock sources and preload data buffer can implement as a timer or counter feature , PFD is programmable frequency divider can support sound /melody/carrier generator. The clock sources of TCP are selected by TCPS0 & TCPS1 two bits of the timer control registers (TCPC). TCPOV is the timer or counter overflow signal and the rising edge will set the relative INT flag.

✧ TCPC: Timer/counter/PFD control register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPLD	TCPS1	TCPS0	TCPEN
Read/Write	R/W	R/W	R/W	R/W

TCPEN: TCP counting enabled. (0: disable; 1: enable)

TCPLD: TCP auto-reload enabled. (0: disable; 1: enable)

TCPS1 & TCPS0: TCP clock source selection bits.

TCPS1	TCPS0	Selected Clock source
0	0	CK0
0	1	CK1
1	0	CK2
1	1	CK3

✧ TCPDL: TCP low nibble data register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP3/TCPD3	TCP2/TCPD2	TCP1/TCPD1	TCP0/TCPD0
Read/Write	R/W	R/W	R/W	R/W

TCP3~TCP0: Reading the counter low nibble data.

TCPD3~TCPD0: Writing TCPD low nibble of data buffer.

✧ TCPDH: TCP high nibble data register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCP7/TCPD7	TCP6/TCPD6	TCP5/TCPD5	TCP4/TCPD4
Read/Write	R/W	R/W	R/W	R/W

TCP7~TCP4: Reading the counter high nibble data.

TCPD7~TCPD4: Writing TCPD high nibble of data buffer.

✧ TCPD: Like a 8 bit TCP data register[R/W], default value [00H]

TCPD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPD7	TCPD6	TCPD5	TCPD4	TCPD3	TCPD2	TCPD1	TCPD0

The special R/W function for TCP has different Target, AS writing TCPH/L registers that are updating preload data of the TCPD. As read TCPH/L registers that are the brand new TCP counter value.

.Timer

When TCP works as a Timer, user needs give the preload data TCPD for periodic interrupt. After initial setting, user starts the TCP counting by setting TCPEN=1, the TCP cycle period is:

Tc = (selected clock cycle) * (TCPD)

When user writes data to the TCPD, the data just keep in TCPDL/H register. During the TCPEN=1 command executed, the TCPD 1's complement value will load into counter TCP as initial value and start the timer function. Necessary TCPLD=1, timer run with reload feature as TCP up counts and reaches the value 0f "FF_H" or 255. At the same time, interrupt request flag TCPF will set activated, if software enables the corresponding interrupt enable bit, INT hardware will cause MCU interrupt service routine.

.PFD

The PFD Mode includes in timer mode and the output frequency is:

PFD frequency = (selected clock frequency) / (2) / (TCPD)

At this time, most users will disable the interrupt feature for tone or melody generation.

.Counter

Counter feature is implemented only by TCPLD=0, the TCPD can be zero or not that depends on software needs. User starts & stops the counter by changing the TCPEN bit value. On the save side, reading the counter value after stopping the count by disable TCPEN=0, if reading the counter value during value changing that means clock in happening at the same time. The reading of counter value may disrupt for transient state. If 8 bit counter is not enough for counting, user can enable the interrupt and using the data RAM as software counter for extending the counter stage.

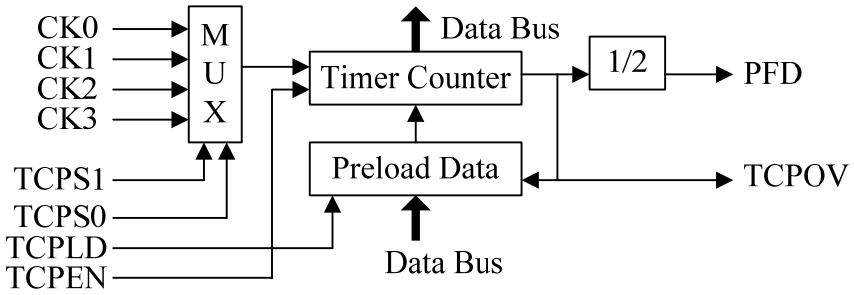


Figure: Timer/Counter/PFD

TCPS1	TCPS0	TCP 1	TCP 2
0	0	FS	FS
0	1	TCP1I	TB2_1OV
1	0	TBCK	TBCK
1	1	TB1_1OV	TCP1OV

	PFD Output
TCP 1	PFD1
TCP 2	PFD2

FS: System scaled frequency.

TB1_1OV: Time base 1st overflow output.

TB2_1OV: Time base 2st overflow output.

TCP1OV: Timer/counter 1' overflow output.

TBCK: Peripheral clock source, 16KHZ in the RTC mode.

TCP1I: External input clock from pad shared with IO Port .

PFD1: TCP1 cycle time/2 output signal

PFD2: TCP2 cycle time/2 output signal

. 16 bits Timer/Counter/PFD (TCP)

Two sets TCP can be cascaded to form a 16-bit timer/counter when 2nd TCP chooses 1st TCPOV as clock source (TCPS1=1 & TCPS0=1). In the 16-bit timer application, data load is controlled by writing TCPEN=1 of 1stTCP, then user should enable the TCPEN of 2nd TCP at first, then using TCPEN of 1st TCP to control the starting or stopping counting of 16-bit timer/counter. The rising TCPOV of 2nd TCP will reload the contents in the pre-load register into timer/counter, if TCPLD in TCPC of 1st & 2nd TCP are enabled. The interrupt feature keeps the same, but in this case, user disable the 1st TCP INT and enable 2nd TCP is normally setting.

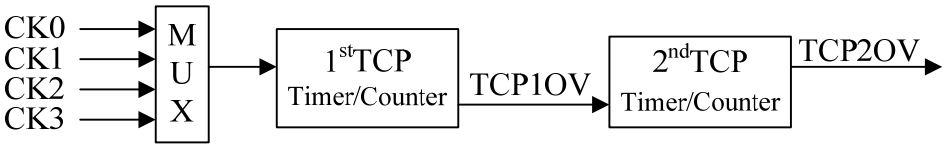


Figure: 16 Bite Timer/Counter Configuration

. I/O PAD Cell Structure & Function Description

.. Input Port

The input port can mask option with pull high resistor and input data can read by port reading command. As mask option with pull-up resister then a wake-up function also offers the system wake up feature for keys or special external triggers.

Input Data	Pull-high	Read Data	Wake-up
0	R	**0**	**Active**
0	No	**0**	**Inhibited**
1	R	**1**	**Non-active**
1	No	**1**	**Inhibited**
Floating	R	**1**	**Non-active**
Floating	No	**?**	**Inhibited**

R: Mask option with pull-up resistor

X: Don't care the value

?: Unknown

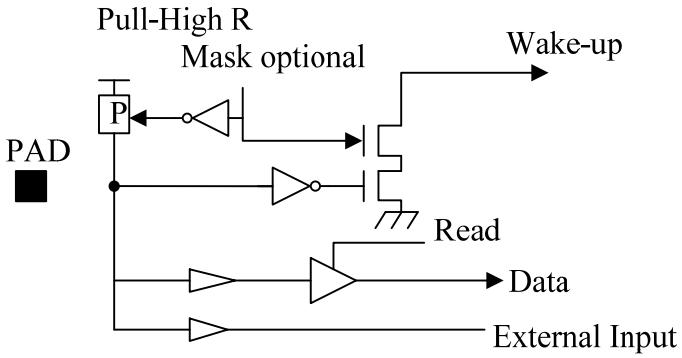


Figure IO-E: Input Port

.. IO Port with external input

The input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. Software can performs a configuration (data=0, changing the control 0 or 1) for open drain type that specifies suitable for key scan application. An additional feature supports the interrupt input triggers and Timer external clock sources.

I/O control Data	Output data	Pull-up R	Wake-up feature	External inputs
0	X	**No**	**No**	**No**
1	0	**No**	**No**	**Enable**
1	1	**Enable**	**Enable**	**Enable**

X: don't care the value

I/O control Data	MODE	PAD
0	**Output mode**	**Output Register data Q**
1	**Input mode**	**Input data**

Read PI	Read Input Data
0	**Output Register data Q**
1	**PAD input data**

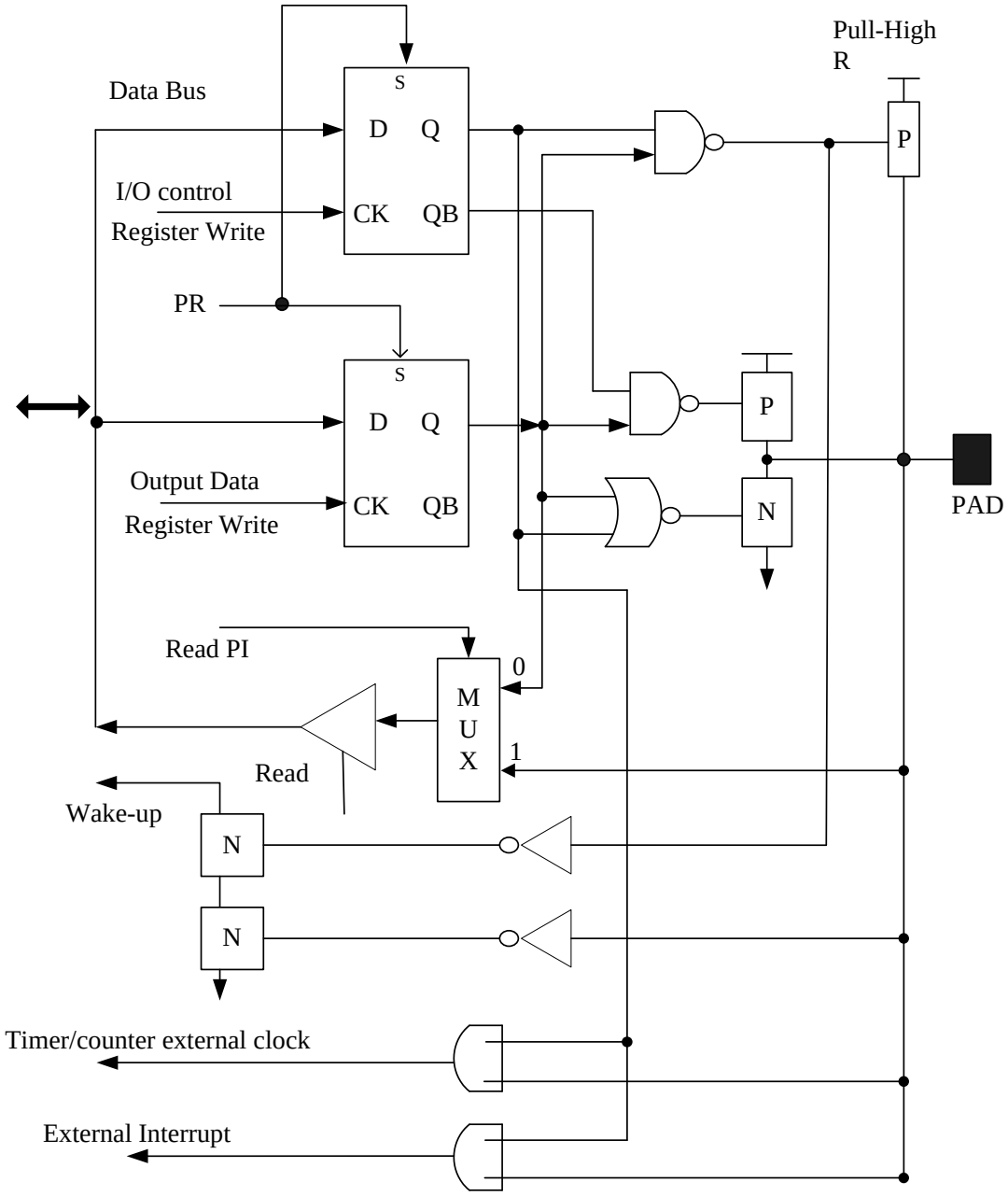


Figure IO-A: Standard IO Port with wake-up/interrupt/timer clock inputs

.. I/O port with internal output

The standard input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. If enable internal output by mask option, the internal output will control by output data (on/off) and outputs to PAD.

I/O control Data	Output data	Pull-up	Wake-up
0	X	**No**	**No**
1	0	**No**	**No**
1	1	**Enable**	**Enable**

X: don't care the value

I/O control Data	Internal output	PAD
0	enable	**Output Register data Q*internal data**
0	disable	**Output Register data**
1	X	**PAD input data**

X: don't care the value

Read PI	Mode	Read Input Data
0	**Output**	**Output Register data Q**
1	**Input**	**PAD input data**

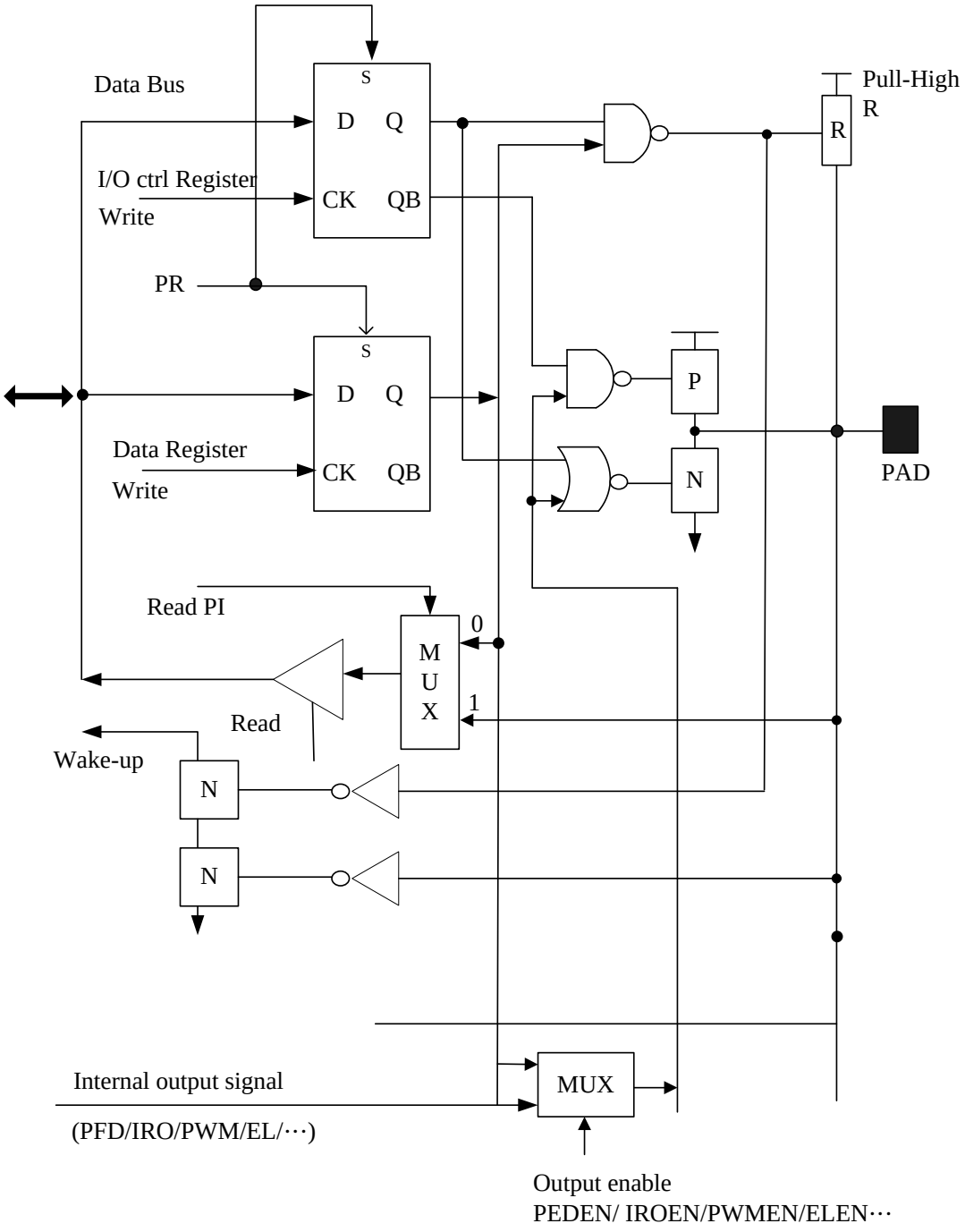


Figure IO-B: Standard I/O Port with internal output signal

.. Standard IO Port

The standard input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. Software can performs a configuration (data=0, changing the control 0 or 1) for open drain type that specifies suitable for key scan application.

I/O control Data	Output data	Pull-up	Wake-up
0	X	**No**	**No**
1	0	**No**	**No**
1	1	**Enable**	**Enable**

X: don't care the value

I/O control Data	MODE	PAD
0	**Output**	**Output Register data Q**
1	**Input**	**Input data**

Read PI	Read Input Data
0	**Output Register data Q**
1	**PAD input data**

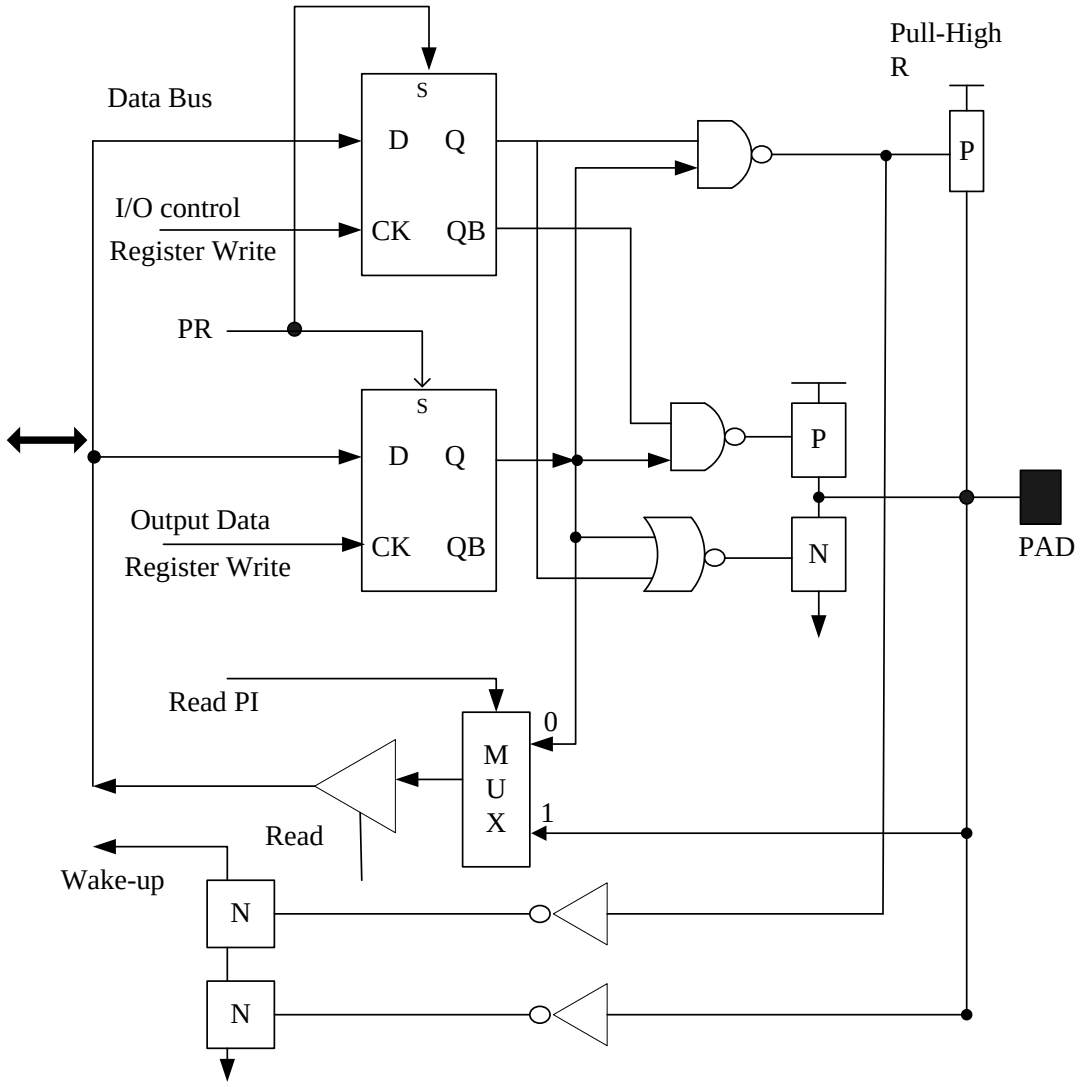


Figure IO-C: Standard IO Port

.. I/O port with internal output & external input

The standard input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. If enable internal output by mask option, the internal output will control by output data (on/off) and outputs to PAD.

I/O control Data	Output data	Pull-up	Wake-up
0	X	**No**	**No**
1	0	**No**	**No**
1	1	**Enable**	**Enable**

X: don't care the value

I/O control Data	Internal output	PAD
0	enable	**Output Register data Q*internal data**
0	disable	**Output Register data**
1	X	**PAD input data**

X: don't care the value

Read PI	Mode	Read Input Data
0	**Output**	**Output Register data Q**
1	**Input**	**PAD input data**

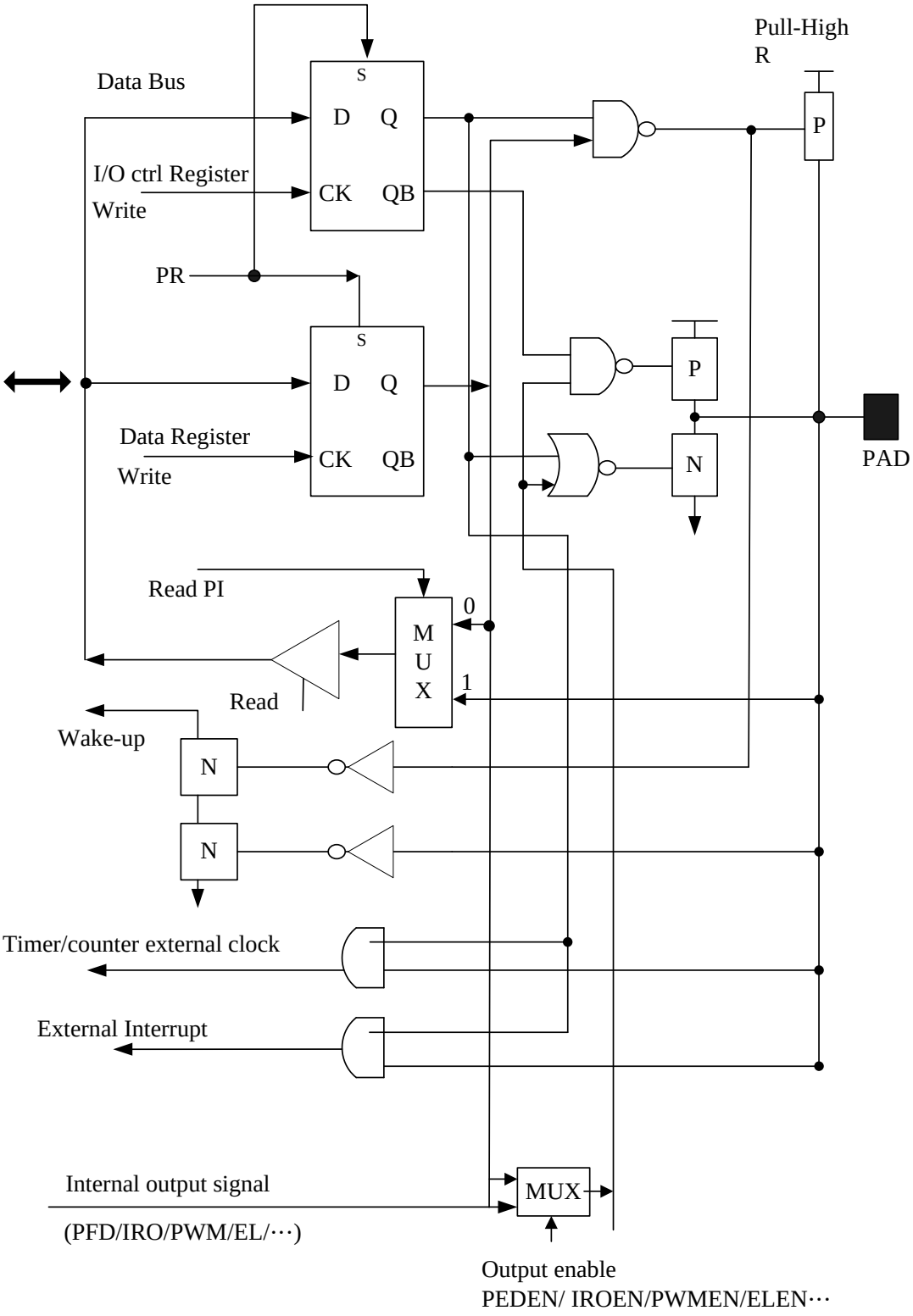


Figure : Standard I/O Port with internal output signal & external

.. LCD Output driver SEGMENT & COMMON

LCD segment and common drivers are controlled by internal timing, and LCD RAM stored the display data is dumped automatically by bit mapping type.

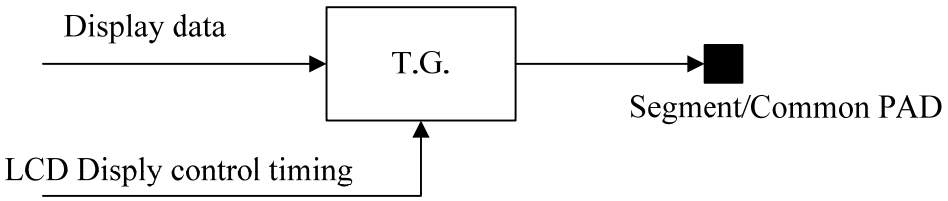


Figure LCD-A: LCD Segment/Common Driver Output

IO Pad Cells

The main features of pad cell are including ESD/EFT protection and general I/O access. A general I/O pad cell can be configured as input with or without pull-up resistor, or working as a CMOS or NMOS output driver. The input pad cell must have pull-up resistor for avoiding a floating state when user doesn't care or not be used. For concerning the standby current, user can use data register or I/O control register to fit the application.

. I/O File Register

✧ PAC: Port A I/O control register [R/W], default value [1111]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PAC3	PAC2	PAC1	PAC0
Read/Write	R/W	R/W	R/W	R/W

PAC3~PAC0: Port A' I/O control register.

Special note : PA0 output driving capability, sink=2mA, source=1mA

✧ PA: Port A data register [R/W], default value [1111]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PA3	PA2	PA1	PA0
Read/Write	R/W	R/W	R/W	R/W

PA3~PA0: Port A' data register.

✧ PBC: Port B I/O control register [R/W], default value [1111]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PBC3	PBC2	PBC1	PBC0
Read/Write	R/W	R/W	R/W	R/W

PBC7~PBC0: Port B I/O control register.

✧ PB: Port B data register [R/W], default value [1111]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PB3	PB2	PB1	PB0
Read/Write	R/W	R/W	R/W	R/W

PB3~PB0: Port B data register.

✧ PCC: Port C I/O control register [R/W], default value [1111]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PCC3	PCC2	PCC1	PCC0
Read/Write	R/W	R/W	R/W	R/W

PCC3~PCC0: Port C I/O control register.

✧ PC: Port C data register [R/W], default value [1111]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PC3	PC2	PC1	PC0
Read/Write	R/W	R/W	R/W	R/W

PC3~PC0: Port C data register.

✧ PDC: Port D I/O control register [R/W], default value [1111]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PDC3	PDC2	PDC1	PDC0
Read/Write	R/W	R/W	R/W	R/W

PDC3~PDC0: Port D I/O control register.

✧ PD: Port D data register [R/W], default value [1111]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PD3	PD2	PD1	PD0
Read/Write	R/W	R/W	R/W	R/W

PD3~PD0: Port D data register.

✧ PE: Port E data register [R/W], default value [1111]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PE3	PE2	PE1	PE0
Read/Write	R/W	R/W	R/W	R/W

PE3~PE0: Port E data register.

✧ PF: Port F data address [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	----	----	PF1	PF0
Read/Write	----	----	R/W	R/W

PF1~PF0 :Port F data input.

✧ PAI: Port A pad data reading address [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PAI3	PAI2	PAI1	PAI0
Read/Write	R	R	R	R

PAI3~PAI0: port A' pad data

✧ PBI: Port B pad data reading address [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PBI3	PBI2	PBI1	PBI0
Read/Write	R	R	R	R

PBI3~PBI0: Port B' pad data

✧ PCI: Port C pad data reading address [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PCI3	PCI2	PCI1	PCI0
Read/Write	R	R	R	R

PCI3~PCI0: Port C' pad data

✧ PDI: Port D pad data reading address [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PDI3	PDI2	PDI1	PDI0
Read/Write	R	R	R	R

PDI3~PDI0: Port D' pad data

✧ PEI: Port E pad data reading address [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PEI3	PEI2	PEI1	PEI0
Read/Write	R	R	R	R

PEI3~PEI0: Port E' pad data

✧ PFI: Port F pad data reading address [R], default value [----]

Register	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Bit Name	PFI3	PFI2	PFI1	PFI0
Read/Write	R	R	R	R

PFI3~PFI0: Port F' pad data

TT-Bus Interface

· TT-Bus Registers

There are eight registers used in the TT-Bus interface, these are discussed in the following paragraphs.

*** TT-Bus Low Nibble Address Register (TTADRL)**, default [000-]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	AD3	AD2	AD1	-
Read/Write	R/W	R/W	R/W	-

AD3~AD1 are the slave address bits of the TT-Bus module.

*** TT-Bus Low Nibble Address Register (TTADRH)**, default [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	AD7	AD6	AD5	AD4
Read/Write	R/W	R/W	R/W	R/W

AD7~AD4 are the slave address bits of the TT-Bus module.

*** TT-Bus Control Register 1 (TTCR1)**, default [1---]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TXAK	-	-	-
Read/Write	R/W	-	-	-

TXAK – Acknowledge Enable

1(set) – Do not send acknowledge signal.

0(clear) – Send acknowledge signal at 9th clock bit.

If cleared, an acknowledge signal will be sent out to the bus at the 9th clock bit after receiving one byte of data. If set, no acknowledge signal response. This is an active low control bit.

*** TT-Bus Control Register 2 (TTCR2)**, default [00-0]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	IEN	IIEN	-	TX
Read/Write	R/W	R/W	-	R/W

IEN – TT-Bus Enable

1(set) – TT-Bus interface system enabled.

0(clear) – TT-Bus interface system disabled.

IIEN – TT-Bus interrupt Enable

1(set) – TT-Bus interrupt enabled.

0(clear) – TT-Bus interrupt disabled.

This bit enables the IIF (in TTSR) for TT-Bus interrupts.

TX – Transmit/Receive Mode Select

1(set) – TT-Bus is set for transmit mode.

0(clear) – TT-Bus is set for receive mode.

*** TT-Bus Status Register 1 (TTSR1)**, default [-001]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	SRW	IIF	RXAK
Read/Write	-	R	R/W	R

SRW – Slave R/W Select

1(set) – Read from slave from calling master.

0(clear) – Write to slave from calling master.

When IAAS is set, the R/W command bit of the calling address sent from the master is latched into this SRW bit. By checking this bit, the CPU can then select slave transmit/receive mode by configuring TX bit of the TT-Bus Control register 2.

IIF – TT-Bus Interrupt

1(set) – A TT-Bus interrupt has occurred.

0(clear) – A TT-Bus interrupt has not occurred.

When this bit is set, an interrupt is generated to the CPU if IIEN is set. This bit is set when one of the following events occurs:

1) Completion of one byte of data transfer. It is set at the falling edge of the 9th clock - ICF set.

2) A match of the calling address with its own specific address – IAAS set.

This bit must be cleared by software in the interrupt routine

RXAK – Receive Acknowledge

1(set) – No Acknowledge signal detected.

0(clear) – Acknowledge signal detected after 8 bits data transmitted.

If cleared, it indicates an acknowledge signal has been received after the completion of 8 bits data transmission on the bus. If set, no acknowledge signal has been detected at the 9th clock. This is an active low status flag.

* **TT-Bus Status Register 2 (TTSR2)**, default [000-]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	ICF	IAAS	IBB	-
Read/Write	R	R/W	R	-

ICF – Data Transfer Complete

1(set) – A byte transfer has been completed.

0(clear) – A byte is being transfer.

When ICF is set, the IIF (TT-Bus interrupt) bit is also set. A TT-Bus interrupt is generated if the IIEN bit is set.

IAAS – Addressed as Slave

1(set) – Currently addressed as slave.

0(clear) – Not currently addressed.

This IAAS bit is set when its own specific address (TT-Bus Address register) matches the calling address. When IAAS is set, the IIF (TT-Bus interrupt) bit is also set. An interrupt is generated if the IIEN bit is set. Then CPU needs to check the SRW bit and set its TX bit accordingly. Writing to the TT-Bus Control register 2 clears this bit.

IBB – Bus Busy

1(set) – TT-Bus busy.

0(clear) – TT-Bus idle.

This bit indicates the status of the bus. When a START signal is detected, IBB is set. When a STOP signal is detected, it is cleared.

* **TT-Bus Low Nibble Data I/O Register (TTDRL)**, default [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	D3	D2	D1	D0
Read/Write	R/W	R/W	R/W	R/W

D3~D0 are the low nibble bits of the TT-Bus module.

In transmit mode, data written into this register is sent to the bus automatically, with the most significant bit out first. In receive mode, reading of this register initiates receiving of the next byte data.

* **TT-Bus High Nibble Data I/O Register (TTDRH)**, default [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	D7	D6	D1	D0
Read/Write	R/W	R/W	R/W	R/W

D7~D4 are the high nibble bits of the TT-Bus module.

· Programming Considerations:

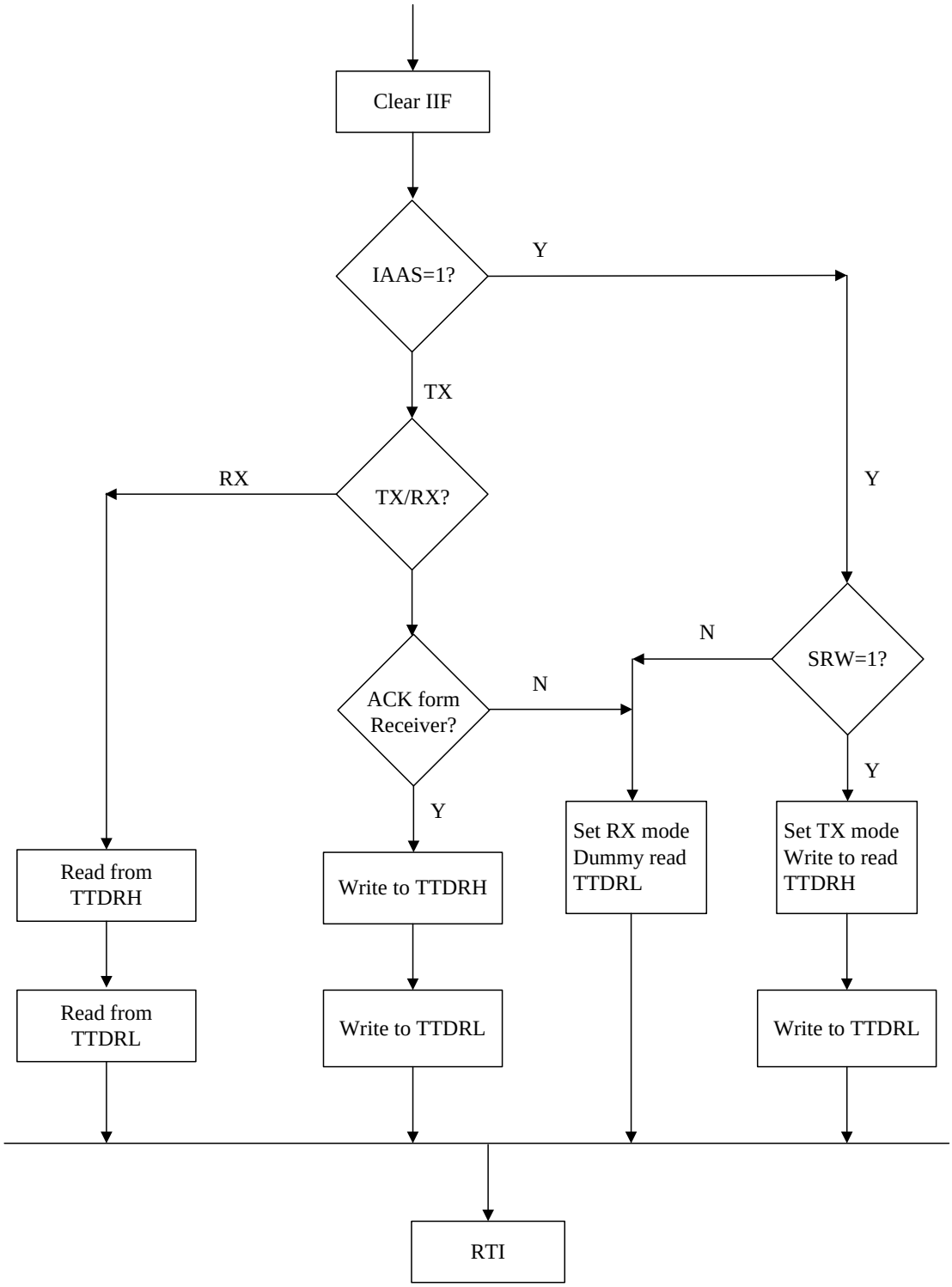


Figure.4 Flowchart of TT-Bus Interrupt Routine

§ Mask Option Table:

All the OTP mask option register can open for user to reset the initial value, but should enable the MRO. User writes MRO address first then changes the target mask option register data. The MRO enable will be cleared with other writing address.

✧ MOP0: Mask option register [R/W], default value [0000]

Mask option	Bit3	Bit2	Bit1	Bit0
Bit Name	INT1S1	INT1S0	INT0S1	INT0S0
Read/Write	R/W	R/W	R/W	R/W

✧ MOP1: Mask option register [R/W], default value [0000]

Mask option	Bit3	Bit2	Bit1	Bit0
Bit Name	PFD2B	PFD1B	OSCHS1	OSCHS0
Read/Write	R/W	R/W	R/W	R/W

✧ MOP3: Mask option register [R/W], default value [0000]

Mask option	Bit3	Bit2	Bit1	Bit0
Bit Name	PF3R	PF2R	IIC for A	
Read/Write	R/W	R/W	R/W	

✧ MOP4: Mask option register [R/W], default value [0000]

Mask option	Bit3	Bit2	Bit1	Bit0
Bit Name	LVREN	CPUFS1	CPUFS0	
Read/Write	R/W	R/W	R/W	

✧ MOP6: Mask option register [R/W], default value [---1]

Mask option	Bit3	Bit2	Bit1	Bit0
Bit Name	LDO VS	5V/3VB	-	-
Read/Write	-	-	-	-

The following table shows the mask option in this chip. All the mask options must be defined clearly and ensure to meet user's proper function.

No.	Mask Option	Function Descriptions	
+2	**High speed oscillator, OSCH**	00	RC built-in, Input port enable
	PF2~PF3 Input port	01	Crystal/resonator, External input
		10	R external adjustable
		11	RC built-in, Input port enable
+2	**INT1F trigger type**	00	Low level trigger
	INT1S1,INT1S0	01	Falling edge trigger
		10	Rising edge trigger
		11	Dual edge trigger
+2	**INT0F trigger type**	00	Low level trigger
	INT0S1,INT0S0	01	Falling edge trigger
		10	Rising edge trigger
		11	Dual edge trigger
+1	**PFD1B**	0	PFD1B output disable
		1	PFD1B output enable
+1	**PFD2B**	0	PFD2B output disable
		1	PFD2B output enable
+4	**PF2~PF3**	0	No pull-up resistor
	Pull-up resistor	1	With Pull-up resistor

Continuous -----

No.	Mask Option	Function Descriptions	
+1	**Power Supply option**	0	VDD=3V , pump
	3V/5V	1	VDD=5V , no pump
+1	**IIC function for CPUA/CPUB**	0	IIC function for CPUA
		1	IIC function for CPUB
+1	LVREN	0	LVR function disable
		1	LVR function enable
+1	LDO VS	0	LDO Voltage select 2.7V output
		1	LDO Voltage select 3.3V output
+2	Software interrupt select	00	F1 for CPUA call CPUB , F2 for CPUB call CPUA
		01	F1 for CPUA ,call CPUB, F2 for CPUB call CPUA
		10	F1 & F2 for CPUA call CPUB
		11	F1 & F2 for CPUB call CPUA

§ REVISION HISTORY：

2012/08/21：(Ver. 3.0) New build

2018/10/01：(Ver. 3.1) Modify Page 5 Top=-40℃ ~ +85℃