§ PATENTEN

1. PATENT：『電流源控制及補償觸控電容感測方法及其裝置』
   PAT NO. I339356 (Taiwan)
   PAT NO. ZL 2007 1 0202087. 0 (CHINA)
2. PATENT：『具環境變化校正的電容式觸控感測裝置』
   PAT NO. M383780 (Taiwan)
   PAT NO. ZL 2010 2 0141537. 7 (CHINA)
3. PATENT：『省電型多鍵觸摸開關感測裝置』
   PAT NO. M375250 (Taiwan)
   PAT NO. ZL 2010 2 0302392. 4 (CHINA)

§ General Description:

TTP259 MCU is an easy-used 4-bit CPU base microcontroller. It contains 4032-word ROM、384-nibble RAM、time base、timer/counter、interrupt service、IO control hardware、PWM output、IIC function、LVR and touch pad feature for specified applications. The device is also suitable for diverse simple applications in control appliance and consumer product.

§ Features:

1. Tontek RISC 4-bit CPU core
2. Total 26 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 CPU clocks) except read table instruction(RTB)
4. Advance CMOS process
5. Working memory with 4032*16 program ROM and 384*4 SRAM
6. 4-level stacks
7. Operating voltage: 2.4V~5.5V(LVR=2.2V); 3.3V~5.5V(LVR=3.0V); 2.2V~5.5V(LVR OFF)
8. System operating frequency: (at VDD=5V)
   . High speed system oscillator (OSCH)
   - ✧ Built-in RC oscillator: 4MHz(typical)

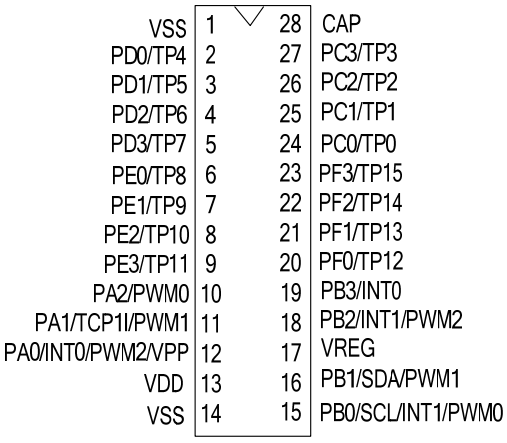
   . Low speed peripheral oscillator (OSCL)
   - ✧ Built-in RC oscillator: 16KHz(typical)
9. Provide 7 IO+16 touch pad or 23 general programmable IO
   - ✧ IO port built-in key wake-up feature enable by software setting
   - ✧ Provide external interrupt inputs
   - ✧ Provide internal signal outputs, like PWM

10. TWO time base
    - ✧ Time base offers 2 various period interrupt request
11. One 8-bit TCP1 auto-reload timer/counter
    - ✧ 4 timer clock sources selected by software
12. One 12-bit TCP2 auto-reload timer/counter, can improve PWM function
    - ✧ 4 timer clock sources selected by software
13. Built-in 3 set 12-bit PWM output
14. MCU system protection and power saving controlled mode
    - ✧ Built-in watch dog timer (WDT) circuit
    - ✧ Built-in low voltage reset (LVR) function
    - ✧ Out of user program's range detection
    - ✧ ROM code error detection
    - ✧ Provide high/low system operating speed, sleep and stop mode for power saving control
15. Provide 16 pins with touch pad detection
16. LDO voltage can select 2.7V or 4.2V output by mask option
17. LVR voltage can select 2.2V or 3.0V by mask option
18. Provide two wire serial interface (IIC-BUS)
19. Provide 10 interrupt sources
    - ✧ External: INT0, INT1 shared with IO pad
    - ✧ Internal: two time base, two timer/counter
    - ✧ Two touch pad's interrupt
    - ✧ Two IIC interrupt
20. Provide package types
    - ✧ 28SSOP/20TSSOP/16SOP

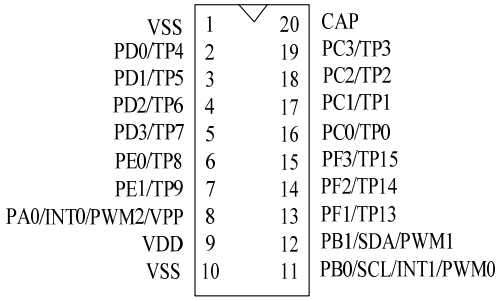
§ Applications:

1. Household electric appliances
2. Consumer products
3. Measurement controller

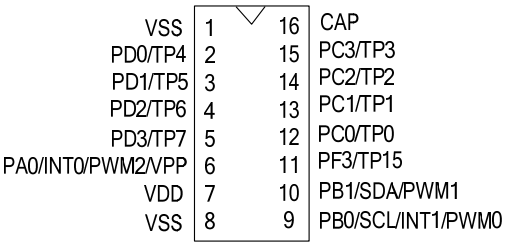
§ Package Description:



28SSOP-A

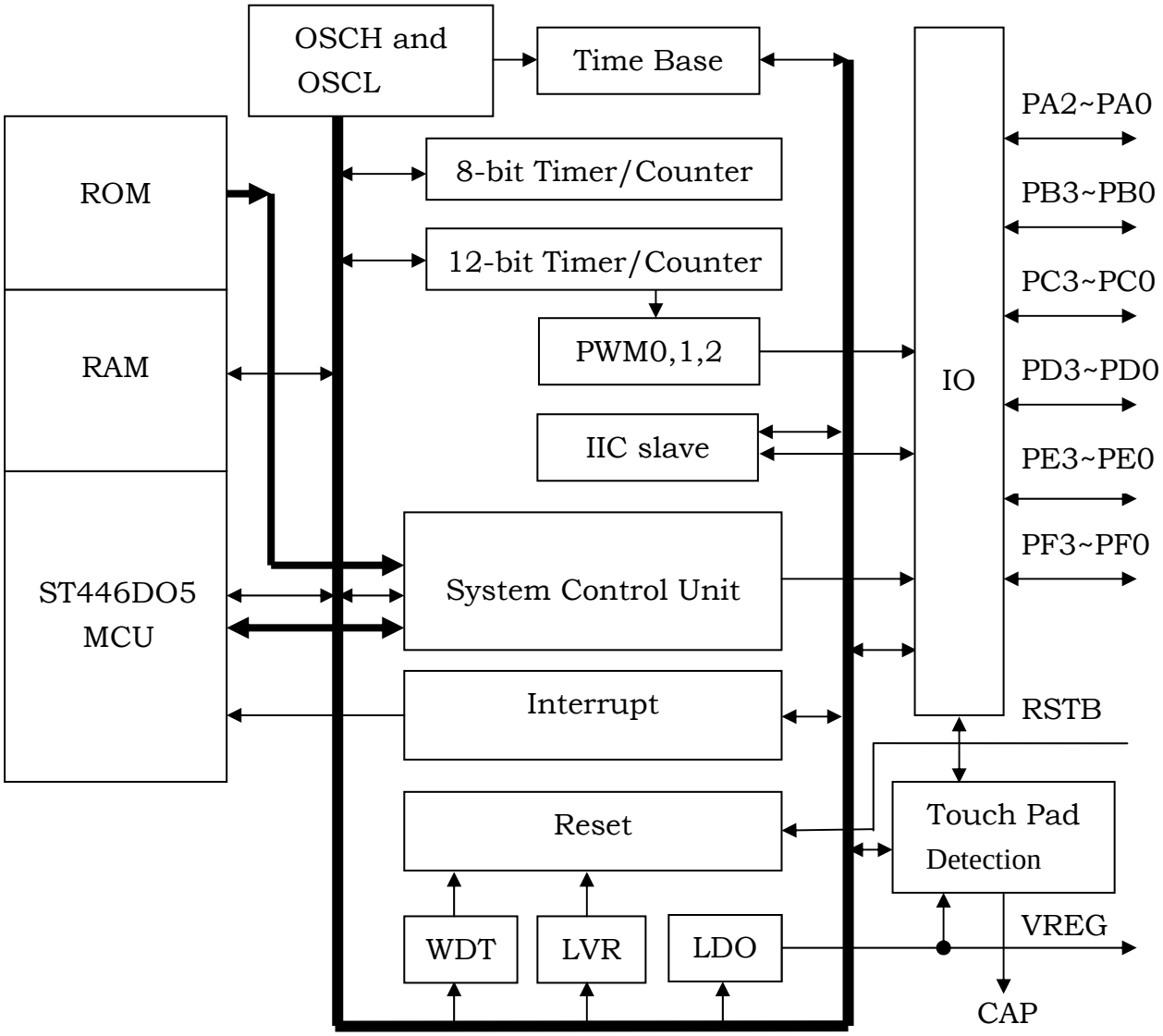


20TSSOP-B



16SOP-B

§ Block Diagram:



§ Pad Description:

Pad Name	Share Pad	IO	Pad	Mask Option	Pad Description
VDD	-	Power	+2	-	Positive power supply.
VSS	-	Power	+4	-	Negative power supply, ground.
RSTB	-	I	+1	-	External reset input, active low.
PA0 PA1 PA2	INT0/PWM2/VPP TCP1I/PWM1 PWM0	IO/I/O IO/I/O IO/O	+3	Yes	IO port with external interrupt input, external clock input and PWM output. PA0 is shared with external interrupt input, PA1 is shared with external clock input, PA0,PA1,PA2 is shared with PWM output.
PB0 PB1 PB2 PB3	SCL/INT1/PWM0 SDA/PWM1 INT1 INT0/PWM2	IO/I/O IO/O IO/I IO/I/O	+4	Yes	IO port with internal IICBUS, external interrupt input and PWM output. PB0,PB1 is shared with internal IICBUS, PB0,PB2,PB3 is shared with external interrupt input, PB0,PB1,PB3 is shared with PWM output.
PC0 PC1 PC2 PC3	TP0 TP1 TP2 TP3	IO/I IO/I IO/I IO/I	+4	-	IO port or touch pad input.
PD0 PD1 PD2 PD3	TP4 TP5 TP6 TP7	IO/I IO/I IO/I IO/I	+4	-	IO port or touch pad input.
PE0 PE1 PE2 PE3	TP8 TP9 TP10 TP11	IO/I IO/I IO/I IO/I	+4	-	IO port or touch pad input.
PF0 PF1 PF2 PF3	TP12 TP13 TP14 TP15	IO/I IO/I IO/I IO/I	+4	-	IO port or touch pad input.
CAP	-	O	+1	-	Touch signal output.
VREG	-	Power	+1	-	LDO voltage output.
Total pad	-	-	32	-	-

§ IO Cell Type Description:

Pin Name	IO Type	Description
PA0	Figure IO-G	STD IO with internal PWM output and external interrupt trigger input.
PA1	Figure IO-C	STD IO with internal PWM output and external TCP1 clock input.
PA2	Figure IO-B	STD IO with internal PWM output.
PB0	Figure IO-E	STD IO with internal PWM output and external interrupt trigger input and IIC.
PB1	Figure IO-F	STD IO with internal PWM output and IIC.
PB2	Figure IO-D	STD IO with internal PWM output and external interrupt trigger input.
PB3	Figure IO-H	STD IO with external interrupt trigger input.
PC0~PC3	Figure IO-A	STD IO with touch pad input.
PD0~PD3	Figure IO-A	STD IO with touch pad input.
PE0~PE3	Figure IO-A	STD IO with touch pad input.
PF0~PF3	Figure IO-A	STD IO with touch pad input.

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-40~+85	℃
Storage Temperature	Tst	-50~+125	℃
Supply Voltage	VDD	VSS-0.3~VSS+6.0	V
OTP Supply Voltage	VPP	VSS-0.3~VSS+12.5	V
Input Voltage	Vin	VSS-0.3~VDD+0.3	V
Human Body Mode	ESD	>5	KV
Note: VSS symbolizes for system ground.			

§ DC and AC Characteristics

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	F_{OSCH}=4MHz, LVR on 2.2V	2.4	-	5.5	V
		F_{OSCH}=4MHz, LVR on 3.0V	3.3	-	5.5	
		F_{OSCH}=4MHz, LVR off	2.2	-	5.5	
Operating Current (Normal Mode, CPU working, IO no load)	I_{nd1}	VDD=5.0V, no load, F_{OSCL} on, F_{OSCH}=4MHz, LVR off, LDO off	-	3.5	4.0	mA
	I_{nd2}	VDD=5.0V, no load, F_{OSCL} on, F_{OSCH} off, LVR off, LDO off	-	30	50	uA
Operating Current (Sleep Mode, CPU stop, IO no load)	I_{sd1}	VDD=5.0V, no load, F_{OSCL} on, F_{OSCH}=4MHz, LVR off, LDO off	-	0.6	0.8	mA
	I_{sd2}	VDD=3.0V, no load, F_{OSCL} on, F_{OSCH} off, LVR off, LDO off	-	5	10	uA
Standby Current (Stop Mode, CPU stop, IO no load)	I_{sd3}	VDD=5.0V, no load, F_{OSCL} off, F_{OSCH} off, LVR off, LDO off	-	-	1	uA
LVR Current	I_{LVR}	VDD=5.0V		55		uA
LDO Current	I_{LDO}	VDD=5.0V		100		uA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
RSTB and INT	V_{IL}	Input Low Voltage	0	-	0.3	VDD
RSTB and INT	V_{IH}	Input High Voltage	0.7	-	1.0	VDD
PA0 Sink Current	I_{OL}	VDD=5.0V, VOL=0.6V	-	2	-	mA
PA0 Source Current	I_{OH}	VDD=5.0V, VOH=4.3V	-	-1	-	mA
Output port Sink Current (PA, PB exclude PA0)	I_{OL}	VDD=5.0V, VOL=0.6V	-	32	-	mA
Output Port Source Current (PA, PB exclude PA0)	I_{OH}	VDD=5.0V, VOH=4.3V	-	-8	-	mA
Output port Sink Current (PC, PD, PE, PF)	I_{OL}	VDD=5.0V, VOL=0.6V	-	16	-	mA
Output Port Source Current (PC, PD, PE, PF)	I_{OH}	VDD=5.0V, VOH=4.3V	-	-8	-	mA
IO Port Pull-up Resistor	R_{PH}	VDD=5.0V	100	150	200	KΩ
RSTB Pull-up Resistor	R_{PH}	VDD=5.0V	30	50	80	KΩ
Low Voltage Reset (LVR)	V_{LVR1}	For AC application	2.7	3.0	3.3	V
	V_{LVR2}		2.0	2.2	2.4	V
LDO Voltage	V_{LDO1}		3.8	4.2	4.6	V
	V_{LDO2}		2.4	2.7	3.0	V
Bandgap Voltage	V_{BGAP}		1.0	1.12	1.23	V

§ AC Characteristics: (Test condition at room temperature=25°C)

Parameter	Test Condition		Min.	Typ.	Max.	Unit
External Reset	Low active pulse width t_{RES}		2	-	-	CPU clock
Interrupt input	Low active pulse width t_{INT}		2	-	-	CPU clock
Wake up input	Low active pulse width t_{WKUP}, Application de-bounce should be manipulated by user' software		2	-	-	OSCL
System Oscillator Frequency	F_{OSCH} (Built-in RC)	VDD=5.0V	-	4M	-	Hz
Peripheral Oscillator Frequency	F_{OSCL} (Built-in RC)	VDD=5.0V	-	16K	-	Hz
Startup Period of Oscillators	T_{OSCH} (Built-in RC)	wake-up from off mode	8	-	-	T_{OSCH}
	T_{OSCL} (Built-in RC)	Wake-up from off mode	8	-	-	T_{OSCL}
Stable Time Of System Clock Switching	T_{OSCH} (Built-in RC)	OSCL→OSCH and OSCH off	8	-	-	T_{OSCL}
	(If H/L=0 then OSCH stop)					
	T_{OSCL} (Built-in RC)	OSCH→OSCL and OSCL on	-	-	-	T_{OSCL}
Timer/Counter input clock frequency	Input frequency rating, no de-bounce circuit built-in, VDD=5V		DC	-	4M	Hz
System Stable Time after Power up	After power up, the system needs to initialize the configured state and OST		-	-	40	ms

§ Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~FBF_H	-	Program ROM [4032*16]
-	000_H~007_H	File Registers
-	008_H~$01F_H$	Peripheral registers (I)
-	020_H~$19F_H$	Working RAM [384*4]
-	200_H~304_H	Peripheral registers (II)

§ Interrupt Vectors:

Interrupt Vectors	Function Description
$000	Hardware reset
$001	Hardware interrupt

§ File registers:

Address	Symbol	R/W	Default	Description
000_H	(DP1)	R/W	----	Indirect addressing register
001_H	ACC	R/W	xxxx	Accumulator and read table 1st data
002_H	TB1	R/W	xxxx	Read table 2nd data
003_H	TB2	R/W	xxxx	Read table 3rd data
004_H	TB3	R/W	xxxx	Read table 4th data
005_H	DPL	R/W	xxxx	Data pointer low nibble data
006_H	DPM	R/W	xxxx	Data pointer middle nibble data
007_H	DPH	R/W	xxxx	Data pointer high nibble data

§ Peripheral registers:

$20C_H$	TCP1C	R/W	0000	TCP1 Timer/counter control register

Address	Symbol	R/W	Default	Description
008_H	PS	R/W	-100	CPU power saving control register
009_H	PSP	R/W	0---	Peripheral power saving control register
$00A_H$	INTC	R/W	0000	Interrupt enable control register
$00B_H$	INTF	R/W	0000	Interrupt request flag register
$00C_H$	INTC1	R/W	0000	Extended interrupt enable control register
$00D_H$	INTF1	R/W	0000	Extended interrupt request flag register
$00E_H$	PWMC	R/W	-000	PWM control register
$00F_H$	PWM0L	R/W	xxxx	PWM0 duty low nibble data register
010_H	PWM0M	R/W	xxxx	PWM0 duty middle nibble data register
011_H	PWM0H	R/W	xxxx	PWM0 duty high nibble data register
012_H	PAC	R/W	-111	IO port A control register
013_H	PA	R/W	-111	IO port A output data register
014_H	PBC	R/W	1111	IO port B control register
015_H	PB	R/W	1111	IO port B output data register
016_H	PCC	R/W	1111	IO port C control register
017_H	PC	R/W	1111	IO port C output data register
018_H	PDC	R/W	1111	IO port D control register
019_H	PD	R/W	1111	IO port D output data register
$01A_H$	PEC	R/W	1111	IO port E control register
$01B_H$	PE	R/W	1111	IO port E output data register
$01C_H$	PFC	R/W	1111	IO port F control register
$01D_H$	PF	R/W	1111	IO port F output data register
$01E_H$	TPINTC	R/W	00--	Touch pad interrupt enable control register
$01F_H$	TPINTF	R/W	00--	Touch pad interrupt request flag register

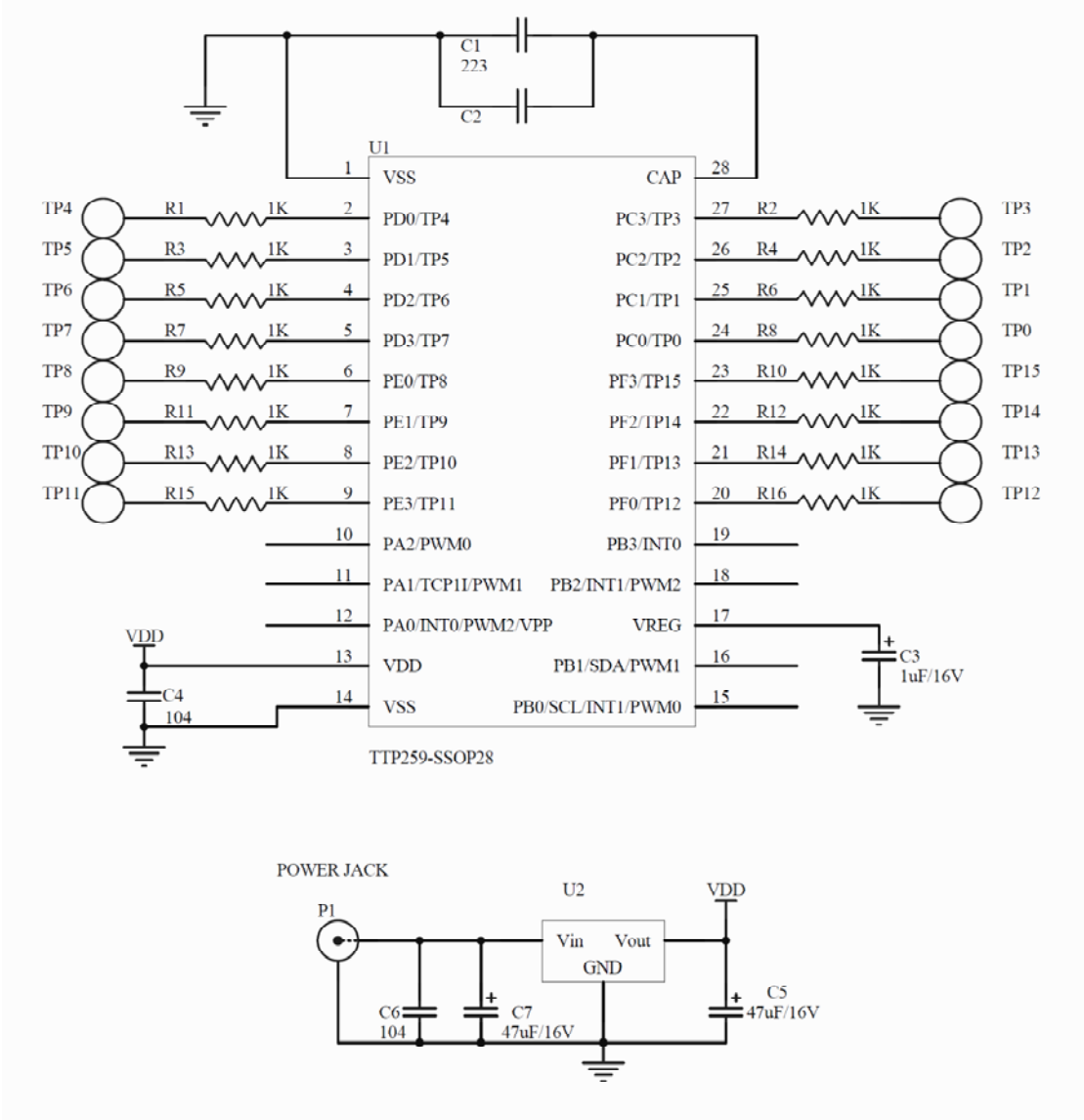
201_H	TCP1L	R/W	xxxx	TCP1 Timer/counter data low register
202_H	TCP1H	R/W	xxxx	TCP1 Timer/counter data high register
203_H	TCP2C	R/W	0000	TCP2 Timer/counter control register
204_H	TCP2L	R/W	xxxx	TCP2 Timer/counter data low register
205_H	TCP2M	R/W	xxxx	TCP2 Timer/counter data middle register
206_H	TCP2H	R/W	xxxx	TCP2 Timer/counter data high register
207_H	PAI	R	----	Port A pad data reading address
208_H	PBI	R	----	Port B pad data reading address
209_H	PCI	R	----	Port C pad data reading address
$20A_H$	PDI	R	----	Port D pad data reading address
$20B_H$	PEI	R	----	Port E pad data reading address
$20C_H$	PFI	R	----	Port F pad data reading address
$20D_H$	TCPFS	R/W	-000	TCP clock source FS pre-scale register
$20E_H$	TBC	R/W	1111	Time base control register
$20F_H$	-	-	----	-
210_H	TPCHS0	R/W	0000	Touch pad channel selector register 0
211_H	TPCHS1	R/W	0000	Touch pad channel selector register 1
212_H	TPCHS2	R/W	0000	Touch pad channel selector register 2
213_H	TPCHS3	R/W	0000	Touch pad channel selector register 3
214_H	TPCTL	R/W	-000	Touch pad control register
215_H	TPCT0	R/W	1111	Touch pad Duty counter 1st nibble
216_H	TPCT1	R/W	1111	Touch pad Duty counter 2nd nibble
217_H	TPCT2	R/W	1111	Touch pad Duty counter 3rd nibble
218_H	CSAL	R/W	0000	Touch pad C load low nibble
219_H	CSAH	R/W	--00	Touch pad C load high nibble
$21A_H$	MCKS	R/W	-111	Modulation clock selector register
$21B_H$	SPCON0	R/W	0000	Special control register 0
$21C_H$	SPCON1	R/W	0000	Special control register 1
$21D_H$	SPCON2	R/W	--00	Special control register 2
$21E_H$	LDOFLAG	R/W	---0	LDO fail flag
$21F_H$	ODATA	R/W	0000	Touch pad output register for special function
220_H	OSCHADJ	R/W	0001	OSCH frequency adjustment register

221_H	IICCON0	R/W	---1	IIC control register 0
222_H	IICCON1	R/W	0000	IIC control register 1
223_H	IICSTS	R/W	0001	IIC status register
224_H	IICDATL	R/W	xxxx	IIC data low nibble register
225_H	IICDATH	R/W	xxxx	IIC data high nibble registe
226_H	IICRDATL0	R/W	0000	IIC fast read data low nibble register 0
227_H	IICRDATH0	R/W	0000	IIC fast read data high nibble register 0
228_H	IICRDATL1	R/W	0000	IIC fast read data low nibble register 1
229_H	IICRDATH1	R/W	0000	IIC fast read data high nibble register 1
$22A_H$	PWM1L	R/W	xxxx	PWM1 duty low nibble data register
$22B_H$	PWM1M	R/W	xxxx	PWM1 duty middle nibble data register
$22C_H$	PWM1H	R/W	xxxx	PWM1 duty high nibble data register
$22D_H$	PWM2L	R/W	xxxx	PWM2 duty low nibble data register
$22E_H$	PWM2M	R/W	xxxx	PWM2 duty middle nibble data register
$22F_H$	PWM2H	R/W	xxxx	PWM2 duty high nibble data register
230_H	ADJSTAT	R	--11	Frequency Adjustment Status flag register
231_H	TBLDRL	R	0000	Time base preload register low nibble
232_H	TBLDRH	R	1000	Time base preload register high nibble
300_H	RESETF	R/W	0000	Reset flag
301_H	TBRB	W	----	Time base clear address
302_H	MRO	W	----	Mask option register enable address
303_H	CLRWDT	W	----	Clear WDT 2nd instruction
304_H	LVREN	R/W	---0	LVR enable control register

Note: a. Default means initial value after power on or reset.

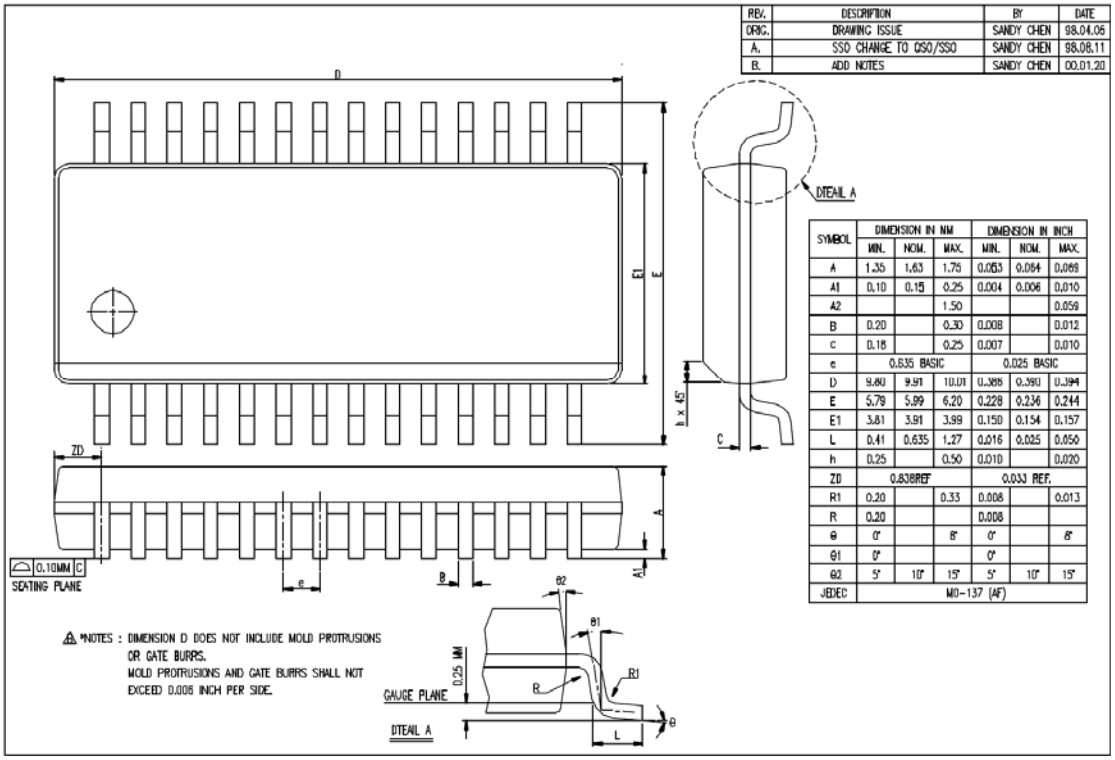
b. R is “read” only, W is “write” only, R/W is both of “read” and “write”.

§ Application Circuit：



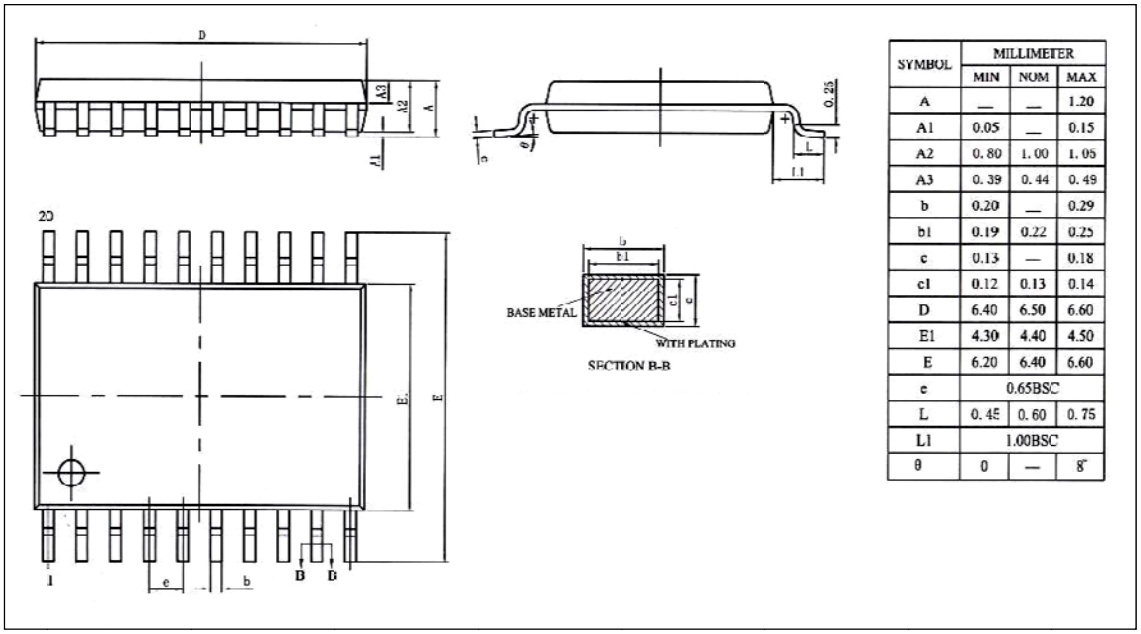
§ Package and Pad Information:

- **SSOP 28**



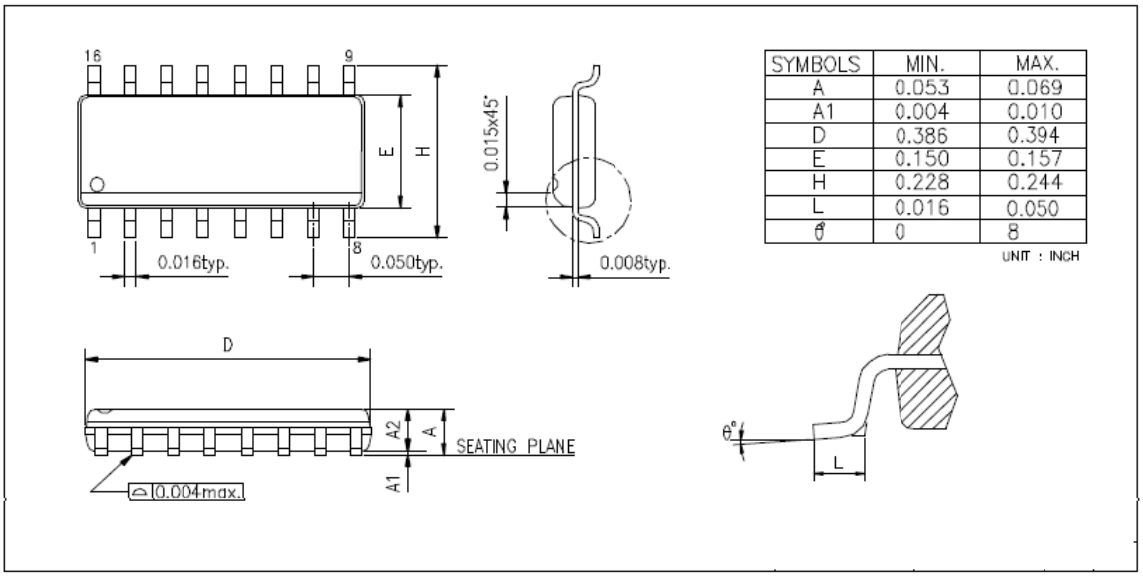
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	9.80	9.91	10.01	0.386	0.390	0.394
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
ZD	0.838REF			0.033 REF.		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AF)					

- **TSSOP 20**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

- **SOP 16**



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ	0	8

UNIT : INCH

§ Ordering Information：

	Package type
TTP259-ASFN	SSOP28-A
TTP259-DTDN	TSSOP20-B
TTP259 -EOBN	SOP16-B

§ REVISION HISTORY：

2015/05/08：(Ver. 1.0) New build
2015/05/25：(Ver. 1.1) Modify package type TSSOP20-B and SOP16-B
2018/09/20：(Ver. 1.2) Modify TSSOP20 outline diagram
2018/10/02：(Ver. 1.3) Modify Page6 Top=-40~+85